

FEATURES

Six 96 kHz DACs

Three independent stereo DAC pairs
Independent 8, 11.025, 16, 22.05, 32, 44.1,
48, 88.2, and 96 kHz sample rates
16-, 20-, and 24-bit PCM resolution
Selectable stereo mixer on outputs

Four 96 kHz ADCs

Two independent stereo ADC pairs
Simultaneous record of up to four channels
Independent 8, 11.025, 16, 22.05, 32, 44.1,
48, 88.2, and 96 kHz sample rates
16-, 20-, and 24-bit resolution

S/PDIF OUTPUT

Supports 44.1, 48, 88.2, and 96 kHz sample rates
16-, 20-, and 24-bit data widths; PCM and AC3 formats
Digital PCM gain control

DEDICATED AUXILIARY PINS

Stereo CD input w/GND sense
Mono out pin for internal speakers or telephony
Analog PCBeep input pin

ENHANCED FEATURES

Two stereo headphone amplifiers
Microsoft Vista Premium logo for notebook and desktop
95 dB audio outputs, 90 dB audio inputs
Internal 32-bit arithmetic for greater accuracy
Impedance and presence detection on all jack pins
Digital synthesis PCBeep
C/LFE channel swapping
Two general-purpose digital I/O (GPIO) pins
Advanced power management modes
EAPD control for internal speakers
48-lead, Pb-free LFCSP_VQ package

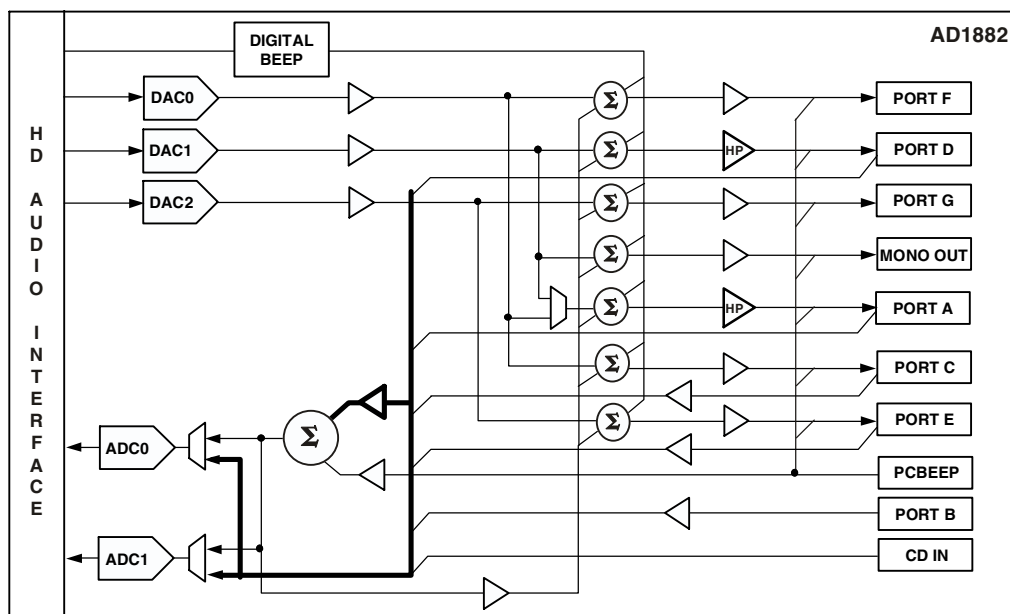


Figure 1. AD1882 Block Diagram

Rev. 0

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TABLE OF CONTENTS

General Description 3

Additional Information 3

Jack Configuration 3

AD1882 Specifications 4

Test Conditions 4

Performance 4

General Specifications 4

HD-Audio Link Specifications 6

Power Down States 6

Absolute Maximum Ratings 7

ESD Sensitivity 7

Environmental Conditions 7

Pin Configuration and Function Descriptions 8

HD Audio Widgets 11

AD1882 HD Audio Parameters 12

Outline Dimensions 16

Ordering Guide 16

REVISION HISTORY

7/07–Rev 0: Initial version

GENERAL DESCRIPTION

The AD1882 audio codec and SoundMAX® software provides superior HD audio quality that exceeds Vista Premium performance. The AD1882 has six DACs and four ADCs, two stereo headphone ports, C/LFE swapping, digital and analog PCBeep, and S/PDIF output, making the AD1882 the right choice for desktop PCs where performance is the primary consideration.

The jack retasking feature on this product supports various configurations including platforms for 5.1 on 5 or 3 jacks, and front panel jack retasking.

The AD1882 is available in a 48-lead Pb-free frame chip scale package in both reels and trays. See [Ordering Guide on Page 16](#).

ADDITIONAL INFORMATION

This data sheet provides a general overview of the AD1882 SoundMAX codec's architecture and functionality. Additional information on the AD1882 is available in the AD1882 Programmers Reference Manual. Please contact your local ADI sales representative for more information. For information on SoundMAX codecs and software see Analog Devices website at <http://www.analog.com/soundMAX>.

JACK CONFIGURATION

The guidelines shown in [Table 1](#) through [Table 3](#) should be used when selecting ports for particular functions..

Table 1. Typical Desktop Configuration with Discreet Jacks

Port	Function
Port A	Front Panel Headphone
Port B	Front Panel Microphone
Port C	Rear Panel Line-In
Port D	Rear Panel Line-Out/Headphone
Port E	Rear Panel Microphone
Port F	Rear Panel Surround
Port G	Rear Panel C/LFE

Table 2. Typical Desktop Configuration with 5.1 on 3 Jacks

Port	Function
Port A	Front Panel Headphone
Port B	Front Panel Microphone
Port C	Rear Panel Line-In/Surround
Port D	Rear Panel Line-Out/Headphone
Port E	Rear Panel Microphone / C/LFE

Table 3. Typical Notebook Configuration

Port	Function
Port A	Headphone
Port B	Microphone
Port C	Internal Microphone
Port D	Internal Stereo Speakers
Port E	Docking Station Line/Microphone In

AD1882

AD1882 SPECIFICATIONS

TEST CONDITIONS

Parameter	Test Condition
Temperature	25°C
Digital Supply	3.3 V
Analog Supply	3.3 V
MIC_BIAS_IN (via Low-Pass Filter)	5.0 V
Sample Rate f_s	48 kHz
Input Signal (Frequency Sine Wave)	1008 Hz
Amplitude for THD + N	−3.0 dB Full Scale
Analog Output Pass Band	20 Hz to 20 kHz
DAC	10 k Ω Output Load: Line Out Tests 32 Ω Output Load: Headphone Tests
ADC	0 dB Gain

PERFORMANCE

Parameter	Min	Typ	Max	Unit
Line Out Drive (10 k Ω Loads—DAC to Pin)				
Total Harmonic Distortion (THD + N)		−85		dB
Dynamic Range (−60 dB in Ref to f_s A-Weighted)		95		dB
Signal-to-Noise Ratio		95		dB
Headphone Drive (32 Ω Loads—DAC to Pin)				
Total Harmonic Distortion (THD + N)		−83		dB
Dynamic Range (−60 dB in Ref to f_s A-Weighted)		95		dB
Signal-to-Noise Ratio		95		dB
Input Ports (Pin to ADC, Mic Boost = 0 dB)				
Total Harmonic Distortion (THD + N)		−81		dB
Dynamic Range (−60 dB in Ref to f_s A-Weighted)		90		dB
Signal-to-Noise Ratio		90		dB

GENERAL SPECIFICATIONS

Table 4. AD1882 General Specifications

Parameter	Min	Typ	Max	Unit
DIGITAL DECIMATION AND INTERPOLATION FILTERS ¹				
Pass Band – f_s (kHz) = 8 ~ 96	0		0.4 f_s	Hz
Pass-Band Ripple – f_s (kHz) = 8 ~ 96			± 0.005	dB
Stop Band – f_s (kHz) = 8 ~ 96	0.6 f_s			Hz
Stop-Band Rejection – f_s (kHz) = 8 ~ 96				dB
Group Delay – f_s (kHz) = 8 ~ 96		+20	−100	1/ f_s
Group Delay Variation Over Pass Band		0		μ s
ANALOG TO DIGITAL CONVERTERS				
Resolution		24		Bits
Gain Error (Full-Scale Span Relative to Nominal Input Voltage) ²			± 10	%
Interchannel Gain Mismatch (Difference of Gain Errors)			± 0.5	dB
ADC Offset Error ¹			± 5	mV
ADC Crosstalk ¹				
Line Inputs (Input L, Ground R, Read R; Input R, Ground L, Read L)		−85		dB
Line_In to Other		−100	−80	dB

Table 4. AD1882 General Specifications (Continued)

Parameter	Min	Typ	Max	Unit
DIGITAL TO ANALOG CONVERTERS				
Resolution		24		Bits
Gain Error (Full Scale Span Relative to Nominal Input Voltage) ¹			±10	%
Interchannel Gain Mismatch (Difference of Gain Errors)			±0.5	dB
Total Audible Out-of-Band Energy (Measured from $0.6 \times f_s$ to 100 kHz) ¹		–85		dB
DAC Crosstalk				dB
(Input L, Zero R, Read R_OUT; Input R, Zero L, Read L_OUT) ¹		–95		dB
DAC VOLUMES				
Step size (DAC-0, DAC-1, DAC-2)		1.5		dB
Output Gain/Attenuation Range	–58.5		0	dB
Mute Attenuation of 0 dB Fundamental ¹		–80		dB
ADC VOLUMES				
Step size (ADCSEL-0, ADCSEL-1)		1.5		dB
PGA Gain/Attenuation Range	–58.5		+22.5	dB
Mute Attenuation of 0 dB Fundamental ¹		–80		dB
ANALOG MIXER				
Signal-to-Noise Ratio (SNR) Input to Output		95		dB
CD to Port D Output		95		dB
Port B, C, or E to Port D Output		95		dB
Port A to Port D Output		95		dB
Port D to Port A Output		95		dB
Step Size: All Mixer Inputs		1.5		dB
Input Gain/Attenuation Range: All Mixer Inputs	–34.5		+12.0	dB
ANALOG LINE LEVEL OUTPUTS				
Full-Scale Output Voltage	1.0	1.0		V _{rms} ³
Ports C, E, F, and G Mono Out	2.83			V _{p-p}
Output Impedance ¹			300	Ω
External Load Impedance ¹	10			kΩ
Output Capacitance ¹		15		pF
External Load Capacitance			1000	pF
ANALOG HP DRIVE OUTPUTS				
Full-Scale Output Voltage	1.0			V _{rms} ³
Ports A and D	2.83			V _{p-p}
Output Impedance ¹			0.5	Ω
External Load Impedance ¹	32			Ω
Output Capacitance ¹		15		pF
External Load Capacitance ¹			1000	pF
ANALOG INPUTS				
CD, Port D (When Used as Input)		1		V _{rms} ³
		2.83		V _{p-p}
Microphone Boost Amplifier, Ports B, C, or E (When Used as Inputs)		1		V _{rms} ³
		2.83		V _{p-p}
Boost = 0 dB		0.316		V _{rms} ³
		0.894		V _{p-p}
Boost = 10 dB		0.1		V _{rms} ³
		0.283		V _{p-p}
Boost = 20 dB		0.032		V _{rms} ³
		0.089		V _{p-p}
Boost = 30 dB		20		kΩ
Input Impedance ¹		5	7.5	pF
Input Capacitance ¹				

AD1882

Table 4. AD1882 General Specifications (Continued)

Parameter	Min	Typ	Max	Unit
Digital GPIO Pins: GPIO_0, GPIO_1/EAPD				
Input Signal High (V_{IH})	$DV_{IO} \times 0.60$		DV_{IO}	V
Input Signal Low (V_{IL})	0		$DV_{IO} \times 0.24$	V
Input Leakage Current (Signal High, (I_{IH}))		150		nA
Input Leakage Current (Signal Low, (I_{IL}))		50		μ A
Output Signal High (V_{OH})	$DV_{IO} \times 0.72$		DV_{IO}	V
Output Signal Low (V_{OL})	0		$DV_{IO} \times 0.10$	V
$I_{OUT} = -500 \mu A$				
$I_{OUT} = +1500 \mu A$				
S/PDIF_OUT				
Output Signal High (V_{OH})	$DV_{IO} \times 0.72$		DV_{IO}	V
Output Signal Low (V_{OL})	0		$DV_{IO} \times 0.10$	V
$I_{OUT} = -500 \mu A$				
$I_{OUT} = +1500 \mu A$				
POWER SUPPLY				
Analog (AV_{DD}) 3.3 V $\pm 5\%$				
Power Supply Range	3.13	3.30	3.46	V
Power Dissipation		119		mW
Supply Current		36		mA
Digital (DV_{DD}) 3.3 V $\pm 10\%$				
Power Supply Range	2.97	3.30	3.63	V
Power Dissipation		198		mW
Supply Current		60		mA
Digital I/O (DV_{IO}) 3.3 V $\pm 10\%$				
Power Supply Range	2.97	3.30	3.63	V
Power Dissipation		3.96		mW
Supply Current		1.20		mA
Power Supply Rejection (100 mV p-p Signal @ 1 kHz) ¹		80		dB

¹ Guaranteed but not tested.

² Measurements reflect main ADC.

³ RMS values assume sine wave input.

HD-AUDIO LINK SPECIFICATIONS

HD-Audio signals comply with the High Definition Audio specifications. Please refer to these specifications at:
<http://www.intel.com/standards/hdaudio/>

POWER DOWN STATES

Table 5. Power Down States

Parameter	ID _{VDD} Typ	IA _{VDD} Typ	Unit
Function node in D0, all nodes active	60	36	mA
Function node in D3 ¹	23	1.2	mA
Codec in $\overline{RESET}$	3	3	mA
Individual block power savings			
DAC pair powered down saves (each)	6	6	mA
ADC pair powered down saves (each)	5	4.4	mA
Mixer power control (and associated amps) saves	0	3	mA
MIC_BIAS powered down saves ²	0	1.0	mA

¹ Function node D3 state powers down all nodes except for the V_{REF} , Mixer and MIC_BIAS nodes which have independent power controls. V_{REF} should be kept active when background functions such as jack presence detection or analog pass-through are required. Mixer should be kept active when analog pass-through is required. MIC_BIAS can be disabled if microphones are not in use in the power-down state.

² Powering down the MIC_BIAS powers down all port MIC_BIAS pins. This disables all microphone bias circuits set to 100% or 50%, setting them to the Hi-Z state. The 0 Ω and Hi-Z states remain unaffected by the MIC_BIAS power state.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 6 may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Absolute Maximum Ratings

Power Supplies	Min	Max	Units
Digital (DV _{DD})	−0.30	+3.65	V
Digital I/O (DV _{IO})	−0.30	+3.65	V
Analog (AV _{DD})	−0.30	+3.65	V
Input Current (Except Supply Pins)		±10.0	mA
Analog Input Voltage (Signal Pins)	−0.30	AV _{DD} + 0.3	V
Digital Input Voltage (Signal Pins)	−0.30	DV _{IO} + 0.3	V
Ambient Temperature (Operating)	0	+70	°C
Storage Temperature	−65	+150	°C

ESD SENSITIVITY



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating

$$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$$

T_{CASE} = Case Temperature in °C

PD = Power Dissipation in W

θ_{CA} = Thermal Resistance (Case-to-Ambient)

θ_{JA} = Thermal Resistance (Junction-to-Ambient)

θ_{JC} = Thermal Resistance (Junction-to-Case)

All measurements per EIA-JESD51 with 2S2P test board per EIA-JESD51-7.

Table 7. Thermal Resistance

Package	θ_{JA}	θ_{JC}	θ_{CA}	Unit
LFCSP_VQ	47	15	32	°C/W

AD1882

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

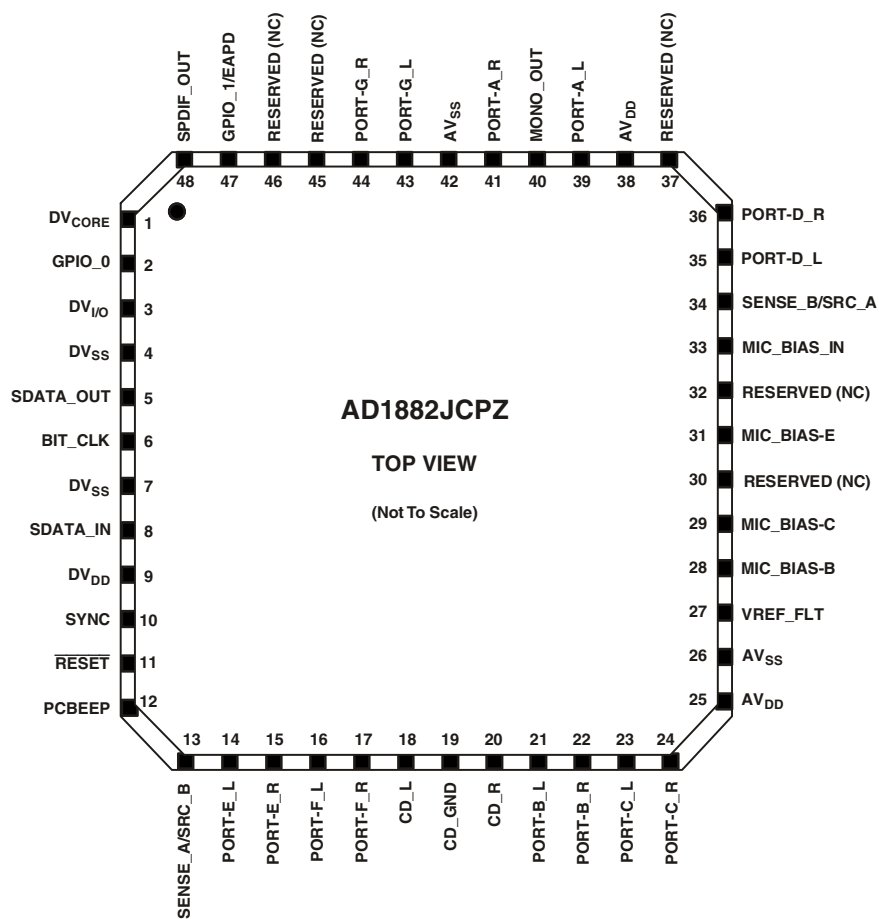


Figure 2. AD1882 48-Lead Package and Pinout

Table 8. AD1882 Pin Descriptions

Mnemonic	Pin No.	Function	Description
DIGITAL INTERFACE			
SDATA_OUT	5	I	Link Serial Data Output. AD1882 input stream. Clocked on both edges of the BIT_CLK.
BIT_CLK	6	I	Link Bit Clock. 24.000 MHz serial data clock.
SDATA_IN	8	I/O	Link Serial Data Input. AD1882 output stream Clocked only on one edge of BIT_CLK.
SYNC	10	I	Link Frame Sync.
RESET	11	I	Link Reset. AD1882 master hardware reset
DIGITAL I/O			
GPIO_0	2	I/O	General Purpose Input/Output Pin. Digital signal used to control external circuitry.
GPIO_1/EAPD	47	I/O	General Purpose Input/Output Pin/EAPD Pin. Digital signal used to control external circuitry. Defaults to Hi-Z. When used as EAPD: Hi-Z = amp-on, DV _{SS} = amp off.
S/PDIF_OUT	48	O	S/PDIF_OUT. Supports S/PDIF output.
JACK SENSE AND EAPD			
SENSE_A/SRC_B	13	I/O	JACK SENSE A-D Input/Sense B Drive.
SENSE_B/SRC_A	34	I/O	JACK SENSE E-H Input/Sense A Drive.
ANALOG I/O			
PCBEEP	12	LI	Monaural Input from System for Analog PCBeep.
PORT-E_L	14	LI, MIC, LO, SWAP	Auxiliary Input/Output Left Channel.
PORT-E_R	15	LI, MIC, LO, SWAP	Auxiliary Input/Output Right Channel.
PORT-F_L	16	I/O	Auxiliary Input/Output Left Channel.
PORT-F_R	17	I/O	Auxiliary Input/Output Right Channel.
CD_L	18	LI	CD Audio Left Channel.
CD_GND	19	LI	CD-Audio-Analog-Ground-Reference (for Differential CD Input). Must be connected to AGND via 0.1 mF capacitor if not in use as CD_GND.
CD_R	20	LI	CD Audio Right Channel.
PORT-B_L	21	LI, MIC, HP, LO	Front Panel Stereo MIC/Line-In.
PORT-B_R	22	LI, MIC, HP, LO	Front Panel Stereo MIC/Line-In.
PORT-C_L	23	LI, MIC, LO	Rear Panel Stereo MIC/Line-In.
PORT-C_R	24	LI, MIC, LO	Rear Panel Stereo MIC/Line-In.
PORT-D_L	35	LI, HP, LO	Rear Panel Headphone/Line-Out.
PORT-D_R	36	LI, HP, LO	Rear Panel Headphone/Line-Out.
PORT-A_L	39	LI, MIC, HP, LO	Front Panel Headphone/Line-Out.
MONO_OUT	40	LO	Monaural Output to Internal Speaker or Telephony Subsystem Speakerphone.
PORT-A_R	41	LI, MIC, HP, LO	Front Panel Headphone/Line-Out.
PORT-G_L	43	LO, SWAP	Rear Panel C/LFE Output.
PORT-G_R	44	LO, SWAP	Rear Panel C/LFE Output.
FILTER/REFERENCE			
MIC_BIAS-B	28	O	Switchable Microphone Bias. For use with Port B (Pins 21, 22).
MIC_BIAS-C	29	O	Switchable Microphone Bias. For use with Port C (Pins 23, 24).
MIC_BIAS-E	31	O	Switchable Microphone Bias. For use with Port E (Pins 14, 15).
DV _{CORE}	1	O	CAUTION: DO NOT APPLY 3.3 V TO THIS PIN! Filter connection for internal core voltage regulator. This pin must be connected to filter caps: 10 μ F, 1.0 μ F, and 0.1 μ F connected in parallel between Pin 1 and DV _{SS} (Pin 4).
VREF_FLT	27	O	Voltage Reference Filter. This pin must be connected to filter caps: 1.0 μ F and 0.1 μ F connected in parallel between Pin 27 and AV _{SS} (Pins 26, 42).

The symbols used in this table are defined as: I = Input, O = Output, LI = Line level input, LO = Line level output, HP = Output capable of driving headphone load, MIC = Input supports microphones with MIC bias and boost amplifier, SWAP = Outputs can swap L/R channels (typically used to support C/LFE or shared C/LFE function).

AD1882

Table 8. AD1882 Pin Descriptions (Continued)

Mnemonic	Pin No.	Function	Description
POWER AND GROUND			
DV _{I/O} (3.3V)	3	I	Connect to the I/O Voltage Used for the HD-Audio Controller Signals.
DV _{SS}	4, 7	I	Digital Supply Return (Ground).
DV _{DD} (3.3 V)	9	I	Digital Supply Voltage 3.3 V. This is regulated down to DV _{CORE} on Pin 1 to supply the internal digital core internal to the AD1882.
AV _{DD} (3.3 V)	25, 38	I	CAUTION: DO NOT APPLY 5.0 V TO THESE PINS! Analog supply voltage 3.3 V ONLY. Note: AV _{DD} supplies should be well regulated and filtered as supply noise degrades audio performance.
MIC_BIAS_IN	33	I	Source Power for Microphone Bias Boost Circuitry.
AV _{SS}	26, 42	I	Analog Supply Return (Ground). AV _{SS} should be connected to DV _{SS} using a conductive trace under, or close to, the AD1882.

The symbols used in this table are defined as: I = Input, O = Output, LI = Line level input, LO = Line level output, HP = Output capable of driving headphone load, MIC = Input supports microphones with MIC bias and boost amplifier, SWAP = Outputs can swap L/R channels (typically used to support C/LFE or shared C/LFE function).

HD AUDIO WIDGETS

In the following table, node IDs that are not shown are reserved for future use.

Table 9. HD Audio Widgets

Node ID	Name	Type ID	Type	Description
00	ROOT	x	Root	Device Identification
01	FUNCTION	x	Function	Designates this Device as an Audio Codec
02	S/PDIF DAC	0	Audio Output	S/PDIF Digital Stream Output Interface
03	DAC_0	0	Audio Output	Headphone/Surround Side (7.1) Channel Digital/Audio Converters
04	DAC_1	0	Audio Output	Stereo Front Channel Digital/Audio Converters
05	DAC_2	0	Audio Output	Stereo C/LFE Channel Digital/Audio Converters
08	ADC_0	1	Audio Input	Stereo Record Channel 1 Audio/Digital Converters
09	ADC_1	1	Audio Input	Stereo Record Channel 2 Audio/Digital Converters
0B	S/PDIF Mix Selector	3	Audio Selector	Selects which ADC Drives the S/PDIF Mixer
0C	ADC Selector 0	3	Audio Selector	Selects and Amplifies/Attenuates the Input to ADC_0
0D	ADC Selector 1	3	Audio Selector	Selects and Amplifies/Attenuates the Input to ADC_1
10	Digital Beep	7	Beep Generator	Internal Digital PCBeep Signal
11	Port A (Headphone)	4	Pin Complex	Front Panel Headphone/Microphone Jack
12	Port D (Front L/R)	4	Pin Complex	Rear Panel Front/Headphone Jack
13	Mono Out	4	Pin Complex	Monorail Output Pin (Internal Speakers or Telephony System)
14	Port B (Front Mic)	4	Pin Complex	Front Panel Microphone/Headphone Jack
15	Port C (Line In)	4	Pin Complex	Rear Panel Line-In Jack
16	Port F (Surr Back)	4	Pin Complex	Rear Panel Surround-Rear (5.1) Jack
17	Port E (Rear Mic)	4	Pin Complex	Rear Panel Mic Jack
18	CD In	4	Pin Complex	Analog CD Input
19	Mixer Power Down	5	Power Widget	Powers Down the Analog Mixer and Associated Amps
1A	Analog PCBeep	4	Pin Complex	External Analog PCBeep Signal Input
1B	S/PDIF Out	4	Pin Complex	S/PDIF Output Pin
1D	S/PDIF Mixer	2	Audio Mixer	Mixes the Selected ADC with the Digital Stream to Drive S/PDIF Out
1E	Mono Out Mixer	2	Audio Mixer	Selects Which Source Drives the Mono Out Signal
20	Analog Mixer	2	Audio Mixer	Mixes Individually Gainable Analog Inputs
21	Mixer Output Atten	3	Audio Selector	Attenuates the Mixer Output to Drive the Port Mixers
22	Port A Mixer	2	Audio Mixer	Mixes the Port A Selected DAC and Mixer Output Amps to Drive Port A
23	VREF Power Down	F	Vendor Defined	Powers Down the Internal and External VREF Circuitry
24	Port G (C/LFE)	4	Pin Complex	Rear Panel C/LFE Jack
26	Port E Mixer	2	Audio Mixer	Mixes DAC_1 and Mixer Output Amps to Drive Port E
27	Port G Mixer	2	Audio Mixer	Mixes DAC_1 and Mixer Output Amps to Drive Port G
29	Port D Mixer	2	Audio Mixer	Mixes DAC_0 and Mixer Output Amps to Drive Port D
2A	Port F Mixer	2	Audio Mixer	Mixes DAC_2 and Mixer Output Amps to Drive Port F
2C	Port C Mixer	2	Audio Mixer	Mixes the Port C Selected DAC and Mixer Output Amps to Drive Port C
2D	Stereo Mix Down	2	Audio Mixer	Mixes the Stereo L/R Channels to Drive Mono Output
2F	BIAS Power Down	F	Vendor Defined	Powers Down the Internal MIC_BIAS_FILT and all MIC_BIAS Pins
37	Port A Out Selector	3	Audio Selector	Selects the Port A DAC (0, 1)
39	Port B Boost	3	Audio Selector	Microphone Boost Amp for Port B
3A	Port C Boost	3	Audio Selector	Microphone Boost Amp for Port C
3C	Port E Boost	3	Audio Selector	Microphone Boost Amp for Port E

AD1882 HD AUDIO PARAMETERS

The SSID value is set on codec power-up only. SSID is not reset by link or soft reset in order to preserve modifications by BIOS control.

Table 10. Root and Function Node Parameters

Node ID	Name	Vendor ID 00	01	Revision ID 02 ¹	03	Sub Node Count 04	Func. Group Type 05	Audio F.G. Caps 08	GPIO Caps 11
00	ROOT	11D41882		00100100		00010001			
01	FUNCTION					0002003B	00000001	00010C0C	40000002

¹ Subject to change with silicon stepping.

Table 11. SubSystem ID ¹

SubSystem ID			31:16	15:8	7:0
Node ID	Name	Value	SSID	SKU	Asm ID
01	FUNCTION	BFD20000	BFD2	00	00

¹ The default SSID is over-written by platform BIOS after power on. It is preserved across HD Audio link reset and verb reset.

Table 12. Widget Parameters

Node ID	Widget Capabilities 09	PCM Size, Rate 0A	Stream Formats 0B	Pin Capabilities 0C	Input Amp Capabilities 0D	ConnList Length 0E	Power States 0F	Processing Caps 10	Output Amp Capabilities 12	Volume Knob Capabilities 13
01	00000480	000E01FF	00000001		80000000		00000009		00052727	
02	0003031D	000E01E0	00000005			00000001			80052727	
03	00000405	000E01FF	00000001			00000000	00000009		00052727	
04	00000405	000E01FF	00000001			00000000	00000009		00052727	
05	00000405	000E01FF	00000001			00000000	00000009		00052727	
08	00100501	000E01FF	00000001			00000001	00000009			
09	00100501	000E01FF	00000001			00000001	00000009			
0B	00300301					00000002				
0C	0030010D					00000008			80053627	
0D	0030010D					00000008			80053627	
10	0070000C					00000000			800B0F0F	
11	0040018D			0000373F		00000001			80000000	
12	0040058D			0001003F		00000001	00000009		80000000	
13	0040050C			00010010		00000001	00000009		80051F1F	
14	00400081			00003727		00000000				
15	0040018D			00003737		00000001			80000000	
16	0040018D			00000017		00000001			80000000	
17	0040098D			00003737		00000001			80000000	
18	00400001			00000020		00000000				
19	00500500					00000002	00000009			
1A	00400000			00000020		00000000				
1B	00400301			00000010		00000001				
1D	00200303				80000000	00000002				
1E	00200103				80000000	00000002				
1F	00F00100			00000010		00000001				
20	0020010B				80051F17	00000008				
21	0030010D					00000001			80051F1F	
22	00200103				80000000	00000002				
23	00F00100					00000008				
24	0040098D			00000017		00000001			80000000	
26	00200103				80000000	00000002				
27	00200103				80000000	00000002				
29	00200103				80000000	00000002				
2A	00200103				80000000	00000002				
2C	00200103				80000000	00000002				
2D	00200100					00000001				
2F	00F00100					00000003				
37	00300101					00000002				
39	0030010D					00000001			00270300	
3A	0030010D					00000001			00270300	
3C	0030010D					00000001			00270300	

Table 13. Connection List

Node ID	Connections		0	1		2		3		4		5		6		7	
	[0-3]	[4-7]	NID	I	NID	I	NID	I	NID	I	NID	I	NID	I	NID	I	NID
02	0000001D		1D														
03																	
04																	
05																	
08	0000000C		0C														
09	0000000D		0D														
0B	00000908		08		09												
0C	18BC3911	20123B3B	11		39	1	3C		18		3B		3B		12		20
0D	18BC3911	20123B3B	11		39	1	3C		18		3B		3B		12		20
10																	
11	00000022		22														
12	00000029		29														
13	0000002D		2D														
14																	
15	0000002C		2C														
16	0000002A		2A														
17	00000026		26														
18																	
19	00002120		20		21												
1A																	
1B	00000002		02														
1D	00000B01		01		0B												
1E	00002104		04		21												
1F	00000002		02														
20	12113A39	1A183B3C	39		3A		11		12		3C		3B		18		1A
21	00000020		20														
22	00002137		37		21												
23	A2209811	BC30AE24	11	1	18		20	1	22		24	1	2E		30	1	3C
24	00000027		27														
26	00002105		05		21												
27	00002105		05		21												
29	00002104		04		21												
2A	00002106		03		21												
2C	00002131		03		21												
2D	0000001E		1E														
2F	00171514		14		15		17										
37	00000403		03		04												
39	00000014		14														
3A	00000015		15														
3C	00000017		17														

In [Table 14](#), default configuration values are set on codec power-up only. Default configuration values are not reset by link or soft reset to preserve modifications by BIOS control.

Table 14. Default Configuration Bytes

Name	Value	31:30	29:28	27:24	23:20	19:16	15:12	8	7:4	3:0
		Connectivity	Location		Def. Device	Conn Type	Color	Misc.	Def Assn	Sequence
			Chasis	Position				JD Over Ride		
Port A (Headphone)	0221401F	Jack	External	Front	HP Out	1/8" Jack	Green	0	1	F
Port D (Front L/R)	01014010	Jack	External	Rear	Line Out	1/8" Jack	Green	0	1	0
Mono Out	901701F0	Fixed	Internal	N/A	Speaker	Other Analog	Unknown	1	F	0
Port B (Front Mic)	02A190F0	Jack	External	Front	Mic In	1/8" Jack	Pink	0	F	0
Port C (Line In)	01813021	Jack	External	Rear	Line In	1/8" Jack	Blue	0	2	1
Port F (Surr Back)	01011012	Jack	External	Rear	Line Out	1/8" Jack	Black	0	1	2
Port E (Rear Mic)	01A19020	Jack	External	Rear	Mic In	1/8" Jack	Pink	0	2	0
CD IN	9933012E	Fixed	Internal	Special 3	CD	ATAPI	Unknown	1	2	E
Analog PCBeep	90F701F0	Fixed	Internal	N/A	Other	Other Analog	Unknown	1	F	0
S/PDIF Out	014511F0	Jack	External	Rear	SPDIF Out	Optical	Black	1	F	0
Port G (C/LFE)	01016011	Jack	External	Rear	Line Out	1/8" Jack	Orange	0	1	1

AD1882

OUTLINE DIMENSIONS

Dimensions are shown in millimeters.

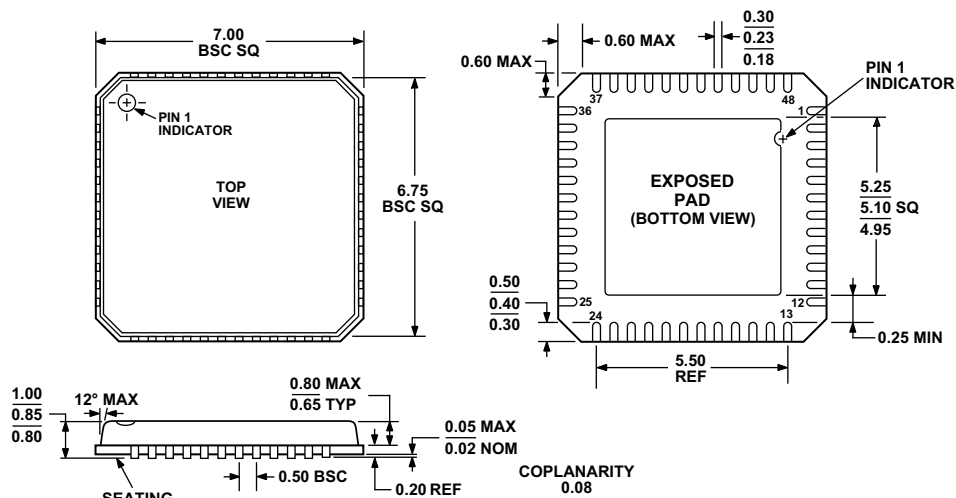


Figure 3. 48-Lead, Lead Frame Chip Scale Package [LFCSP_VQ]
7 mm x 7 mm Body, Very Thin Quad
(CP-48-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD1882JCPZ ¹	0°C to 70°C	48-Lead LFCSP_VQ	CP-48-1
AD1882JCPZ-RL ¹	0°C to 70°C	48-Lead LFCSP_VQ	CP-48-1

¹ Z = RoHS Compliant Part.