Highly Programmble Voltage Supervisory Circuit

NOTE: THIS PRODUCT HAS REACHED END OF LIFE

FEATURES

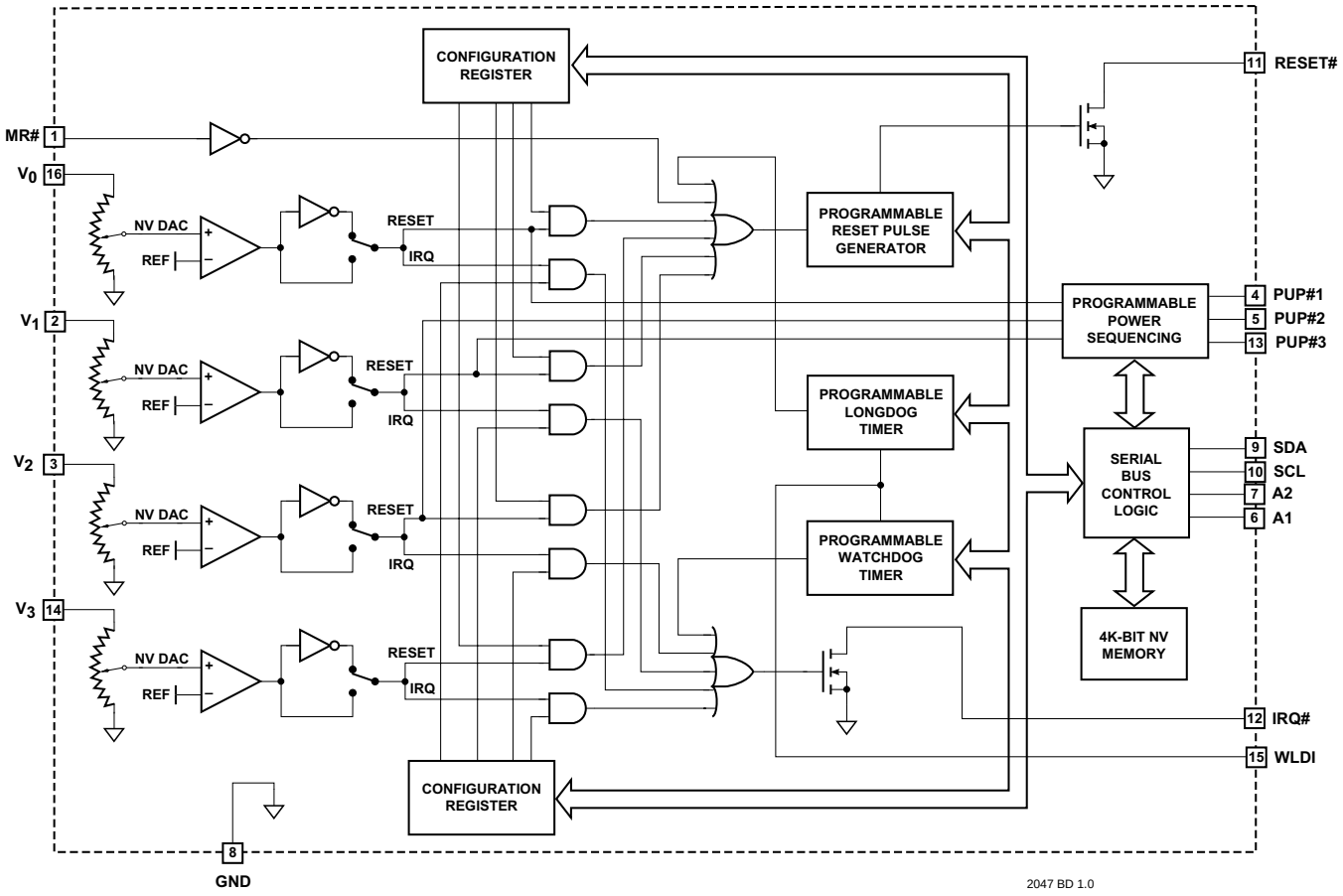
- Operational from any of four Voltage Monitoring Inputs
- Programmability allows monitoring any voltage between 0.9V and 6.0V with NO external components
- Programmable Watchdog Timer
- Programmable Longdog™ Timer
- Programmable Reset Pulse Width
- Programmable Power-up sequencing
- Programmable Nonvolatile Combinatorial Logic for generation of reset and interrupt outputs
- Fault Status Register

INTRODUCTION

The SMS44 is a highly programmable voltage supervisory circuit designed specifically for advanced systems needing to monitor multiple voltages. The SMS44 can monitor four separate voltages without the need of any external voltage divider circuitry

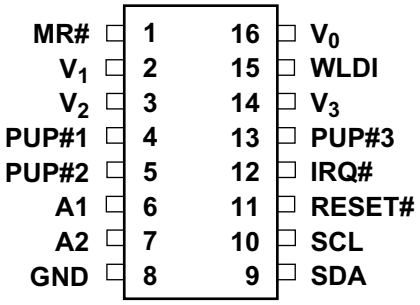
The SMS44 watchdog timer has a user programmable timeout period and it can be placed in an idle mode for system initialization or system debug. All of the functions are user accessible through an industry standard 2-wire serial interface.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

16-Pin SOIC or
16-Pin SSOP



2047 T PCon 2.0

PIN NAMES

Pin	Name	Function
1	MR#	Manual reset input
2	V_1	Voltage supply and monitor input
3	V_2	Voltage supply and monitor input
4	PUP#1	Power up permitted output
5	PUP#2	Power up permitted output
6	A1	Address input
7	A2	Address input
8	GND	Power supply return
9	SDA	Serial data I/O
10	SCL	Serial data clock
11	RESET#	Reset out
12	IRQ#	Interrupt out
13	PUP#3	Power up permitted output
14	V_3	Voltage supply and monitor input
15	WLDI	Watchdog/longdog timer interrupt
16	V_0	Voltage supply and monitor input

2047 Pins Table 2.0

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -55°C to 125°C
Storage Temperature ..... -65°C to 150°C
Lead Solder Temperature (10 secs) ..... 300 °C
Terminal Voltage with Respect to GND:
V_0, V_1, V_2, and V_3 ..... -0.3V to 6.0V
All Others ..... -0.3V to 6.0V

*COMMENT

Stresses beyond the listed Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

DC OPERATING CHARACTERISTICS

(**Over Recommended Operating Conditions; Voltages are relative to GND**)

Symbol	Parameter	Notes			Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage	1V min. refers to a valid reset output being generated			1.0		5.5	V
		Memory read/write operations: at least one of the V inputs must be at or above V_{CC} min.			2.7		5.5	V
I_{CC}	Supply current	3.6V < VCC ≤ 5.5V				25	50	µA
		3.6V ≥ VCC				25	50	µA
		Configuration register or memory access					2	mA
V_{PTH} Range	Programmable threshold range	Reset threshold voltage range V_0 to V_3 (20mV increments)			0.9		6.0	V
V_{PTH}	Programmable threshold				–10	V_{PTH}	10	mV
V_{HYST}	V_{RST} hysteresis					50		mV
V_{OL}	RESET# low voltage output	I_{SINK} = 1.2mA, V_{CC} = V_{RST} min.					0.3	V
		I_{SINK} = 1.2mA, V_{CC} ≥ 2.7V					0.3	V
	IRQ# low voltage output	I_{SINK} = 1.2mA, V_{CC} = V_{RST} min.					0.3	V
		I_{SINK} = 200µA, V_{CC} = 1.2V					0.3	V
t_{PRTO}	Programmable reset pulse width		RTO1	RTO0				
			0	0	20	25	30	msec
			0	1	35	50	65	
			1	0	65	100	135	
			1	1	130	200	270	
t_{DRST}	V in to RESET# delay	100mV overdrive				20		µs

2047 Elect TableA 2.1

Symbol	Parameter	Notes			Min.	Typ.	Max.	Unit
t_{PWDTO}	Programmable watchdog timer period	WD2	WD1	WD0				
		0	0	0		OFF		
		0	1	1	280	400	520	ms
		1	0	0	560	800	1040	
		1	0	1	1120	1600	2080	
		1	1	0	2240	3200	4160	
		1	1	1	4480	6400	8320	
t_{PLDTO}	Programmable longdog timer period		LD1	LD0				
			0	0		OFF		
			0	1	1120	1600	2080	ms
			1	0	2240	3200	4160	
			1	1	4480	6400	8320	
$t_{PDLY}X$	Programmable delay from V_{PTH} to PUP# out		PUP#X-1	PUP#X-0				
			0	0		OFF		
			0	1		25		ms
			1	0		50		
			1	1		100		
I_{MR}	MR# pullup current					100		µA
T_{MR}	MR# input pulse width				50			ns
T_{DMRRST}	Delay from MR# low to RESET# low					100		ns
V_{IL}	MR# input threshold						0.6	V
V_{IH}					$0.7 \times V_{CC}$			V

2047 Elect TableB 2.0

PIN DESCRIPTIONS

V_0 through V_3

These inputs are used as the voltage monitor inputs and as the voltage supply for the SMS44. Internally they are diode ORed and the input with the highest voltage potential will be the default supply voltage.

The RESET# output will be true if any one of the four inputs is above 1V. However, for full device operation at least one of the inputs must be at 2.7V or higher.

The sensing threshold for each input is independently programmable in 20mV increments from 0.9V to 6.0V. Also, the occurrence of an under- or over-voltage condition that is detected as a result of the threshold setting can be used to generate subsequent action(s), such as RESET# or IRQ#. The programmable nature of the threshold voltage eliminates the need for external voltage divider networks.

PUP#1, PUP#2, PUP#3

These are the power-up permitted outputs when the SMS44 is programmed to provide the sequencing of LDOs or DC to DC converters. Each delay is independently enabled and programmable for its duration (**configuration register 7**). If all PUP# outputs are enabled the sequence would be as follows: V_0 above threshold then delay to PUP#1 turning on; V_1 above threshold then delay to PUP#2 turning on; V_2 above threshold then delay to PUP#3 turning on to end the sequence.

MR#

The manual reset input always generates a RESET# output whenever it is driven low. The duration of the RESET# output pulse will be initiated when MR# goes low and it will stay low for the duration of MR# low plus the programmed reset timeout period (t_{PRTO}). If MR# is brought low during a power-on-sequence of the PUP#s the sequence will be halted for the reset duration, and will then resume from the point at which it was interrupted. If MR# is low the configuration registers can be read or written to so long as at least one of the V_X inputs is ≥2.7V.

RESET#

The reset output is an active low open drain output. It will be driven low whenever the MR# input is low or whenever an enabled under-voltage or over-voltage condition exists, or when a longdog timer expiration exists. The four voltage monitor inputs are always functioning, but their ability to generate a reset is programmable (**configuration register 4**). Refer to figures 1 and 2 for a detailed illustration of the relationship between MR#, IRQ#, RESET# and the V_{IN} levels.

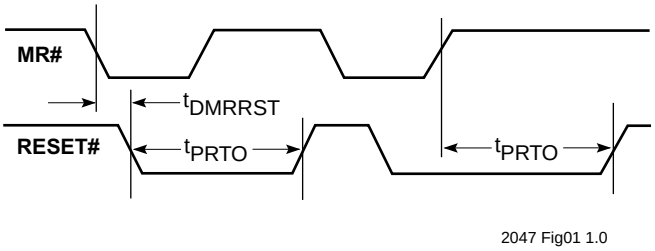


Figure 1. RESET# Timing with MR#

IRQ#

The interrupt output is an active low open-drain output. It will be driven low whenever the watchdog timer times out or whenever an enabled under-voltage or over-voltage condition on a V input exists (**configuration register 6**).

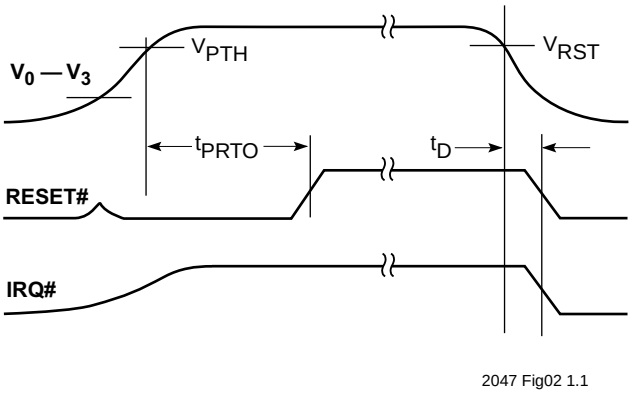


Figure 2. RESET# Timing with IRQ#

WLDI

Watchdog and longdog timer interrupt input. A low to high transition on the WLDI input will clear both the watchdog and longdog timers, effectively starting a new timeout period.

If WLDI is stuck low and no low-to-high transition is received within the programmed t_{PWDTO} period (programmed watch dog timeout) IRQ# will be driven low. If a transition is still not received within the programmed t_{PLDTO} period (programmed longdog timeout) RESET# will be driven low. Refer to Figure 3 for a detailed illustration.

Holding WLDI high will block interrupts from occurring but will not block the longdog from timing out and generating a reset. Refer to Figure 4 for a detailed illustration of the relationship between IRQ#, RESET#, and WLDI.

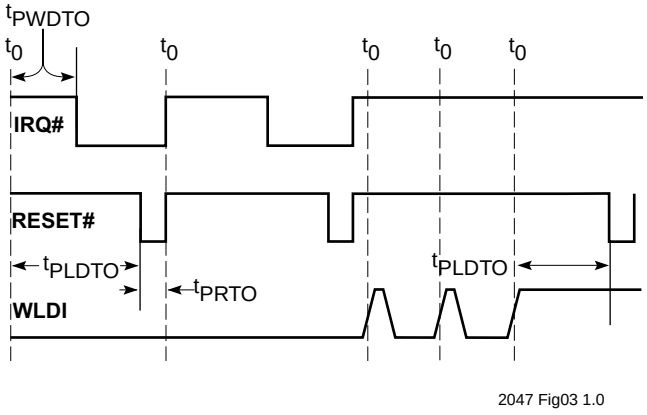


Figure 3. Watchdog, Longdog and WLDI Timing

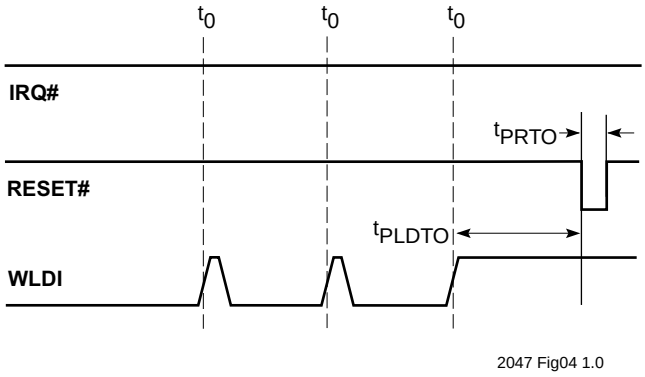


Figure 4. Watchdog, Longdog and WLDI Timing

A1, A2

A1 and A2 are the address inputs. When addressing the SMS44 memory or configuration registers the address inputs distinguish which one of four possible devices sharing the common bus is being addressed.

SDA

SDA is the serial data input/output pin. It should be tied to V_{CC} through a pull-up resistor.

SCL

SCL is the serial clock input. It should be tied to V_{CC} through a pull-up resistor.

DEVICE OPERATION

SUPPLY AND MONITOR FUNCTIONS

The V_0, V_1, V_2 and V_3 inputs are internally diode-ORed so that any one of the four can act as the device supply. The RESET# output will be guaranteed true so long as one of the four pins is at or above 1V.

> **Note***: for performing a memory operation (read or write) and to have the ability to change configuration register contents at least one supply input must be above 2.7V.*

If sequencing is enabled, the designer must insure V_0 is the primary supply and is the first to become active.

Associated with each input is a comparator with a programmable threshold for detection of under-voltage conditions on any of the four supply inputs. The threshold can be programmed in 20mV increments anywhere within the range of 0.9V to 6.0V. Configuration registers 0, 1, 2, and 3 adjust the thresholds for V_0, V_1, V_2 and V_3 respectively.

If the value contained in the register is all zeroes, the corresponding threshold will be 0.9V. If the contents were 05_{HEX} the threshold would then be 1.0V [0.9V + (5 × 0.02V)]. All four registers are configured as 8-bit registers.

RESET AND IRQ FUNCTIONS

Both the reset and interrupt outputs have four programmable sources for activation. Configuration register 4 is used for selecting the activation source, which can be any combination of V_0, V_1, V_2 and V_3. A monitor input can only be programmed to activate on either an under-voltage or over-voltage condition, but not both conditions.

The RESET# output has two hardwired sources for activation: the MR# input, and the expiration of the Longdog timer. RESET# will remain active so long as MR# is low, and will continue driving the RESET# output for t_{PRTO} (programmable reset time out) after MR# returns high. The MR# input cannot be bypassed or disabled. The Longdog timer can be bypassed by programming it to the off or idle mode.

The watchdog is the sole hardwired source for driving the IRQ# output low. It can effectively be bypassed by programming it to the off or idle mode. Refer to Figures 1, 2, 3 and 4 for a detailed illustration of the relationships among the affected signals.

The SMS44 also provides the option of the monitors triggering on either an under-voltage or over-voltage condition. The low-order four bits of configuration register 5

7 MSB	**6**	**5**	**4**	**3**	**2**	**1**	**0 LSB**
V_3	V_2	V_1	V_0	V_3	V_2	V_1	V_0
RESET Trigger Source				IRQ Trigger Source			

2047 Table01 1.0

Table 1. Configuration Register 4

program these options.

The high order four bits of configuration register 5 are read only, and their state indicates the sources of interrupts. Whenever an interrupt is generated the status of the V inputs will be recorded in the status register. The status will remain in the register until the device is powered-down

	3 MSB	**2**	**1**	**0 LSB**
	V_3	V_2	V_1	V_0
Writing a 0 enables undervoltage detection for the selected V input	0	0	0	0
Writing a 1 enables overvoltage detection for the selected V input	1	1	1	1

2047 Table02 1.0

Table 2. Configuration Register 5

or another interrupt occurs that overwrites the previous status.

7 MSB	**6**	**5**	**4 LSB**	
V_3	V_2	V_1	V_0	
0	0	0	0	Reading a 1 indicates the source of the interrupt
1	1	1	1	

2047 Table03 1.0

Table 3. Configuration Register 5

If an interrupt occurs and no bits are set the default assumption must be the watchdog generated the interrupt.

WATCHDOG AND LONGDOG TIMERS

The SMS44 contains two timers that can be programmed independently. The Watchdog is intended to be of shorter duration and will generate an interrupt if it times out. The

Longdog timer will generally be programmed to be of longer duration than the watchdog and it will generate a reset if it times out. Both timers are cleared by a low to high transition on WLDI and they both start simultaneously.

If the watchdog should timeout the device status will be recorded in the status register. If the Longdog times out RESET# will drive low either until a WLDI clear is received or until t_{PRTO} (whichever occurs first), at which time it will return high. Refer to Figures 3 and 4 illustrating the action of RESET# and IRQ# with respect to the Watchdog and Longdog timers and the WLDI input.

If WLDI is held low the timers will free-run generating a series of interrupts and resets. If WLDI is held high the interrupt (watchdog) output will be disabled and only the reset (Longdog) output will be active.

7 MSB	6	5	4	3	2	1	0 LSB
SEQ	**RTO1**	**RTO0**	**LD1**	**LD0**	WD2	WD1	WD0
x	x	x	0	0	Longdog Off		
x	x	x	0	1	1600ms		
x	x	x	1	0	3200ms		
x	x	x	1	1	6400ms		
x	0	0	x	x	t_{PRTO} = 25ms		
x	0	1	x	x	t_{PRTO} = 50ms		
x	1	0	x	x	t_{PRTO} = 100ms		
x	1	1	x	x	t_{PRTO} = 200ms		
0	x	x	x	x	Sequence On		
1	x	x	x	x	Sequence Off		

2047 Table04 1.0

Table 4. Configuration Register 6

7 MSB	6	5	4	3	2	1	0 LSB
SEQ	RTO1	RTO0	LD1	LD0	**WD2**	**WD1**	**WD0**
OFF					0	0	0
400ms					0	1	1
800ms					1	0	0
1600ms					1	0	1
3200ms					1	1	0
6400ms					1	1	1

2047 Table05 1.0

Table 5. Configuration Register 6

When the Longdog times out, a reset will be generated. When reset returns high (after t_{PRTO} or after a WLDI strobe) both timers are reset to time zero. Therefore, if the Longdog t_{PLDTO} is equal to or shorter than the watchdog t_{PWDTO}, the reset will effectively clear the interrupt before it can drive the output low.

7 MSB	6	5	4	3	2	1	0 LSB
Address Select		**PUP# State**					
		PUP#3		**PUP#2**		**PUP#1**	
Lock	**AS0**	1	0	1	0	1	0
x	**0**	Device type address 1010, responds only to biased A2 & A1 combinations					
x	**1**	Device type address 1011, responds only to biased A2 & A1 combinations					
0	x	Configuration read/write enabled					
1	x	Configuration read/write locked out					

2047 Table06 1.0

Table 6. Configuration Register 7

Register 6 is also used to set the programmable reset timeout period (t_{PRTO}) and to select the sequence option.

Bit 1	Bit 0	$t_{PDLY}X$
0	0	0ms (no) Delay
0	1	25ms Delay
1	0	50ms Delay
1	1	100ms Delay

2047 Table07 1.0

Table 7. PUP Delays

Sequence Delay Programming

The sequence delays are programmed in register 7. Bit 7 of register 6, must be set to a “0” in order to enable the sequencing of the PUP# outputs. Sequencing will not commence until V_0 is above its programmed threshold.

Each PUP# (-3, -2 and -1) is delayed according to the states of its Bit 1 and Bit 0 as indicated in Table 7.

Refer to Figures 5 and 6 for the detailed timing relationship of the programmable power-on sequencing.

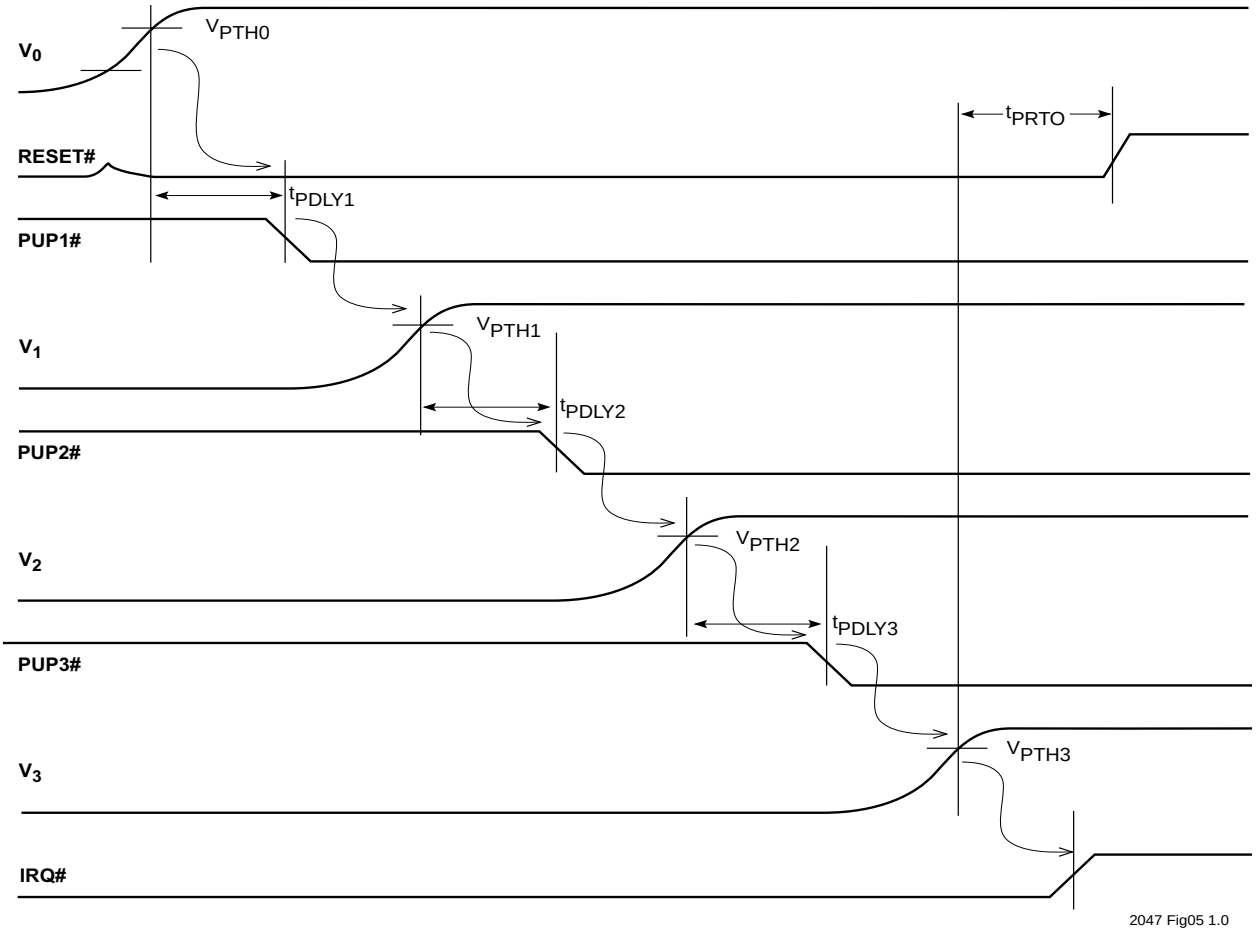
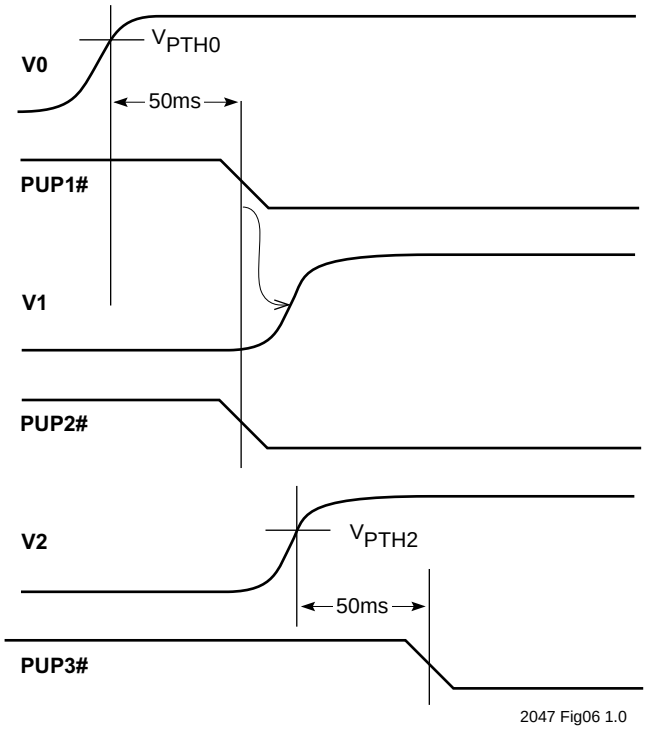


Figure 5. V_x Input and PUP# Sequence



⇦**Figure 6. Timing with Register Contents 22_{HEX}**

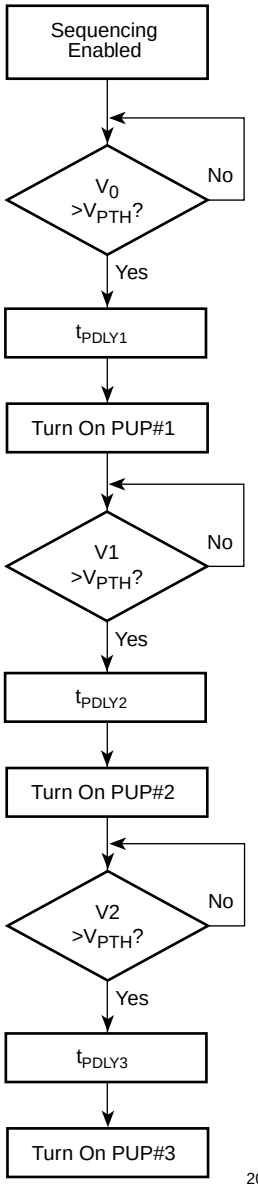


Figure 7. Sequence Flow Chart

The delay from V_{PTH0} until PUP#1 low is t_{PDLY1}. There is a similar $t_{PDLY}X$ delay for V1 to PUP#2 and V2 to PUP#3. They are programmed in register 7. See Figure 5.

Sequencing will always occur as indicated in the flow chart.

MEMORY OPERATION

Data for the configuration registers and the memory array are read and written via an industry standard two-wire interface. The bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are a serial data line (SDA) and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus. See Memory Operating Characteristics: Table 8 and Figure 8.

Input Data Protocol

The protocol defines any device that sends data onto the bus as a "transmitter" and any device that receives data as a "receiver." The device controlling data transmission is called the "master" and the controlled device is called the "slave." In all cases the SMS44 will be a "slave" device, since it never initiates any data transfers.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock high time, because changes on the data line while SCL is high will be interpreted as start or stop condition.

Symbol	Parameter	Conditions	Min.	Max.	Units
f_{SCL}	SCL clock frequency		0	100	kHz
t_{LOW}	Clock low period		4.7		µs
t_{HIGH}	Clock high period		4.0		µs
t_{BUF}	Bus free time	Before new transmission	4.7		µs
$t_{SU:STA}$	Start condition setup time		4.7		µs
$t_{HD:STA}$	Start condition hold time		4.0		µs
$t_{SU:STO}$	Stop condition setup time		4.7		µs
t_{AA}	Clock edge to valid output	SCL low to valid SDA (cycle n)	0.3	3.5	µs
t_{DH}	Data Out hold time	SCL low (cycle n+1) to SDA change	0.3		µs
t_R	SCL and SDA rise time			1000	ns
t_F	SCL and SDA fall time			300	ns
$t_{SU:DAT}$	Data In setup time		250		ns
$t_{HD:DAT}$	Data In hold time		0		ns
TI	Noise filter SCL and SDA	Noise suppression		100	ns
t_{WR}	Write cycle time			5	ms

2047 Table08 2.2

Table 8. Memory Operating Characteristics

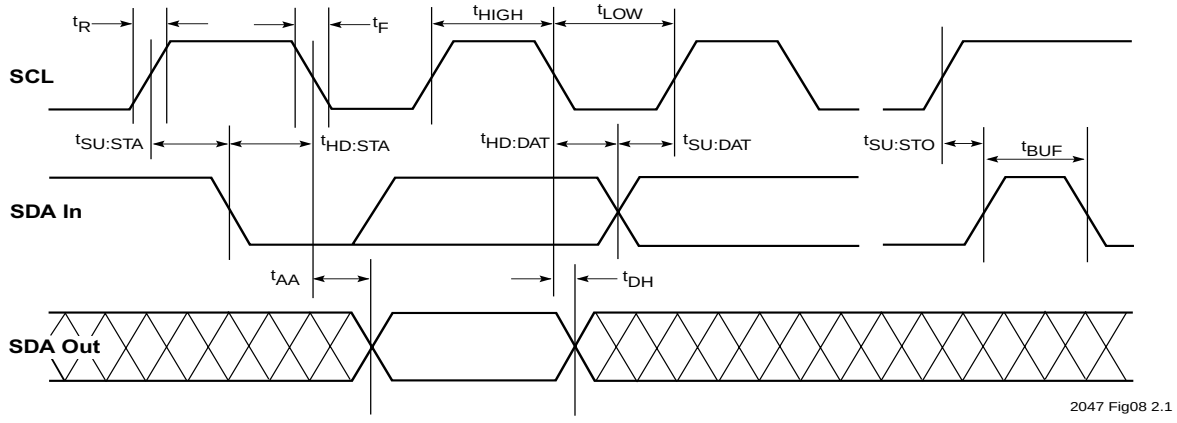


Figure 8. Memory Operating Characteristics

START and STOP Conditions

When both the data and clock lines are HIGH the bus is said to be not busy. A High-to-Low transition on the data line, while the clock is HIGH, is defined as the "START" condition. A Low-to-High transition on the data line, while the clock is HIGH, is defined as the "STOP" condition. See Figure 9.

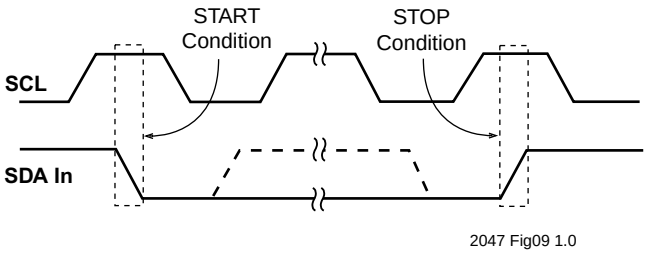


Figure 9. START and STOP Conditions

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line low to ACKnowledge that it received the eight bits of data.

The SMS44 will respond with an ACKnowledge after recognition of a START condition and its slave address byte. If both the device and a write operation are selected the SMS44 will respond with an ACKnowledge after the receipt of each subsequent 8-bit word. In the READ mode the SMS44 transmits eight bits of data, then releases the SDA line, and monitors the line for an ACKnowledge signal. If an ACKnowledge is detected and no STOP condition is generated by the master, the SMS44 will continue to transmit data. If an ACKnowledge is not detected the SMS44 will terminate further data transmissions and awaits a STOP condition before returning to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier/address. For the SMS44 the default is 1010_{BIN}. The next two bits are the Bus Address. The next bit (the 7th) is the MSB of the memory address.

Read/Write Bit

The last bit of the data stream defines the operation to be performed. When set to "1" a read operation is selected; when set to "0" a write operation is selected.

7 MSB	6	5	4	3	2	1	0 LSB
Address Bits							
Device Type				Bus		MSB	R/W
SMS44				x	x	x	x
1	0	0	1	Configuration Register			
1	0	1	0	Memory (default)			
1	0	1	1	Alternate Memory			

2047 Table09 1.0

Table 9. Slave Addresses

WRITE OPERATIONS

The SMS44 allows two types of write operations: byte write and page write. A byte write operation writes a single byte during the nonvolatile write period (t_{WR}). The page write operation, limited to the memory array, allows up to 16 bytes in the same page to be written during t_{WR}.

Byte Write

After the slave address is sent (to identify the slave device and select either a read or write operation), a second byte is transmitted which contains the low order 8 bit address of any one of the 512 words in the array. Upon receipt of the word address the SMS44 responds with an ACKnowledge. After receiving the next byte of data it again responds with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the SMS44 begins the internal write cycle. While the internal write cycle is in progress the SMS44 inputs are disabled and the device will not respond to any requests from the master.

Page Write (memory only)

The SMS44 is capable of a 16-byte page write operation. It is initiated in the same manner as the byte-write operation, but instead of terminating the write cycle after the first data word the master can transmit up to 15 more bytes of data. After the receipt of each byte the SMS44 will respond with an ACKnowledge.

The SMS44 automatically increments the address for subsequent data words. After the receipt of each word, the low order address bits are internally incremented by one.

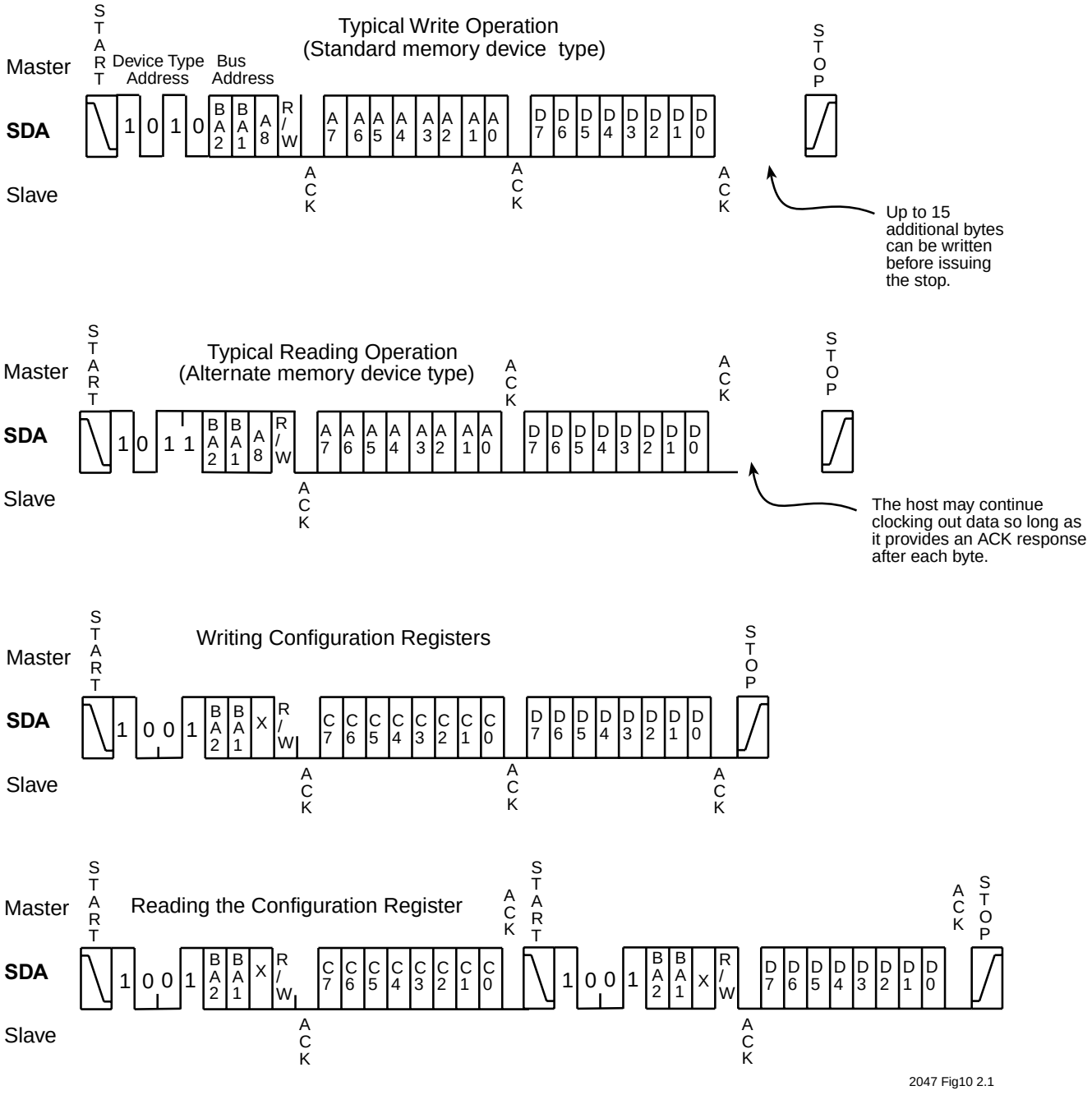


Figure 10. Read and Write Operations

The high order bits of the address byte remain constant. Should the master transmit more than 16 bytes, prior to generating the STOP condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte-write operation, all inputs are disabled during the internal write cycle. Refer to Figure 10 for the address, ACKnowledge, and data transfer sequence.

Acknowledge Polling

When the SMS44 is performing an internal WRITE operation it will ignore any new START conditions. Since the device will only return an acknowledge after it accepts the START the part can be continuously queried until an acknowledge is issued, indicating that the internal WRITE cycle is complete. See the flow diagram for the proper sequence of operations for polling.

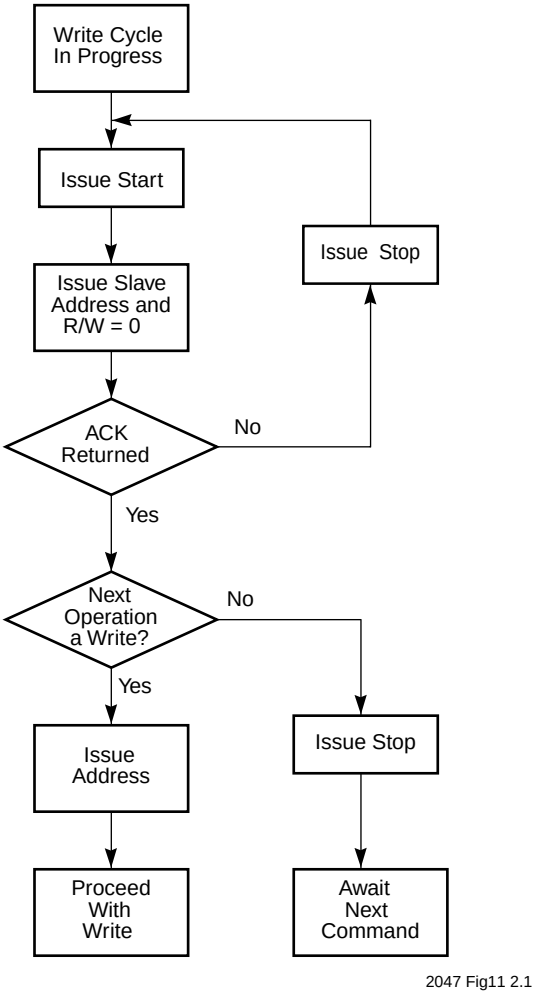


Figure 11. Write Flow Chart

READ OPERATIONS

Read operations are initiated with the R/W bit of the identification field set to "1." T here are two different read options: 1. Current Address Byte Read, and 2. Random Address Byte Read

Current Address Read (memory only)

The SMS44 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a read or write) was to address location n, the next read operation would access data from address location n+1 and increment the current address pointer. When the SMS44 receives the slave address field with the R/W bit set to "1," it issues an acknowledge and transmits the 8-bit word stored at address location n+1. The current address byte read operation only accesses a single byte of data. The master does not acknowledge the transfer, but does generate a stop condition. At this point, the SMS44 discontinues data transmission.

Random Address Read (Register and Memory)

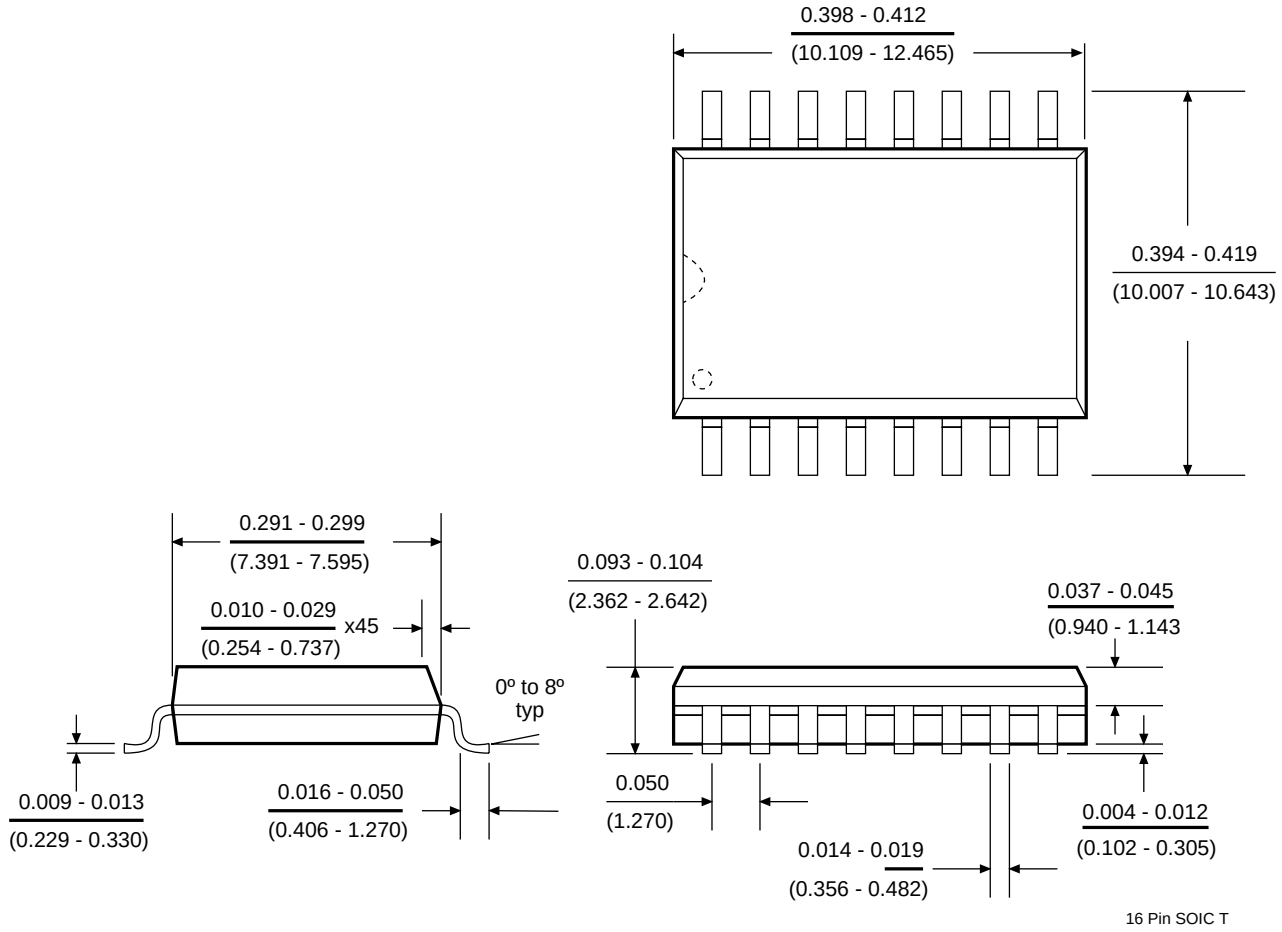
Random address read operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with the R/W bit set to WRITE), followed by the address of the word it is to read. This procedure sets the internal address counter of the SMS44 to the desired address. After the word address acknowledge is received by the master it immediately reissues a start condition, followed by another slave address field with the R/W bit set to READ. The SMS44 will respond with an acknowledge and then transmit the 8 data bits stored at the addressed location. At this point the master does not acknowledge the transmission but does generate the stop condition. The SMS44 discontinues data transmission and reverts to its standby power mode.

Sequential READ (Memory Only)

Sequential reads can be initiated as either a current address READ or random access READ. The first word is transmitted as with the other byte read modes (current address byte READ or random address byte READ); however, the master now responds with an ACKnowledge, indicating that it requires additional data from the SMS44. The SMS44 continues to output data for each ACKnowledge received. The master terminates the sequential READ operation by not responding with an ACKnowledge, and issues a stop condition. During a sequential read operation the internal address counter is automatically incremented with each ACKnowledge signal. For read operations all address bits are incremented, allowing the entire array to be read using a single read command. After a count of the last memory address the address counter will 'roll-over' and the memory will continue to output data.

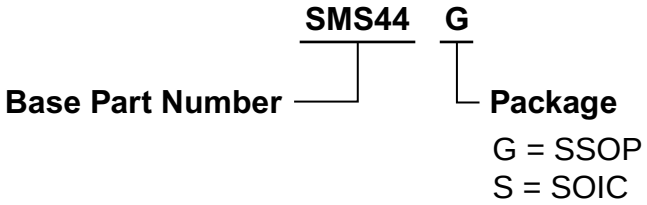
PACKAGES

16 PIN SOIC PACKAGE



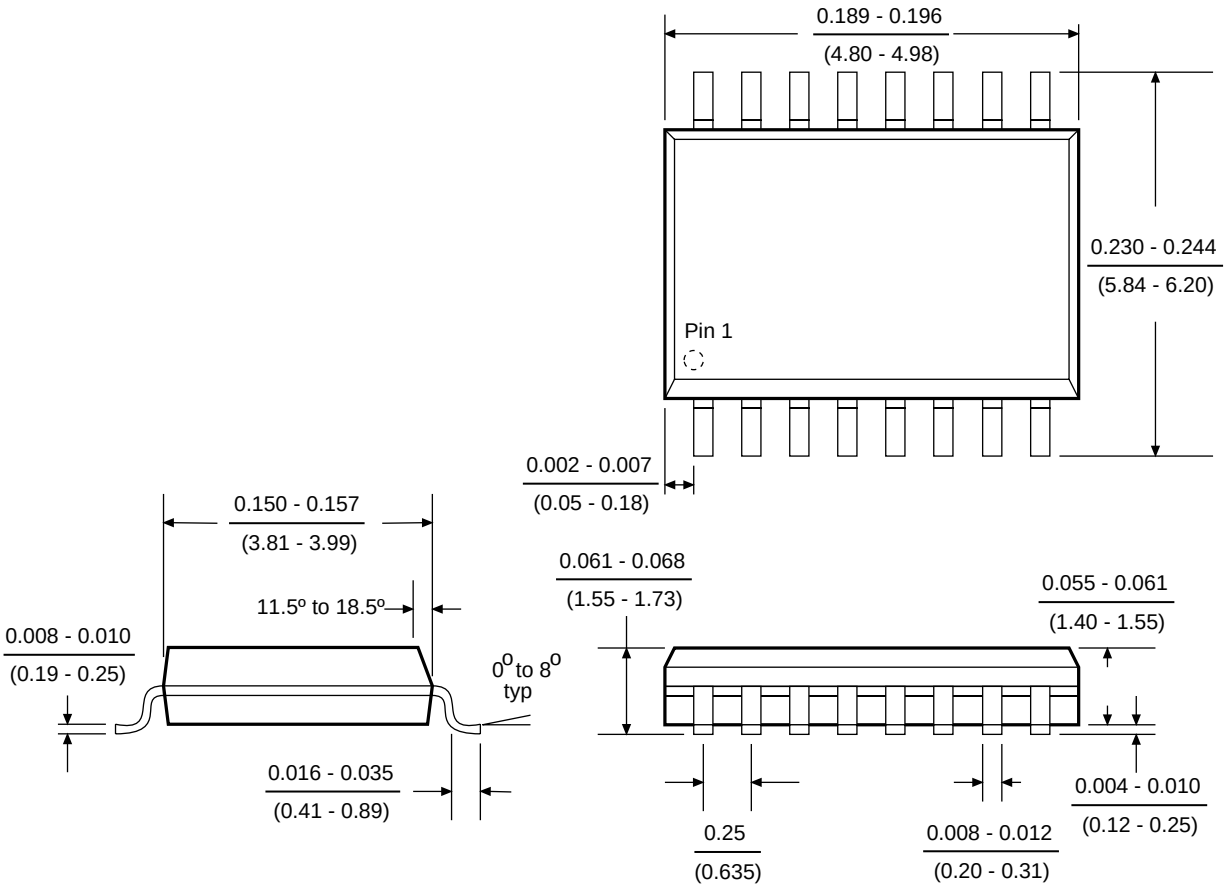
16 Pin SOIC T

ORDERING INFORMATION



2047 Tree 1.0

16 PIN SSOP PACKAGE



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