Product List

SM89T16R1L16, 16MHz 64KB internal flash MCU
SM89T16R1C25, 25MHz 64KB internal flash MCU

General Description

The SM89T16R1 is a high speed (4 clocks / machine cycle) single-chip 8-bits microcontroller manufactured in an advanced CMOS process with on chip flash memory. It supports a derivative of the 80C51 microcontroller family. The SM89T16R1 has the same instructions set as the 80C51.

The SM89T16R1 contains a 64KB on chip program flash, a volatile 1280 x 8 bits data RAM, four 8-bits I/O ports, one 4-bits I/O port, two 16-bits timer/event counters, and an additional 16-bits timer coupled to capture and compare latches, a two-priority-level, nested interrupt structure, two pulse-width- modulation outputs, two UART and two DPTR, an on-chip oscillator and timing circuit. For system that requires extra capability the SM89T16R1 can be expanded using standard TTL compatible memory and logic.

In addition, The SM89T16R1 has two software selectable modes of power saving – IDLE mode and POWER-DOWN mode. The IDLE mode freezes the CPU while allowing the RAM, timer, serial ports, and interrupt system to continue functioning. The POWER-DOWN mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

The Power Management Mode (PMM) is useful for portable or battery-powered applications. This feature allows software to select a lower speed clock as the main time base.

Feature

- Working Voltage: 3.3V or 5.0V.
- 80C51 Central Processor Unit (CPU), High-Speed Architecture (4 clocks / machine cycle), the maximum clock rate is 25 MHz.
- 64K x 8 on chip flash memory can be programmed at V_{PP} = 12V
- 1280 x 8 RAM (On-Chip 256 bytes and Expand 1024 bytes), expandable externally to 64KB
- Two standard 16-bits timers/counters
- An additional 16-bits timer/counter coupled to a capture and compare register.
- Two 8-bits / 5-bits resolution Pulse-Width-Modulation (PWM) outputs.
- Four channels 6 bits Analog to Digital Converter (ADC).
- Four 8-bits I/O ports.(For PDIP package)
- Four 8-bits I/O ports plus one 4-bits I/O port. (For PLCC or PQFP package)
- Two Full-duplex Enhance UART
- Two DPTR (either data pointer can be incremented and decrement).
- 13 interrupt sources (default 6 + int2, int3, int4, int5, UART1, ADC, RTC) with 2 priority levels.
- RTC (Real Time Clock) function.
- Extended temperature range (-40℃ to +85℃)
- Software enable/disable ALE output pulse
- Wake-up from POWER-DOWN mode by external interrupt, RTCI or H/W Reset.

Ordering Information

SM89T16R1ihhk
yymmv

i: process identifier {L=3.0V~3.6V,C=4.5V~ 5.5V}
hh: working clock in MHz {16,25}
k: package type postfix {as below table}
yy: year mm: month
v: version identifier { , A, B, ...}

Taiwan
4F, No. 1 Creation Road 1,
Science-based Industrial Park,
Hsinchu, Taiwan 30077

TEL: 886-3-578-3344 #2667
886-3-579-2987
FAX: 886-3-5792960
886-3-5780493

Package Spec.

Package	Pin / PAD	Frequency
44L PQFP	Figure 1	16 MHz at 3.3V and 25MHz at 5V
44L PLCC	Figure 2	16 MHz at 3.3V and 25MHz at 5V
40L PDIP	Figure 3	16 MHz at 3.3V and 25MHz at 5V

Pin Configuration

Figure 1 44L PQFP Package

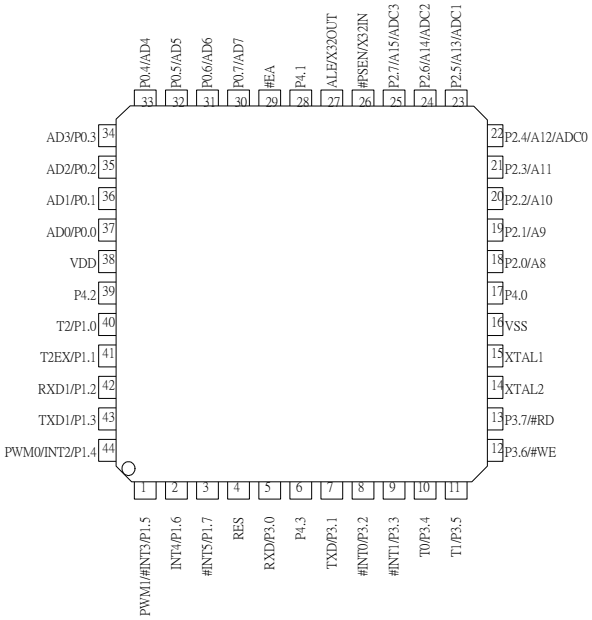


Figure 2 44L PLCC Package

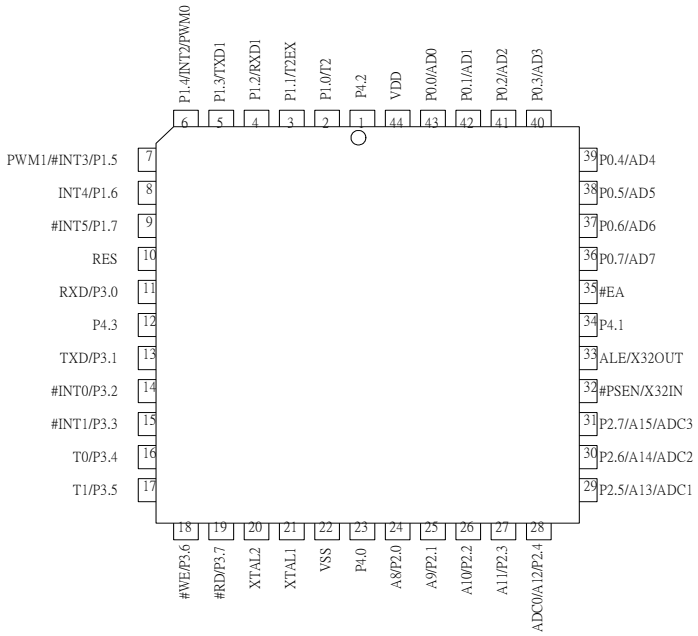
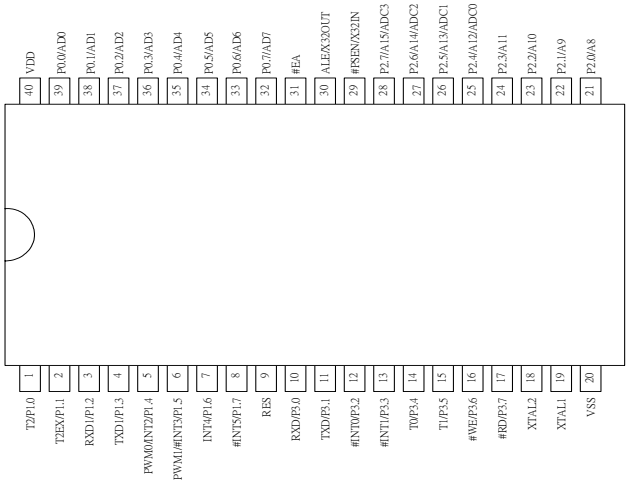
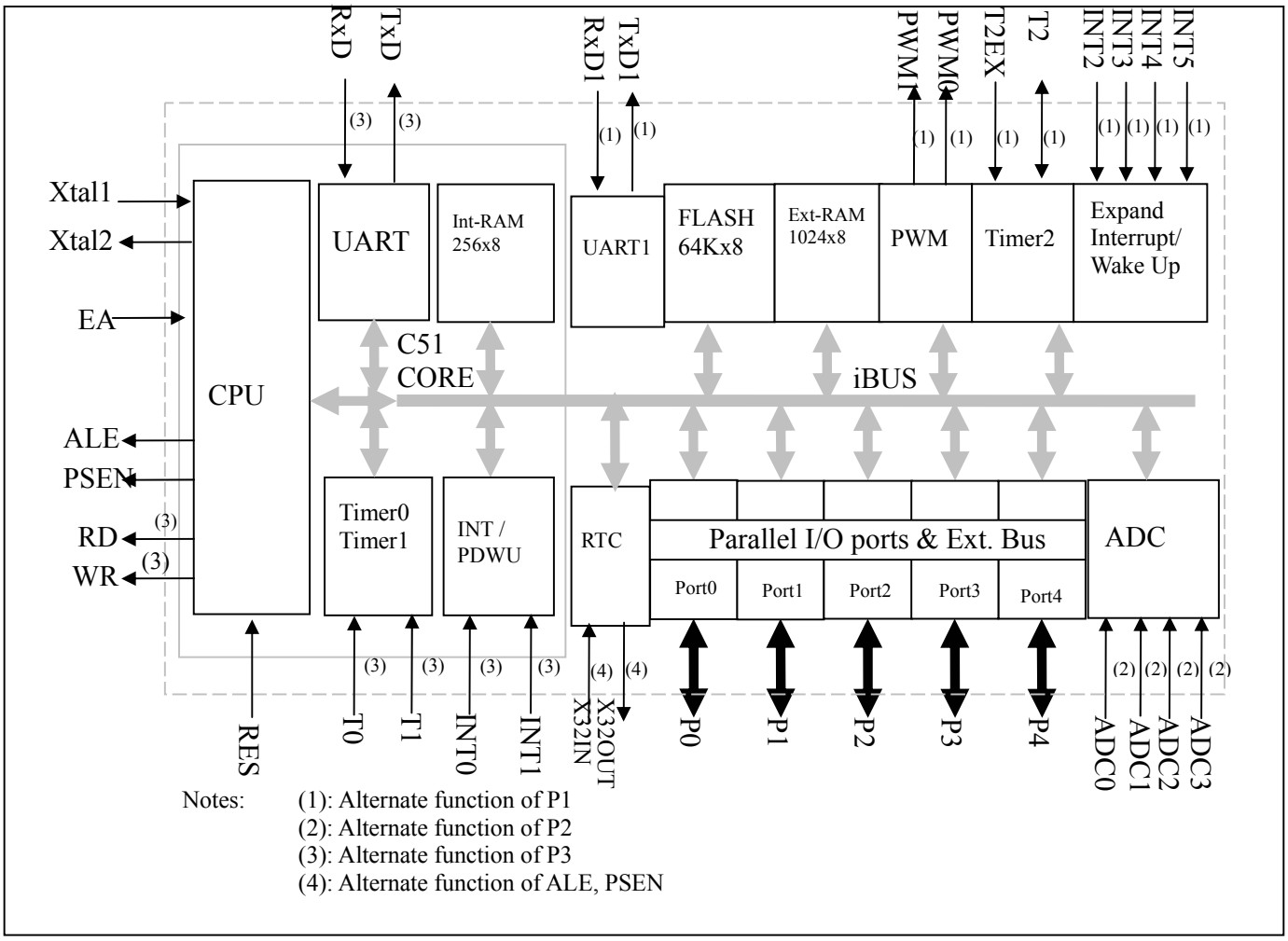


Figure 3 40L PDIP Package



Block Diagram



Notes:
(1): Alternate function of P1
(2): Alternate function of P2
(3): Alternate function of P3
(4): Alternate function of ALE, PSEN

Pin Description

MNEMONIC	DIP 40 pin	PQFP 44 Pin	PLCC 44 pin	Names and Functions
VDD	40	38	44	**Power supply**: +3.3V and +5V power supply pin during normal operations and power saving modes.
P0.0 – P0.7	39,38,37,36 35,34,33,32	37,36,35,34 33,32,31,30	43,42,41,40 39,38,37,36	**Port 0**: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them become floating and can be used as high- impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port Pin Alternative function P0.0 AD0 P0.1 AD1 P0.2 AD2 P0.3 AD3 P0.4 AD4 P0.5 AD5 P0.6 AD6 P0.7 AD7
P1.0 – P1.7	1,2,3,4, 5,6,7,8	40,41,42,43, 44,1,2,3	2,3,4,5, 6,7,8,9	**Port 1:** An 8-bits bidirectional I/O port with internal pull-ups on all pins. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: IIL). Alternate function of SM89T16R1 include: Port Pin Alternative function P1.0 T2: TIMER2 clock output P1.1 T2EX: TIMER2 reload/capture DIR. P1.2 RxD1: UART1 input P1.3 TxD1: UART1 output P1.4 PWM0: PWM channel 0 output INT2: rising edge trigger P1.5 PWM1: PWM channel 1 output #INT3: falling edge trigger P1.6 INT4: rising edge trigger P1.7 #INT5: falling edge trigger
RST	9	4	10	**Reset**: A high on this pin for two machine cycles while the oscillator is running resets the device. An internal resistor to VSS permits a power-on reset using only an external capacitor to VCC.
P2.0 – P2.7	21,22,23,24, 25,26,27,28	18,19,20,21 22,23,24,25	24,25,26,27, 28,29,30,31	**Port 2:** Port 2 is an 8-bits bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: IIL). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that uses 16-bits addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that uses 8-bits addresses (MOV @Ri), port 2 emits the contents of the P2 special function register. Port Pin Alternative function P2.0 A8 P2.1 A9 P2.2 A10 P2.3 A11 P2.4 A12/ADC0 P2.5 A13/ADC1 P2.6 A14/ADC2 P2.7 A15/ADC3

MNEMONIC	DIP 40 pin	PQFP 44 Pin	PLCC 44 pin	Names and Functions
P3.0 – P3.7	10,11,12,13 14,15,16,17	5,7,8,9, 10,11,12,13	11, 13,14,15, 16,17,18,19	**Port 3**: Port 3 is an 8-bits bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: IIL). Port 3 also serves the special features. Port Pin Alternative function P3.0 RxD UART input P3.1 TxD UART output P3.2 #EX0 external interrupt 0 P3.3 #EX1 external interrupt 1 P3.4 T0: Timer 0 external input P3.5 T1: Timer 1 external input P3.6 #WR External data memory write strobe P3.7 #RD External data memory read strobe
ALE/X32OUT	30	27	33	**Address Latch Enable**: Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted twice every machine cycle, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. Setting SFR SCONF.0 can disable ALE. With this bit set, ALE will be active only during a MOVX instruction. X32OUT: The 32.768KHz crystal output for RTC function.
#PSEN/X32IN	29	26	32	**Program Store Enable:** The read strobe to external program memory. When executing code from the external program memory, #PSEN is activated twice each machine cycle, except that two #PSEN activations are skipped during each access to external data memory. #PSEN is not activated during fetches from internal program memory. X32IN: The 32.768KHz crystal input for RTC function.
#EA	31	29	35	**External Access Enable**: #EA must be externally held low to enable the device to fetch code from external program memory locations. If #EA is held high, the device executes from internal program memory.
XTAL1	19	15	21	**Crystal 1**: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	14	20	**Crystal 2**: Output from the inverting oscillator amplifier.

SFR Mapping

The special function register of SM89T16R1 fall into the following categories

- C51 CORE register: ACC, B, DPL, DPH, PSW, SP
- I/O ports: P0,P1, P2, P3, P4
- Timer/Counter register: T2CON, T2MOD, TCON, TMOD, TH0, TH1, TH2, TL0, TL1, TL2, RCA2PL, RCAP2H
- The Second DPTR register: DPS, DPH1, DPL1
- UART I/O register: SBUF, SCON
- UART1 I/O register: SBUF1, SCON1
- ADC register: ADCSC, ADCD, P2CON
- Power and system control register: PCON, SCONF
- Interrupt system register: IP, IE, IP1, IE1, IFR
- Expand External Interrupt register: EIE, EIP, EXIF
- RTC register: RTCC, RTCS
- PWM output register: PWMC0, PWMC1, PWMD0, PWMD1, P1CON
- PMM (Power Management) register: PMR

Table 1 SFR Map

$F8	**SCON1** 0000 0000	**SBUF1** xxxx xxxx							$FF
$F0	B 0000 0000								$F7
$E8		**SADEN** 0000 0000	**SADEN1** 0000 0000						$EF
$E0	ACC 0000 0000								$E7
$D8	**P4** **xxxx 1111**	**SADDR** 0000 0000	**SADDR1** 0000 0000						$DF
$D0	PSW 0000 0000	**PMR** 01xx 0000		**PWMC0** 0000 0000	**PWMC1** 0000 0000				$D7
$C8	T2CON 0000 0000	**T2MOD** 0000 0000	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			$CF
$C0									$C7
$B8	IP x000 0000	**IP1** 0000 0000	**EIP** xxxx 0000					**SCONF** 0000 0000	$BF
$B0	P3 1111 1111			**PWMD0** 0000 0000	**PWMD1** 0000 0000				$B7
$A8	IE 0000 0000	**IE1** 0000 0000	**IFR** 0000 0000	**EIE** 0000 0000					$AF
$A0	P2 1111 1111	**RTCS** 0000 0000	**RTCC** 0000 0000	**CKCON** 0000 0001	**DPL1** 0000 0000	**DPH1** 0000 0000	**DPS** 0000 0000		$A7
$98	SCON 0000 0000	SBUF xxxx xxxx		**P1CON** 0000 0000	**P2CON** 0000 0000				$9F
$90	P1 1111 1111	**EXIF** 0000 1xxx	**LEDP0** 0000 0000	**LEDP1** 0000 0000	**LEDP2** 0000 0000	**LEDP3** 0000 0000	**LEDP4** 0000 0000		$97
$88	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	**ADCSC** 0000 0000	**ADCD** 0000 0000	$8F
$80	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00xx 0000	$87

Table 2 All SFR list (ADC, RTC, PWM, LED Driving Capability Control)

Symbol	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
A/D Converter											
ADCSC	ADC status & control	8EH	COM	CON	ADCSS1	ADCSS0	CH1	CH0			00H
ADCD	ADC data register	8FH	AD.5	AD.4	AD.3	AD.2	AD.1	AD.0			00H
Real Timer Clock (RTC)											
RTCS	RTC Status	A1H	RTCen	Stable	Sec.5	Sec.4	Sec.3	Sec.2	Sec.1	Sec.0	00H
RTCC	RTC Control	A2H	Int_sel.1	Int_sel.0	Min.5	Min.4	Min.3	Min.2	Min.1	Min.0	00H
PWM output											
PWMC0	PWM 0 Control	D3H						PBS	PFS1	PFS0	00H
PWMC1	PWM 1 Control	D4H						PBS	PFS1	PFS0	00H
PWMD0	PWM 0 Data	B3H	PWMD.7	PWMD.6	PWMD.5	PWMD.4	PWMD.3	PWMD.2	PWMD.1	PWMD.0	00H
PWMD1	PWM 1 Data	B4H	PWMD.7	PWMD.6	PWMD.5	PWMD.4	PWMD.3	PWMD.2	PWMD.1	PWMD.0	00H
LED Driving Capability Control											
LEDP 0	LED output in P0	92H									00H
LEDP 1	LED output in P1	93H									00H
LEDP 2	LED output in P2	94H									00H
LEDP 3	LED output in P3	95H									00H
LEDP 4	LED output in P4	96H									00H

Table 3 : All SFR list (8051, I/O, Timer, UART/UART1, System, Interrupt)

Symbol	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
8051 Core											
ACC*	Accumulator	E0									00H
B	B register	F0									00H
SP	Stack Pointer	81H									07H
PSW*	Process Status	D0H	CY	AC	F0	RS1	RS0	OV		P	00H
DPTR	Data Pointer (2 Bytes)										
DPH	Data Pointer High	83H									00H
DPL	Data Pointer Low	82H									00H
I/O PORT											
P0*	Port 0	80H	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	FFH
P1*	Port 1	90H	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	FFH
P2*	Port 2	A0H	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	FFH
P3*	Port 3	B0H	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	FFH
P4*	Port 4	D8H					P4.3	P4.2	P4.1	P4.0	XFH
P1CON	P1 Control	9BH			PWM1E	PWM0E			-	-	00H
P2CON	P2 Control	9CH	ADCE3	ADCE2	ADCE1	ADCE0					00H
TIMER / Counter											
TCON*	Timer Control register	88H	TF1	TF1	TF0	TR0	IE1	IT1	IE0	IT0	00H
THL0	Timer 0 (2 Bytes)										
TH0	Timer 0 High	8CH									00H
TL0	Timer 0 Low	8AH									00H
THL1	Timer 1 (2 Bytes)										
TH1	Timer 1 High	8DH									00H
TL1	Timer 1 Low	8BH									00H
T2CON*	Timer 2 Control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CT2	CPRL2	00H
T2MOD	Timer 2 Mode Control	C9H	HC5	HC4	HC3	HC2	T2CR		T2OE	DCEN	00H
RCAP2HL	Reload/Capture (2 bytes)										
RCAP2H	RCAP2 High	CBH									00H
RCAP2L	RCAP2 Low	CAH									00H
THL2	Time 2 (2 bytes)										
TH2	Timer 2 High	CDH									00H
TL2	Time 2 Low	CCH									00H
UART & UART1											
SCON*	UART Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00H
SBUF	UART Buffer	99H									XXH
SCON1	UART 1 Control	F8H	SM0_1/FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	00H
SBUF1	UART 1 Buffer	F9H									XXH
SADDR	Slave Address	D9H									00H
SADDR1	Slave Address 1	DAH									00H
SADEN	Slave Address Mask Enable	E9H									00H
SADEN1	Slave Address 1 Mask Enable	EAH									00H
Data Point 1											
DPTR1	Data Pointer 1 (2 Bytes)										
DPH1	Data Pointer 1 High	A5H									00H
DPL1	Data Pointer 1 Low	A4H									00H
DPS	Data Point Select	A6H								DPS.0	00H
Power and System											
PCON	Power Control register	87H	SMOD	SMOD0					PD	IDLE	00H
SCONF	System Control	BFH	SMOD1			PDWUE			OME	ALEI	00H
PMR	Power Management Register	D1H	CD1	CD0			XTOFF				40H
Interrupt system											
IE*	Interrupt Enable	A8H	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	00H
IE1	Interrupt Enable 1	A9H					EADC	ERTC			00H
IFR	Interrupt Flag 1	AAH					ADCIF	RTCIF			00H
EIE	External Interrupt Enable	ABH					EX5	EX4	EX3	EX2	00H
IP*	Interrupt Priority	B8H		PS1	PT2	PS0	PT1	PX1	PT0	PX0	00H
IP1	Interrupt Priority 1	B9H					PADC	PRTC			00H
EIP	External Interrupt Priority	BAH					PX5	PX4	PX3	PX2	X0H
Clock Control											
CKCON	Clock Control	8EH			T2M	T1M	T0M	MD2	MD1	MD0	01H

Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit.	Remarks
TA	Operating temperature	-40	25	85	℃	Ambient temperature under bias
TS	Storage temperature	-55	25	155	℃	Damage to devices could occur
VCC33	Supply voltage	3.0	3.3	3.6	V	
VCC5	Supply voltage	4.5	5.0	5.5	V	
Fosc 16	Oscillator Frequency			16	MHz	For 3.3V application
Fosc 25	Oscillator Frequency			25	MHz	For 5.0V application

DC Characteristic

V_{CC} = 5V (±10%), V_{SS}=0V T_A= -40℃ to 85℃

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	Supply Voltage		4.5	5.5	V
I_{CC}	Supply current operating	See notes 1 f_{CLK} = 12MHz V_{CC} = 5.0V		30	mA
I_{ID}	Supply current IDLE Mode	See note 2 f_{CLK} = 12MHz V_{CC} = 5.0V		15	mA
I_{PD}	Supply current Power-Down MODE RTC Disable	See note 3；V_{CC} = 5.5V		30	μA
	Supply current Power-Down MODE RTC Enable	See note 3；V_{CC} = 5.5V		100	uA
INPUT					
V_{IL1}	Input LOW voltage, P0, P1, P2, P3, P4, /EA		-0.5	0.8	V
V_{IL2}	Input LOW voltage, RES, XTAL1		0	0.8	V
V_{IH1}	Input HIGH voltage, P0, P1, P2, P3, P4, /EA		2.0	Vcc+0.5	V
V_{IH2}	Input HIGH voltage, RES, XTAL1		70%VCC	Vcc+0.5	V
I_{IL}	Input current LOW level Port 1,2,3,4	VIN = 0.45V		-75	μA
I_{TL}	Transition current High to Low Port 1,2,3,4	VIN = 2.0 V		-650	μA
I_{LI}	Input leakage current	0.45V < VIN < VCC-0.3V		±10	μA
OUTPUT					
V_{OL1}	Output LOW voltage, Port 0,ALE, /PSEN	IOL = 3.2mA，VCC=5.0V		0.45	V
V_{OL2}	Output LOW voltage, Port 1, 2, 3, 4	IOL = 1.6mA，VCC =5.0V		0.45	V
V_{OH1}	Output High voltage Port0 ALE, /PSEN	IOH = -800uA，VCC =5.0V	2.4		V
V_{OH1}	Output High voltage Port 1,2,3,4	IOH = -60μA，VCC =5.0V	2.4		V
R_{RST}	Internal RESET pull-down resistor		50	300	kΩ
C_{IO}	Pin capacitance	Test freq=1MHz, TA=25℃		10	pF

V_{CC} = 3.3V (±10%), V_{SS}=0V , T_A=-40℃ to 85℃

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	Supply Voltage		3.0	3.6	V
I_{CC}	Supply current operating	See notes 1 f_{CLK} = 12MHz V_{CC} = 3.6V		20	mA
I_{ID}	Supply current IDLE Mode	See note 2 f_{CLK} = 12MHz V_{CC} = 3.6V		10	mA
I_{PD}	Supply current Power-Down MODE RTC Disable	See note 3；V_{CC} = 3.6V		20	μA
	Supply current Power-Down MODE RTC Enable	See note 3；V_{CC} = 3.6V		30	μA
INPUT					
V_{IL1}	Input LOW voltage, P0, P1, P2, P3, P4, /EA	VCC = 3.6V	0	0.2 VCC -0.2	V
V_{IL2}	Input LOW voltage, RST,XTAL1	VCC = 3.6V	0	0.2 VCC -0.2	V
VIH1	Input HIGH voltage, P0, P1, P2, P3, P4, /EA	VCC = 3.6V	0	0.2 VCC -0.2	V
VIH2	Input HIGH voltage, RST	VCC = 3.6V	0.6 VCC	VCC + 0.2	V

			-0.4		
VIH3	Input HIGH voltage, XTAL1	VCC = 3.6V	0.6 VCC -0.4	VCC + 0.2	V
IIN1	Input current LOW level Port 1,2,3,4	VCC = 3.0V ~3.6V, VIN = 0.45V.	-10	50	μA
ITL	Transition current High to Low Port 1,2,3,4	See note 4 VCC = 3.6V, VIN = 1.2 V	-75	400	μA
ILI	Input leakage current P0, /EA	VCC = 3.0V ~3.6V, 0.45V<VIN<VCC	-10	10	μA
OUTPUT					
V_{OL1}	Output Low voltage, Port 0,ALE, /PSEN	I_{OL} = 7mA，V_{CC} =3.3V		0.4	V
V_{OL2}	Output Low voltage Port 1,2,3,4	I_{OL} = 7mA，V_{CC} =3.3V		0.4	V
V_{OH1}	Output High voltage Port0, ALE, /PSEN	IOH =-300uA，VCC =3.3V	2.4		V
V_{OH2}	Output High voltage Port 1,2,3,4	IOH =-20μA，VCC =3.3V	2.4		V
I_{SK1}	Sink Current Port 1, 2, 3, 4	VCC = 3.3V, VIN = 0.4 V		6	mA
I_{SK2}	Sink Current Port 0,ALE, /PSEN	VCC = 3.3V, VIN = 0.4 V		8	mA
I_{SR1}	Source Current Port 1, 2, 3, 4	VCC = 3.3V, VIN = 2.4 V		-80	uA
I_{SR2}	Source Current Port 0,ALE, /PSEN	VCC = 3.3V, VIN = 2.4 V		-8	mA
R_{RST}	Internal RESET pull-down resistor		50	300	kΩ
C_{IO}	Pin capacitance	Test freq=1MHz, TA=25℃		10	pF

NOTES FOR DC ELECTRICAL CHARACTERISTICS

1. The operating supply current is measured with all output disconnected; XTAL1 driven with $t_r = t_f = 5ns$; $V_{IL} = V_{SS}+0.5V$; $V_{IH}=V_{CC}-0.5V$; XTAL2 not connect;/EA=RST=Port0=V_{CC}.
2. The IDLE MODE supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f = 5ns$; $V_{IL} = V_{SS}+0.5V$; $V_{IH}=V_{CC}-0.5V$; XTAL2 not connect;/EA= Port0=V_{CC}.
3. The POWER-DOWN MODE supply current is measured with all output pins disconnected; VIL = $V_{SS}+0.5V$; $V_{IH}=V_{CC}-0.5V$; XTAL2 not connect; /EA= Port0=V_{CC}.
4. Port 1, 2, 3, and 4 sources a transition current when they are being externally driven from HIGH to LOW. The transition current reaches its maximum value when V_{IN} is approximately 2V.
5. Capacities loading on port 0 and 2 may cause spurious noise to be superimposed on V_{OL} of ALE and port 1, 3, and 4. The noise is due to external bus capacitance discharging into port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacities loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt trigger STROBE input.

AC Characteristic

V_{CC}=3.3V±10%, V_{SS}=0V, t_{clk} min = 1/ f_{max}(maximum operating frequency)
T_A=-40℃ to +85℃
C_L=100pF for Port0, ALE and /PSEN; C_L=80pF for all other outputs unless otherwise specified.

Symbol	FIGURE	PARAMETER	MIN	MAX	UNIT
External Clock drive into XTAL1					
t_{CLCL}	4	Xtal1 Period	62.5 (1)	-	ns
t_{CHCX}	4	Xtal1 HIGH time	31	-	ns
t_{CLCX}	4	Xtal1 LOW time	31	-	ns
t_{CLCH}	4	XTAL1 rise time	-	15	ns
t_{CHCL}	4	XTAL1 fall time	-	15	ns
t_{CYC}	4	Controller cycle time = t_{CLCL} / 4	5.2	-	ns

NOTES:

1. Operating at 25MHz.

Symbol	FIGURE	PARAMETER	MIN	MAX	UNIT
Program Memory					
$1/t_{CLCL}$	7	System clock frequency	3.0	16	MHz
t_{LHLL}	7	ALE pulse width	1.5 t_{CLCL} -5		ns
t_{AVLL}	7	Address valid to ALE low	0.5 t_{CLCL} -5		ns
t_{LLAX}	7	Address hold after ALE low	0.5 t_{CLCL} -5		ns
t_{LLAX}	8	Address hold after ALE low for MOVX Write	0.5 t_{CLCL} -5		ns
t_{LLIV}	7	ALE LOW to valid instruction in		2.5t_{CLCL}-20	ns
t_{LLPL}	7	ALE LOW to /PSEN LOW	0.5 t_{CLCL} -5		ns
t_{PLPH}	7	/PSEN pulse width	2.0 t_{CLCL} -5		ns
t_{PLIV}	7	/PSEN LOW to valid instruction in		2.0t_{CLCL}-20	ns
t_{PXIX}	7	Input instruction hold after /PSEN	0		ns
t_{PXIZ}	7	Input instruction float after /PSEN		t_{CLCL} -5	ns
t_{AVIV1}	7	Port 0 Address to valid instruction in		3.0t_{CLCL}-20	ns
t_{AVIV2}	7	Port 2 Address to valid instruction in		3.5t_{CLCL}-20	ns
t_{PLAZ}	7	/PSEN low to address float	0		ns

MOVX Characteristics Using Stretch Memory Cycles

Symbol	FIGURE	PARAMETER	MIN	MAX	UNIT	Stretch
t_{LHLL2}	8	ALE pulse width	1.5 t_{CLCL} –5 2.0 t_{CLCL} -5		ns	t_{MCS} =0 t_{MCS} >0
t_{LLAX2}	9	Address hold after ALE low for MOVX Write	0.5 t_{CLCL} -5		ns	
t_{RLRH}	8	/RD pulse width	2.0 t_{CLCL} –5 t_{MCS} -10		ns	t_{MCS} =0 t_{MCS} >0
t_{WLWH}	9	/WR pulse width	2.0 t_{CLCL} –5 t_{MCS} -10		ns	t_{MCS} =0 t_{MCS} >0
t_{RLDV}	8	/RD LOW to valid data in		2.0 t_{CLCL} –20 t_{MCS} -20	ns	t_{MCS} =0 t_{MCS} >0
t_{RHDX}	8	Data hold after /RD	0		ns	
t_{RHDZ}	8	Data float after /RD		t_{CLCL} –5 2.0 t_{CLCL} –5	ns	t_{MCS} =0 t_{MCS} >0
t_{LLDV}	8	ALE LOW to valid data in		2.5 t_{CLCL} –5 t_{MCS}+2.0t_{CLCL} –40	ns	t_{MCS} =0 t_{MCS} >0
t_{AVIV1}	8	Port 0 Address to valid instruction in		3.0 t_{CLCL}-20 2.0 t_{CLCL} –5	ns	t_{MCS} =0 t_{MCS} >0
t_{AVIV2}	7,8	Port 2 Address to valid instruction in		3.5 t_{CLCL}-20 2.5 t_{CLCL} –5	ns	t_{MCS} =0 t_{MCS} >0
t_{LLWL}	8,9	ALE LOW to /RD or /WR LOW	0.5 t_{CLCL}–5 1.5 t_{CLCL}–5	0.5 t_{CLCL}+5 1.5 t_{CLCL}+5	ns	t_{MCS} =0 t_{MCS} >0
t_{AVWL1}	8,9	Port0 Address valid to /WR or /RD LOW	t_{CLCL}–5 2.0 t_{CLCL}–5		ns	t_{MCS} =0 t_{MCS} >0

t_{AVDV2}	9	Port2 Address valid to /WR or /RD LOW	$1.5t_{CLCL}-5$ $2.5\ t_{CLCL}-5$		ns	$t_{MCS}=0$ $t_{MCS}>0$
t_{QVWX}	9	Data valid to /WR transition	-5 $1.0\ t_{CLCL}$ -5		ns	$t_{MCS}=0$ $t_{MCS}>0$
t_{WHQX}	9	Data hold after /WR	$1.0\ t_{CLCL}$ -5 $2.0\ t_{CLCL}$ -5		ns	$t_{MCS}=0$ $t_{MCS}>0$
t_{RLAZ}	8	/RD LOW to address float		$0.5\ t_{CLCL}-5$	ns	
t_{WHLH}	8,9	/RD or /WR HIGH to ALE HIGH	0 $1.0\ t_{CLCL}$ -5	10 $1.0\ t_{CLCL}$ +5	ns	$t_{MCS}=0$ $t_{MCS}>0$

Notes:
t_{MCS} is time period related to the Stretch memory cycle selection. The following table shows the value of t_{MCS} for each Stretch selection.

M2	M1	M0	MOVX Cycles	t_{MCS}
0	0	0	2 machine cycles	0
0	0	1	3 machine cycles	$4\ t_{CLCL}$
0	1	0	4 machine cycles	$8\ t_{CLCL}$
0	1	1	5 machine cycles	$12\ t_{CLCL}$
1	0	0	6 machine cycles	$16\ t_{CLCL}$
1	0	1	7 machine cycles	$20\ t_{CLCL}$
1	1	0	8 machine cycles	$24\ t_{CLCL}$
1	1	1	9 machine cycles	$28\ t_{CLCL}$

Parameter	Figure	Symbol	Min	Typ	Max	Unit
Serial Port Clock Cycle Time SM2=0,12 clocks per cycle SM2=1,4 clocks per cycles	10	t_{XLXL}		$12\ t_{CLCL}$ $4\ t_{CLCL}$		ns ns
Output Data Setup to Clock Rising SM2=0,12 clocks per cycle SM2=1,4 clocks per cycles	10	t_{QVXH}		$12\ t_{CLCL}$ $4\ t_{CLCL}$		ns ns
Output Data Hold to Clock Rising SM2=0,12 clocks per cycle SM2=1,4 clocks per cycles	10	t_{XHQX}		$12\ t_{CLCL}$ $4\ t_{CLCL}$		ns ns
Input Data Hold to Clock Rising SM2=0,12 clocks per cycle SM2=1,4 clocks per cycles	10	t_{XHDX}		$12\ t_{CLCL}$ $4\ t_{CLCL}$		ns ns
Clock Rising Edge to Input Data Valid SM2=0,12 clocks per cycle SM2=1,4 clocks per cycles	10	t_{XHDV}		$12\ t_{CLCL}$ $4\ t_{CLCL}$		ns ns

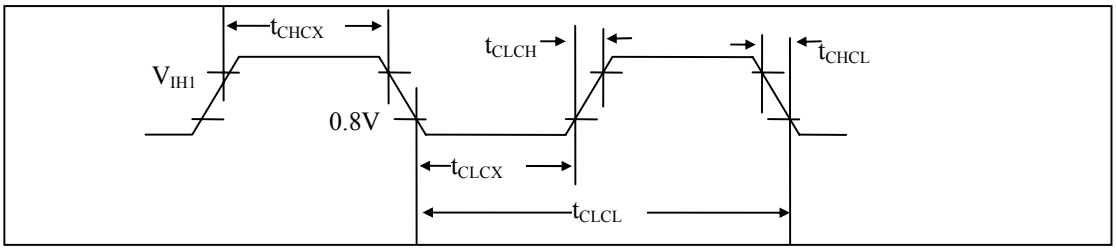


Figure 4 External Clock Drive waveform

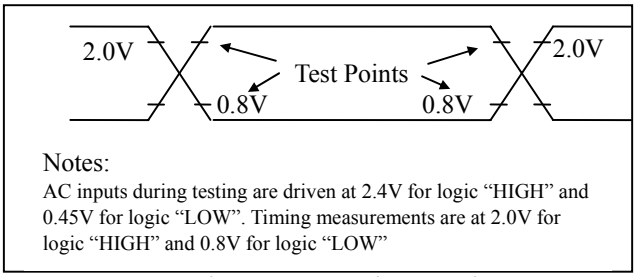


Figure 5 AC Testing Input/Output

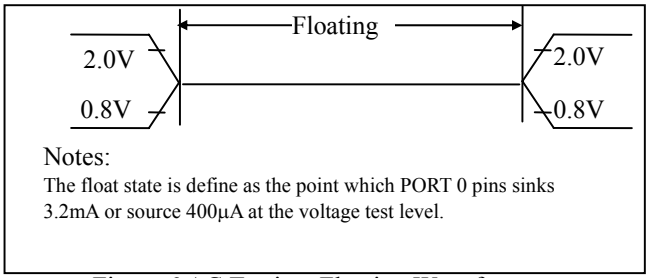


Figure 6 AC Testing, Floating Waveform

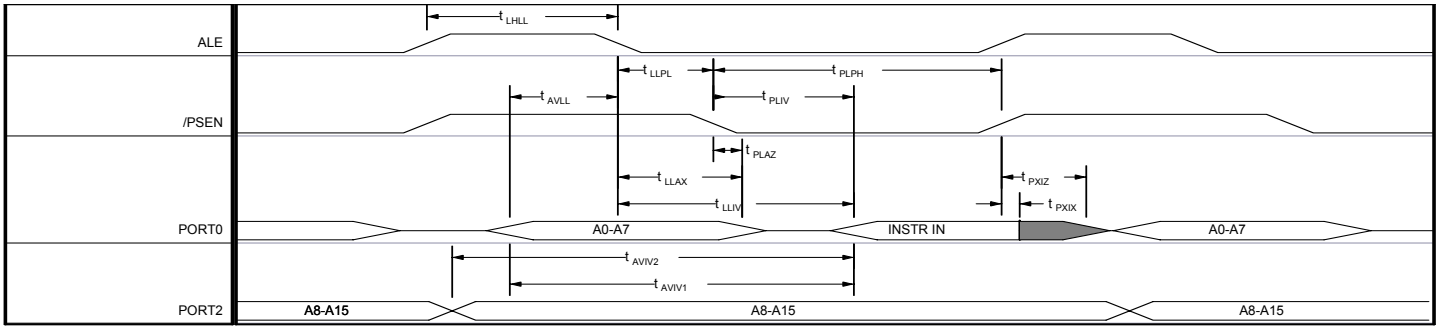


Figure 7 External Program Memory Read Cycle

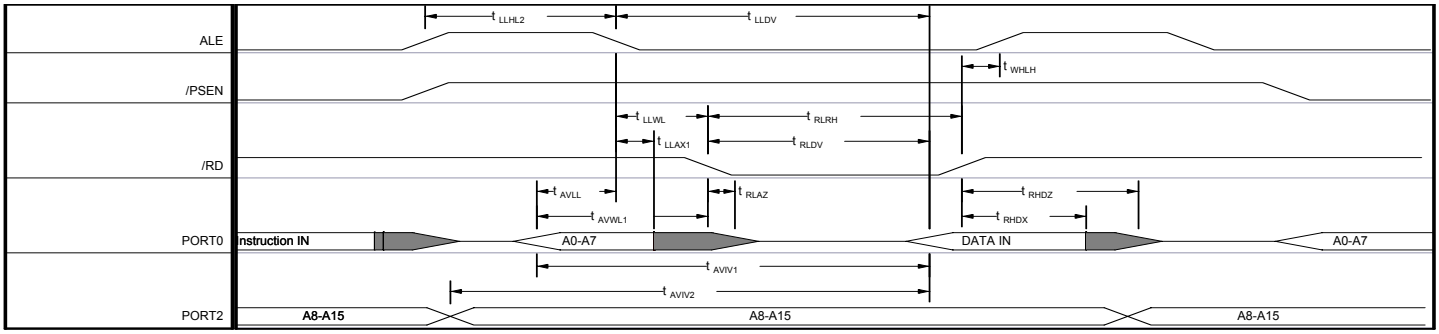


Figure 8 External Data Memory Read cycle

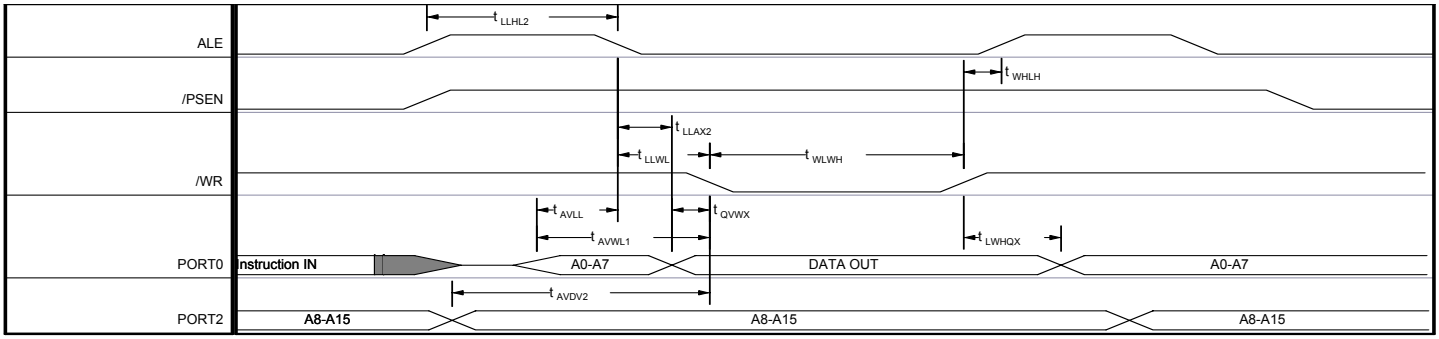


Figure 9 External Data Memory Write cycle

UART (Synchronous Mode)

High Speed Operation SM2=1 => TXD Clock =XTAL/4

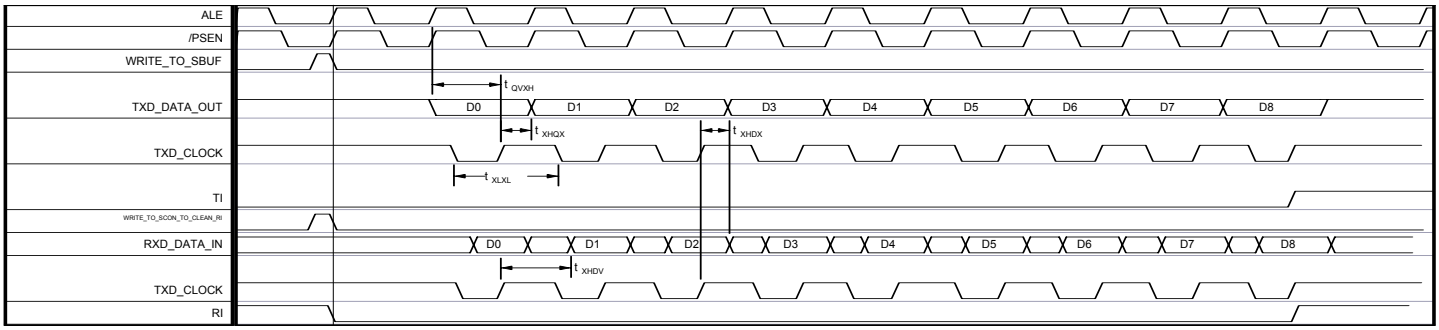


Figure 10 UART Mode 1Timing

UART (Synchronous Mode)

SM2=0 => TXD Clock =XTAL/12

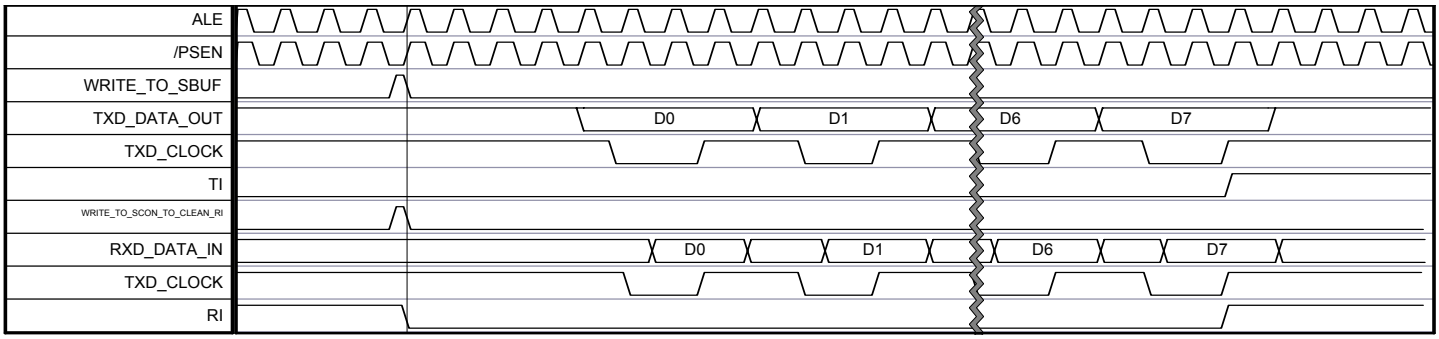


Figure 11 UART Mode 0 Timing

Function Description

The SM89T16R1 is a High-Speed (4 clocks/machine cycle) stand-alone high-performance microcontroller designed for use in 3V/5V application, such as LCD monitor, instrumentation, or high-end consumer applications.
In addition to the 80C51 standard functions, the device provides a number of dedicated hardware functions for these applications.
The SM89T16R1 is a control-oriented CPU with on-chip program and data memory. It can be extended with external data memory up to 64K bytes. For system requiring extra capability, the SM89T16R1 can be enhanced by using external memory and peripherals.
The SM89T16R1 has two software selectable modes of saving power consumption-IDLE and POWER-DOWN. The IDLE mode freezes the CPU while allowing the RAM, timer, serial ports and interrupt system to continue functioning. The POWER-DOWN mode save the RAM contents but freezes the oscillator causing all other chip functions to be inoperative. The POWER-DOWN mode can be terminated by H/W reset, or by any one of the six external interrupt or RTC function.

CPU

The CPU of SM89T16R1 is High-Speed 80C51. The structure of this CPU is shown as FIGURE 12. It contains Instruction Register (IR), Instruction Decoder, Program Counter (PC), Accumulator (ACC), B Register, and control logic. This CPU provides an 8-bits bi-direction bus to communicate with other blocks in the chip. The address and data are transferred through on the same 8-bits bus.

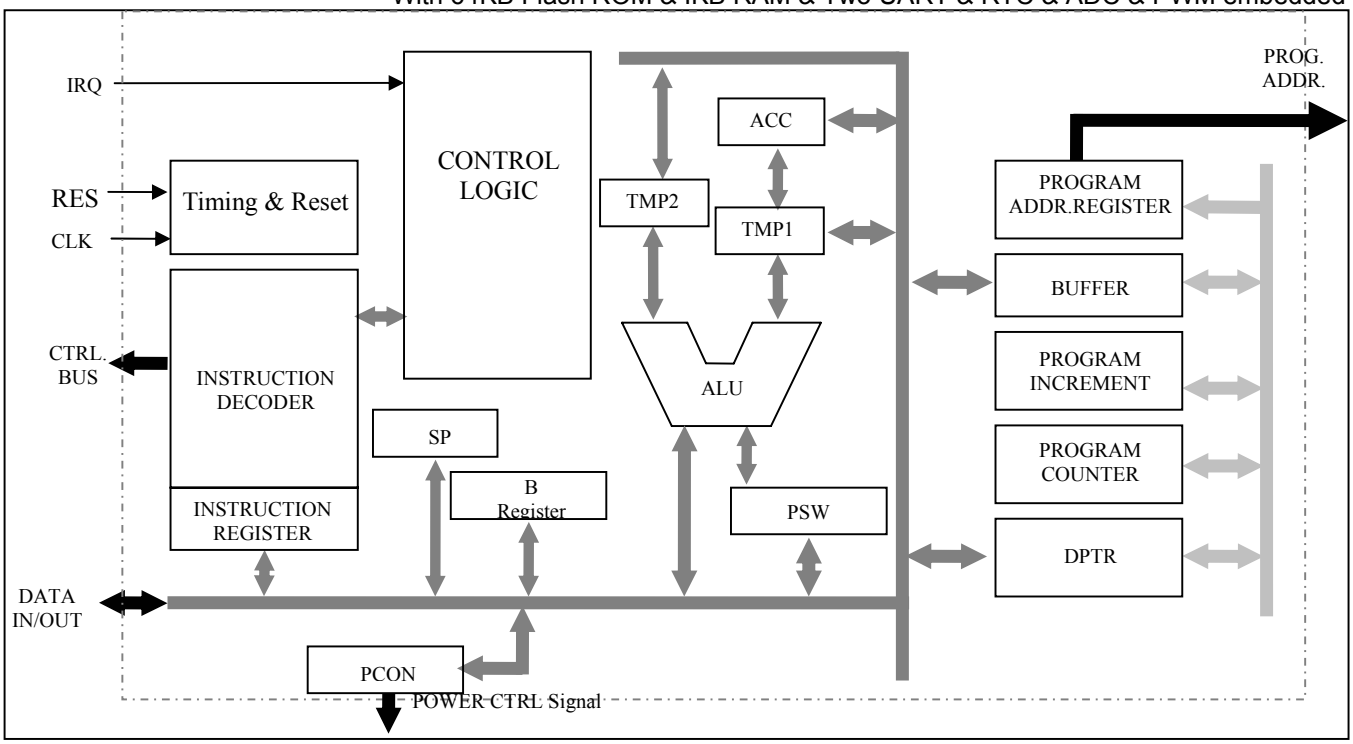


Figure 12 The CPU Structure

CPU Timing

The machine cycle consists of a sequence of 4 states, numbered S1 through S4. Only one-oscillator periods for each state time. Thus a machine cycle takes 4 oscillator periods. FIGURE 13 Shows relationships between oscillator, phase, and S1-S4.

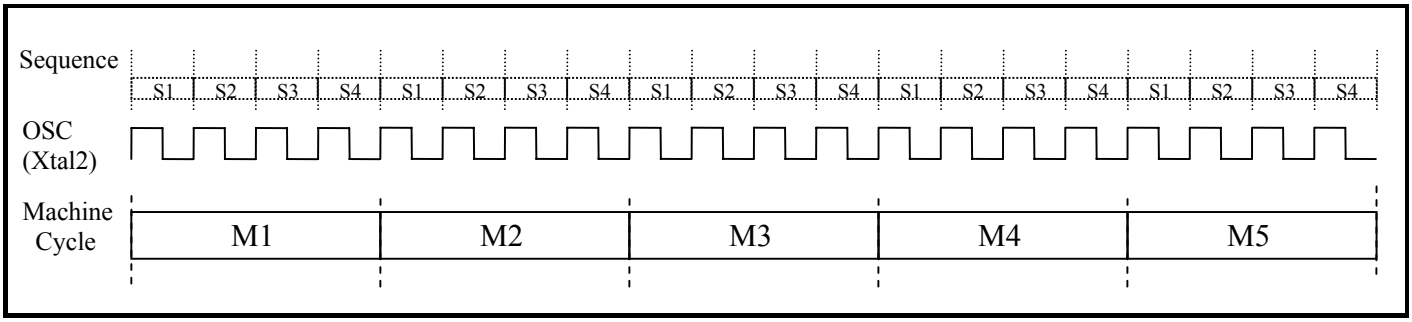
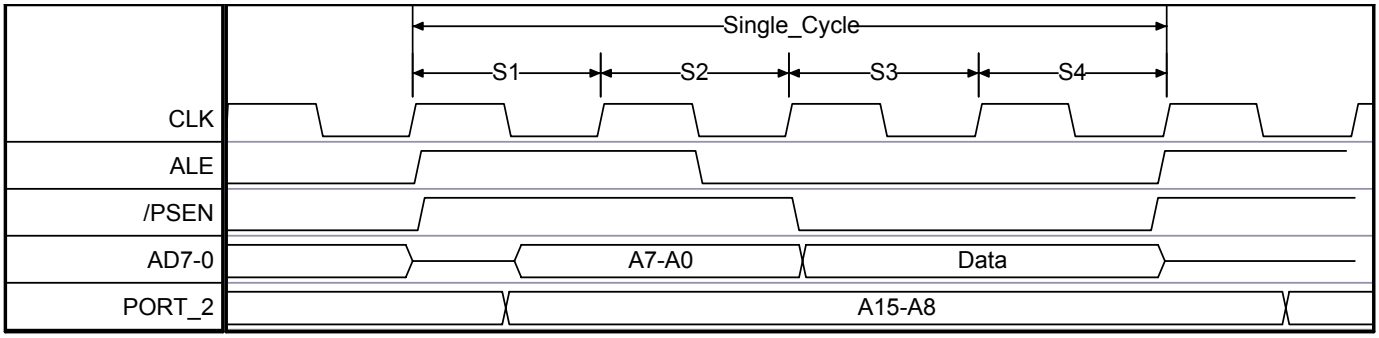


Figure 13 Sequences and Phases

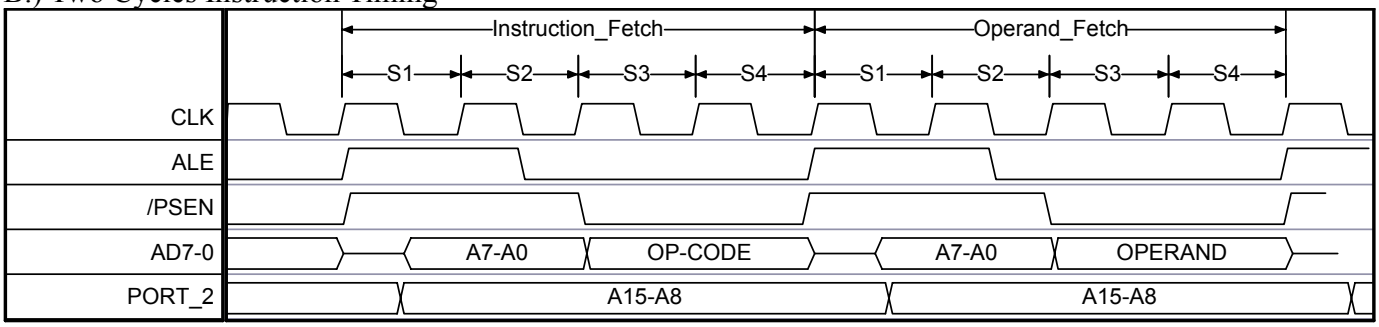
FIGURE 14 shows the fetch / execute sequences in states and phases for various kinds of instructions. Normally the program fetches are generated during each machine cycle, even if the instruction being executed doesn't require it. If the instruction being executed doesn't need more code bytes, the CPU simply ignores the extra fetch, and the PROGRAM COUNTER is incremented accordingly.

Due to the reduced time for each instruction execution, both of the clocks edges are used for internal timing. Hence it is important that the duty cycle of the clock be as close to 50% as possible to avoid timing conflicts. The SM89T16R1 dose one op-code fetch per machine cycle. Therefore, in most of the instructions, the number of machine cycles needed to execute the instruction is equal to the number of bytes in the instruction. Of the 256 available op-codes, 128 of them are signal cycle instruction. See Figure14 shows the different cycle (A-D) instruction timing.

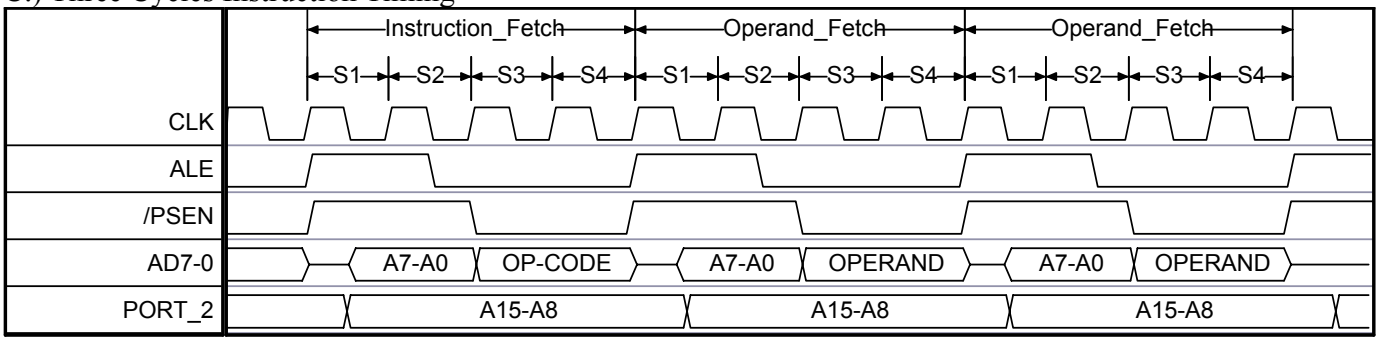
A.) Signal Cycle Instruction Timing



B.) Two Cycles Instruction Timing



C.) Three Cycles Instruction Timing



D.) Four Cycles Instruction Timing

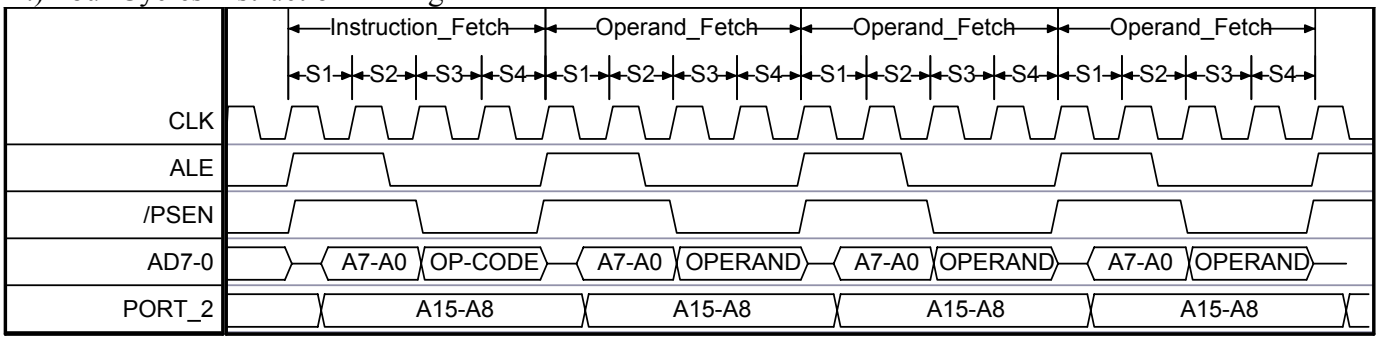
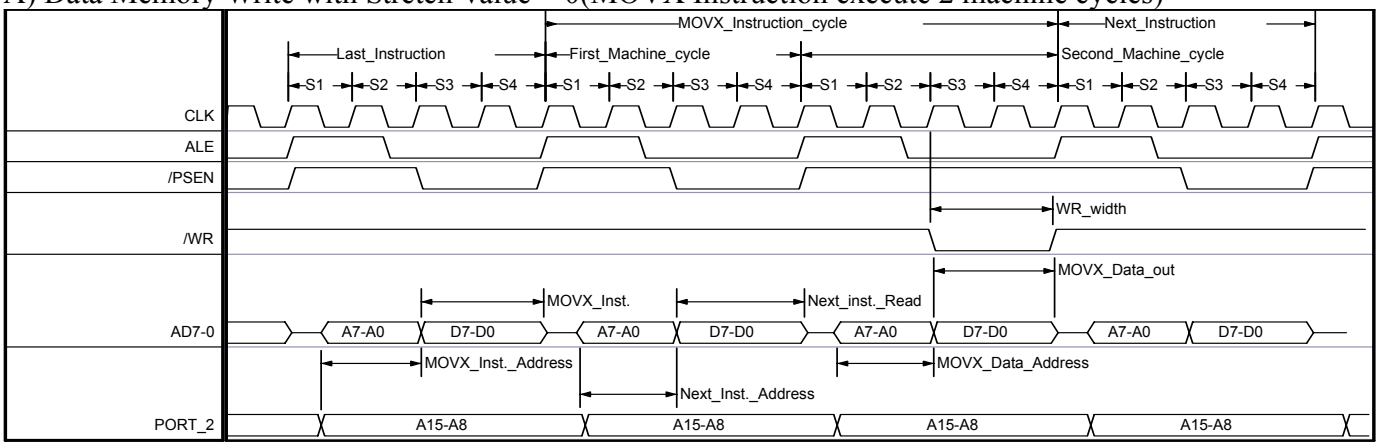


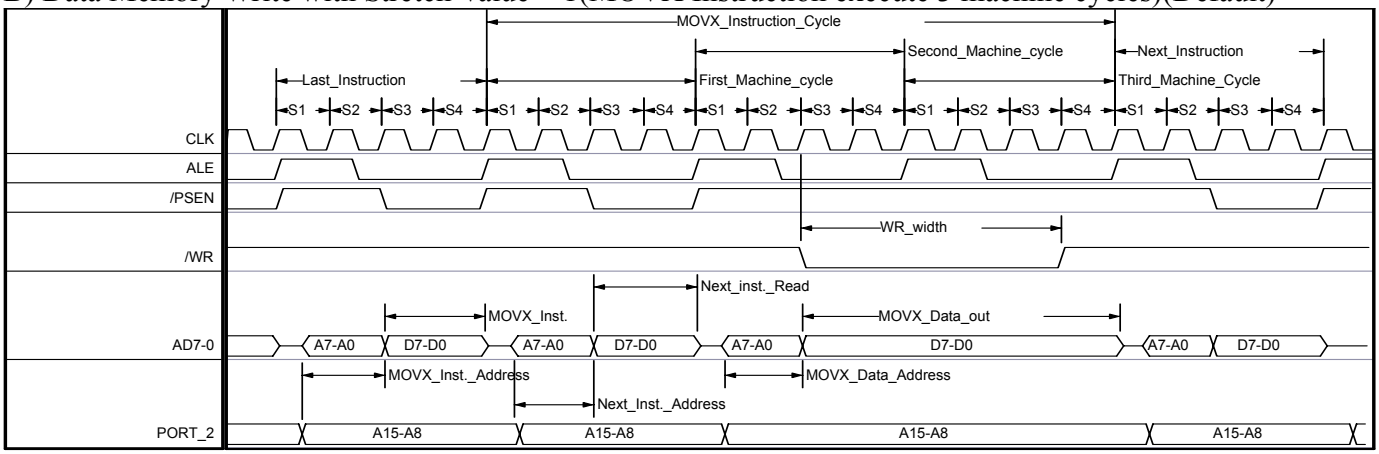
Figure 14 Timing of various instructions

In standard 8032, the MOVX instructions take two machine cycles to execute. However in the SM89T16R1, the user has a facility to stretch the duration of this instruction from 2 machines cycle to 9 machines. The /RD and /WR strobe lines are also proportionately elongated. This gives the user flexibility in accessing both fast and slow peripherals without the use of external circuitry and with minimum software overhead. See FIGURE 15

A) Data Memory Write with Stretch Value = 0(MOVX Instruction execute 2 machine cycles)



B) Data Memory Write with Stretch Value = 1(MOVX Instruction execute 3 machine cycles)(Default)



C) Data Memory Write with Stretch Value = 2(MOVX Instruction execute 4 machine cycles)

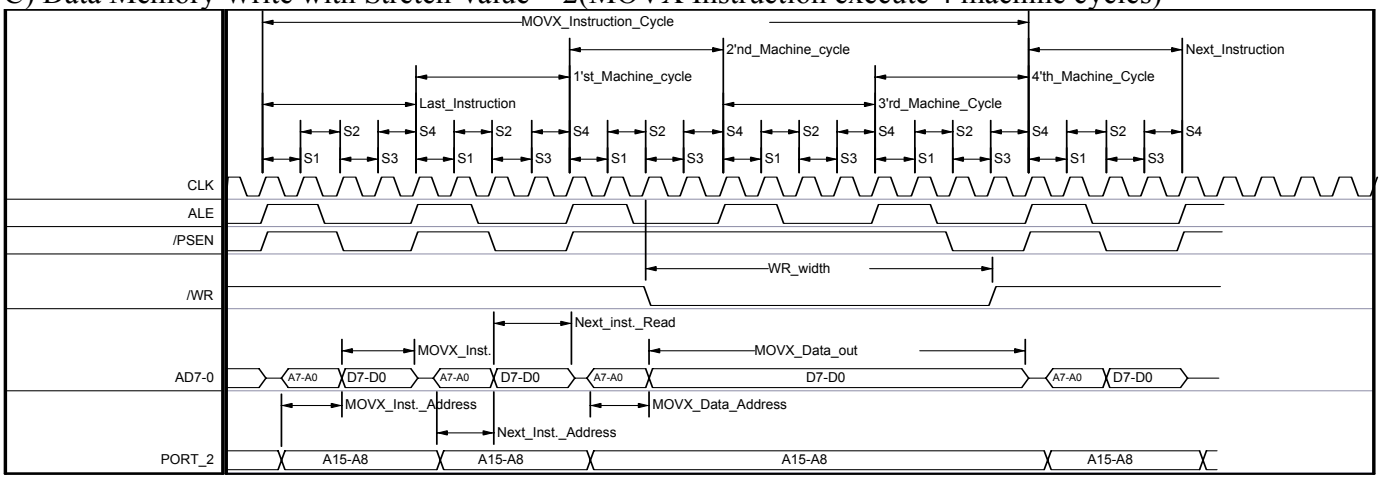


Figure 15: MOVX Instruction Timing (Stretch=0~Stretch=2)

Instruction Set

The SM89T16R1 is High-Speed 80C51; it's contained 4 clocks per machine. The SM89T16R1 dose one op-code fetch per machine cycle .It consists of 111 instructions used 40 single-cycle, 38 used two-cycles, 19 used three-cycles, and 10 used four-cycles.
A summary of the instruction set is given in Table 4.

Addressing Mode

Notes on instruction set and address modes:

Rn	Register R7-R0 of the currently selected register bank.
Direct	8-bits internal data location's address. This could be internal DATA RAM location (0-127) or a SFR[i.e., I/O port, control register, status register, etc.(128-255)]
@Ri	8-bits RAM location addressed indirectly through register R1 or R0 of the actual register bank
#data	8-bits constant included in the instruction
#data16	16-bits constant included in the instruction
addr11	11-bits destination address. Used by ACALL and AJMP. The branch can be anywhere within the same 2 Kbytes page of program memory as the first byte of the following instruction.
Rel	Signed (2's complement) 8-bits offset byte. Used by SJMP and all conditional jumps. Range is -128 to +127 bytes relative to first byte of the following instruction.
Bit	Direct addressed bit in internal data RAM or SFR

Table 4: summary of the instruction

Mnemonic		OPERATION	BYTE	CYCLE
Arithmetic Instructions				
ADD	A,Rn	A = A + Rn	1	1
ADD	A,direct	A = A + direct	2	2
ADD	A,@Ri	A = A + <@Ri>	1	1
ADD	A,#data	A = A + #data	2	2
ADDC	A,Rn	A = A + Rn + C	1	1
ADDC	A,direct	A = A + direct + C	2	2
ADDC	A,@Ri	A = A + @Ri + C	1	1
ADDC	A,#data	A = A + #data + C	2	2
SUBB	A,Rn	A = A − Rn − C	1	1
SUBB	A,direct	A = A − direct − C	2	2
SUBB	A,@Ri	A = A − <@Ri> − C	1	1
SUBB	A,#data	A = A −#data − C	2	2
INC	A	A = A + 1	1	1
INC	Rn	Rn = Rn + 1	1	1
INC	direct	direct = direct + 1	2	2
INC	@Ri	<@Ri> = <@Ri> + 1	1	1
DEC	A	A = A − 1	1	1
DEC	Rn	Rn = Rn − 1	1	1
DEC	direct	direct = direct − 1	2	2
DEC	@Ri	<@Ri> = <@Ri> − 1	1	1
INC	DPTR	DPTR = DPTR + 1	1	1
DEC	DPTR	DPTR = DPTR − 1	1	1
MUL	AB	B:A = A × B	1	1
DIV	AB	A = INT (A/B),B = MOD (A/B)	1	3
DA	A	Decimal adjust ACC	1	1
Logical Instructions				
ANL	A,Rn	A .AND. Rn	1	1
ANL	A,direct	A .AND. direct	2	2
ANL	A,@Ri	A .AND. <@Ri>	1	1
ANL	A,#data	A .AND. #data	2	2
ANL	direct,A	direct .AND. A	2	2
ANL	direct,#data	direct .AND. #data	3	3
ORL	A,Rn	A .OR. Rn	1	1
ORL	A,direct	A .OR. direct	2	2
ORL	A,@Ri	A .OR. <@Ri>	1	1
ORL	A,#data	A .OR. #data	2	2
ORL	direct,A	direct .OR. A	2	2

ORL	direct,#data	direct .OR. #data	3	3
XRL	A,Rn	A .XOR. Rn	1	1
XRL	A,direct	A .XOR. direct	2	2
XRL	A,@Ri	A .XOR. <@Ri>	1	1
XRL	A,#data	A .XOR. #data	2	2
XRL	direct,A	direct .XOR. A	2	2
XRL	direct,#data	direct .XOR. #data	3	3
CLR	A	A = 0	1	1
CPL	A	A = /A	1	1
RL	A	Rotate ACC Left 1 bit	1	1
RLC	A	Rotate Left through Carry	1	1
RR	A	Rotate ACC Right 1 bit	1	1
RRC	A	Rotate Right through Carry	1	1
SWAP	A	Swap Nibbles in A	1	1
Data Transfers Instructions				
MOV	A,Rn	A = Rn	1	1
MOV	A,direct	A = direct	2	2
MOV	A,@Ri	A = <@Ri>	1	1
MOV	A,#data	A = #data	2	2
MOV	Rn,A	Rn = A	1	1
MOV	Rn,direct	Rn = direct	2	2
MOV	Rn,#data	Rn = #data	2	2
MOV	direct,A	direct = A	2	2
MOV	direct,Rn	direct = Rn	2	2
MOV	direct,direct	direct = direct	3	3
MOV	direct,@Ri	direct = <@Ri>	2	2
MOV	direct,#data	direct = #data	3	2
MOV	@Ri,A	<@Ri> = A	1	1
MOV	@Ri,direct	<@Ri> = direct	2	2
MOV	@Ri,#data	<@Ri> = #data	2	2
MOV	DPTR,#data16	DPTR = #data16	3	3
MOVC	A,@A+DPTR	A = code memory[A+DPTR]	1	3
MOVC	A,@A+PC	A = code memory[A+PC]	1	3
MOVX	A,@Ri	A = external memory[Ri] (8-bits address)	1	2~9
MOVX	A,@DPTR	A = external memory[DPTR] (16-bits address)	1	2~9
MOVX	@Ri,A	external memory[Ri] = A (8-bits address)	1	2~9
MOVX	@DPTR,A	external memory[DPTR] = A (16-bits address)	1	2~9
PUSH	direct	INC SP: MOV "@'SP', < direct >	2	2~9
POP	direct	MOV < direct >, "@SP": DEC SP	2	2~9
XCH	A,Rn	ACC and < Rn > exchange data	1	1
XCH	A,direct	ACC and < direct > exchange data	2	2
XCH	A,@Ri	ACC and < Ri > exchange data	1	1
XCHD	A,@Ri	ACC and @Ri exchange low nibbles	1	1
Boolean Instructions				
CLR	C	C = 0	1	1
CLR	bit	bit = 0	2	2
SETB	C	C = 1	1	1
SETB	bit	bit = 1	2	2
CPL	C	C = /C	1	1
CPL	bit	bit = /bit	2	2
ANL	C,bit	C = C .AND. bit	2	2
ANL	C,/bit	C = C .AND. /bit	2	2
ORL	C,bit	C = C .OR. bit	2	2
ORL	C,/bit	C = C .OR. /bit	2	2
MOV	C,bit	C = bit	2	2
MOV	bit,C	bit = C	2	2
JC	rel	Jump if C= 1	2	3
JNC	rel	Jump if C= 0	2	3
JB	bit,rel	Jump if bit = 1	3	4
JNB	bit,rel	Jump if bit = 0	3	4
JBC	bit,rel	Jump if C = 1	3	4
Jump Instructions				
JZ	rel	Jump if A = 0	2	3

JNZ	rel	Jump if A ≠ 0	2	3
JMP	@A+DPTR	Jump to A+ DPTR	1	2
DJNZ	Ri,rel	Decrement and jump if Rn not zero	2	3
DJNZ	Direct,rel	Decrement and jump if direct not zero	3	4
CJNE	A,direct,rel	Jump if A ≠ < direct >	3	4
CJNE	A,#data,rel	Jump if A ≠ < #data >	3	4
CJNE	@Ri,#data,rel	Jump if Rn ≠ < #data >	3	4
CJNE	Ri,#data,rel	Jump if @Ri ≠ < #data >	3	4
ACALL	Address11	Call Subroutine only at 2k bytes Address	2	3
AJMP	Address11	Jump only At 2k bytes addressing	2	3
LCALL	Address16	Call Subroutine in max 64K bytes Address	3	4
LJMP	Address16	Jump to max 64K bytes Address	3	4
SJMP	rel	Jump on at 256 bytes	2	3
RET		Return from subroutine	1	3
RETI		Return from interrupt	1	3
NOP		No Operation	1	1

Memory organization

Program memory

The program memory of SM89T16R1 consists of 64K bytes FLASH memory on chip. If during RESET, the /EA pin was held HIGH, the SM89T16R1 does not execute out of the internal program memory. If the /EA pin was held LOW during RESET the SM89T16R1 fetch all instructions from the external program memory.

Internal Data memory

The Data memory of SM89T16R1 consists of 1280 bytes internal data memory (256 bytes standard RAM and 1024 bytes AUX-RAM). The AUX-RAM is enable by SCONF.1 ($BF.1), and read/write by MOVX (Stretch=0, 2 machine fixed)

Analog to Digital Converter (ADC)

The ADC Block Diagram Shown as below:
Those are only 4 pins mirror to Port 2[7:4] at Vin<3:0>. The Digital output DATA [7:0] were put into ADCD ($8FH). And the ADC interrupt vector is 4BH.
The ADC SFR is shown as below:

ADSCR ($8EH)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
COM	CON	ADCSS1	ADCSS0	CH1	CH0		

COM: Read only. When conversion complete, it will be set.
CON: when set, the ADC will conversion continuous, else it will conversion only once.
ADCSS [1:0]: ADC clock select. (ADC_CLK range 500 KHz~2.5 MHz).If over frequency of ADC_CLK, the conversion data may be unstable.

ADCSS1	ADCSS0	ADC_CLK
0	0	FOSC/4
0	1	FOSC/8
1	0	FOSC/16
1	1	FOSC/32

CH [1:0]: ADC channel select.

CH1	CH0	Input select
0	0	CH0
0	1	CH1
1	0	CH2
1	1	CH3

ADCD ($8FH)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
AD.5	AD.4	AD.3	AD.2	AD.1	AD.0		

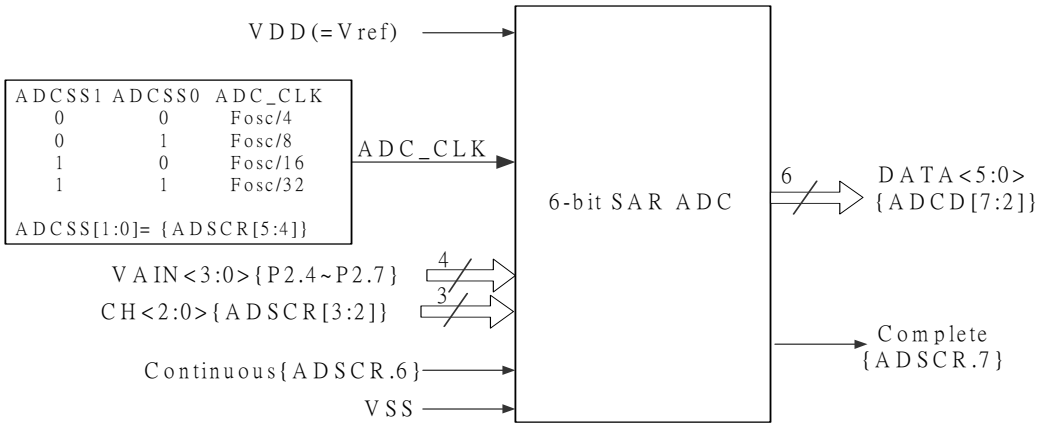


Figure 16 ADC Block Diagram

Dual UART

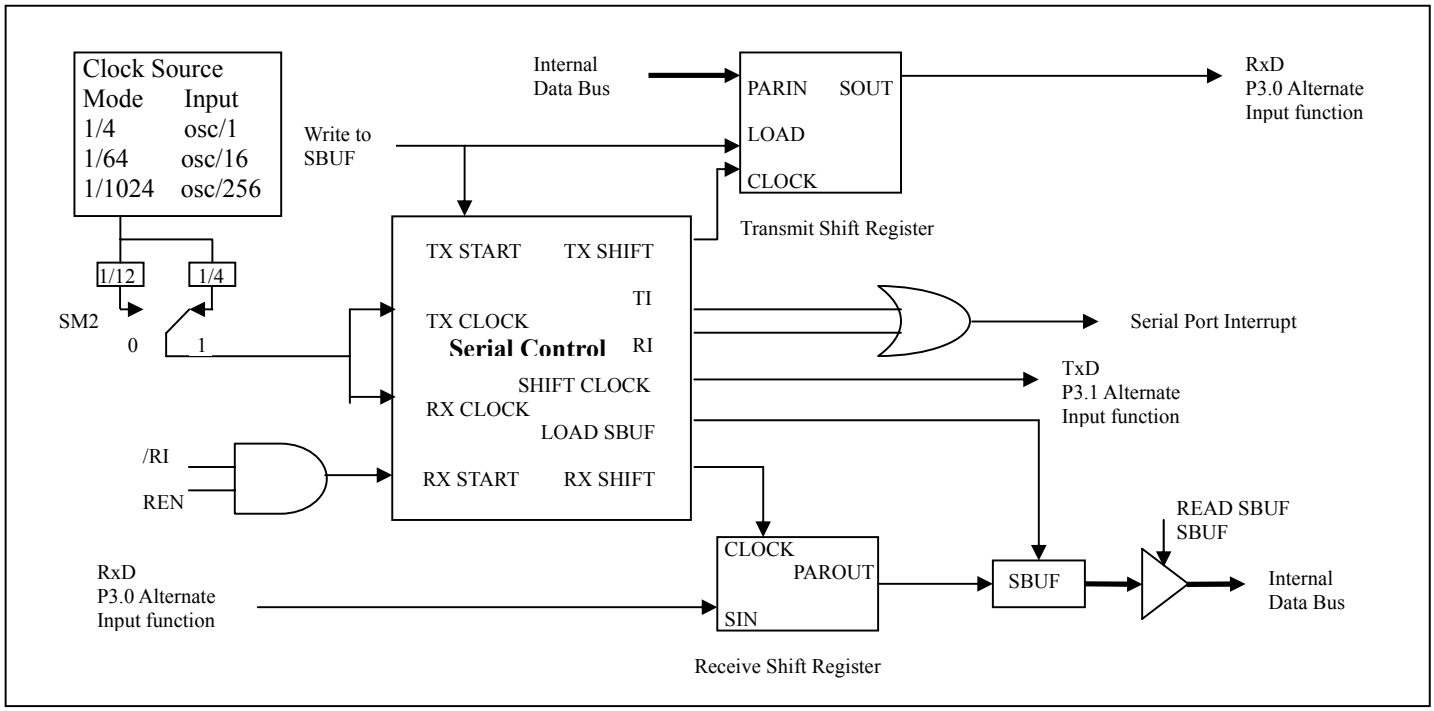
Serial Port in the SM89T16R1 is a full duplex port. The SM89T16R1 provides the user with additional features such as the Frame Error Detection and the Automatic Address Recognition. The serial ports are capable of synchronous as well as asynchronous communication. In Synchronous mode the SM89T16R1 generates the clock and operates in a half duplex mode. In the asynchronous mode, full duplex operation is available. This means that it can simultaneously transmit and receive data. The transmit register and the receive buffer are both addressed as SBUF Special Function Register. However any write to SBUF will be to the transmit register, while a read from the receive buffer register. The serial port can operate in four different modes as described below.

Mode 0

This mode provides synchronous communication with external devices. In this mode serial data is transmitted and received on the RxD line. TxD is used to transmit the shift clock. The TxD clock is provided by the SM89T16R1 whether the device is transmitting or receiving. This mode is therefore a half duplex mode of serial communication. In this mode, 8 bits are transmitted or received per frame. The LSB is transmitted / received first. The baud rate is fixed at 1/12 or 1/4 of the oscillator frequency. This baud rate is determined at the SM2 bit (SCON.5). When this bit is set to 0, then the serial port runs at 1/12 of the clock. When set to 1, the serial port runs at 1/4 of the clock. This additional facility of programmable baud rate in mode 0 is the only difference between the standard 8051 and the SM89T16R1. The function block diagram is shown below. Data enters and leaves the Serial port on the RxD line. The TxD line is used to output the shift clock. The shift clock is used to shift data into and out of the SM89T16R1 and the device at the other end of the line. Any instruction that causes a write to SBUF will start the transmission. The shift clock will be activated and data will shifted out on the RxD pin till all 8 bits are transmitted. If SM2 = 1, then the data on RxD will appear 1 clock period before the falling edge of shift clock on TxD. The clock on TxD then remains low for 2 clock periods, and then goes high again. If SM2 = 0, the data on RxD will appear 3 clock periods before the falling edge of shift clock on TxD. The clock on TxD then remains low for 6 clock periods, and then goes high again. This ensures that at the receiving end the data on RxD line can either be clocked on the rising edge of the shift clock on TxD or latched when the TxD clock is low.

The TI flag is set high following the end of transmission of the last bit. The serial port will receive data when REN is 1 and RI is zero. The shift clock (TxD) will be activated and the serial port will latch data on the rising edge of the shift clock. The external device should therefore present data on the falling edge on the shift clock. This process continues till all the 8 bits have been received. The RI flag is set following the last rising edge of the shift clock on TxD. This will stop reception, till the RI is cleared by software.

Serial Port Mode 0:



Mode 1

In mode 1, the full duplex asynchronous mode is used. Serial communication frames are made up of 10 bits transmitted on TxD and received on RxD. The 10 bits consist of a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive; the stop bit goes into RB8 in the SFR SCON. The baud rate in this mode is variable. The serial baud can be programmed to be 1/16 or 1/32 of the Timer 1 overflow. Since the Timer 1 can be set to different reload values, a wide variation in baud rates is possible.

Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin following the first rollover of divide by 16 counter. The next bit is placed on TxD pin following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide by 16 counter and not directly to the write to SBUF signal. After all 8 bits of data are transmitted the stop bit is transmitted. The TI flag is set after the stop bit has been put out on TxD pin. This will be at the 10th rollover of the divide by 16 counter after a write to SBUF.

Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of the falling edge on the RxD pin; the 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 counter.

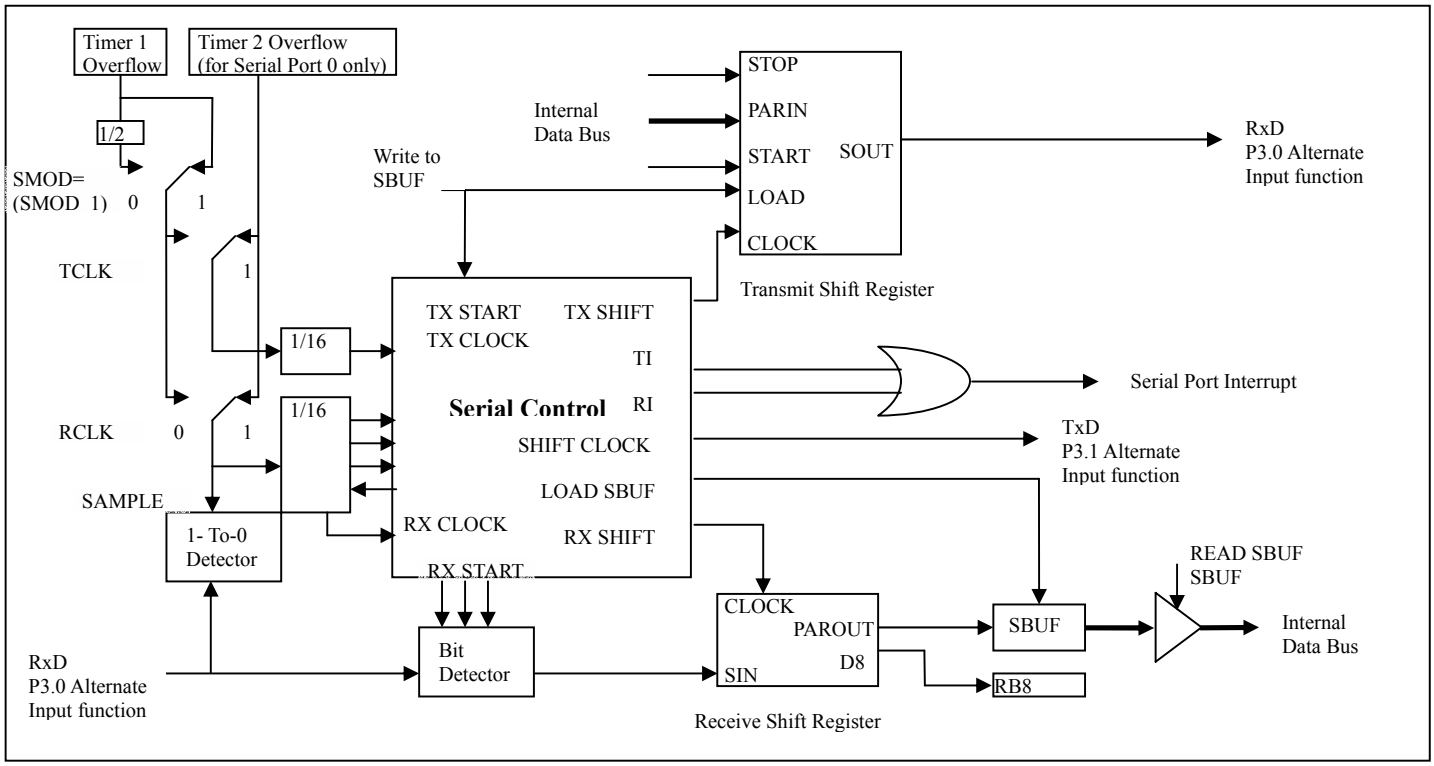
The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three bases. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 or 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port. If the first bit detected after the falling edge of RxD pin is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF.

After shifting in 8 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

RI must be 0 and Either SM2 = 0, or the received stop bit = 1.

If these conditions are met, then the stop bit goes to RB8; the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

Serial Port Mode 1:



Mode 2

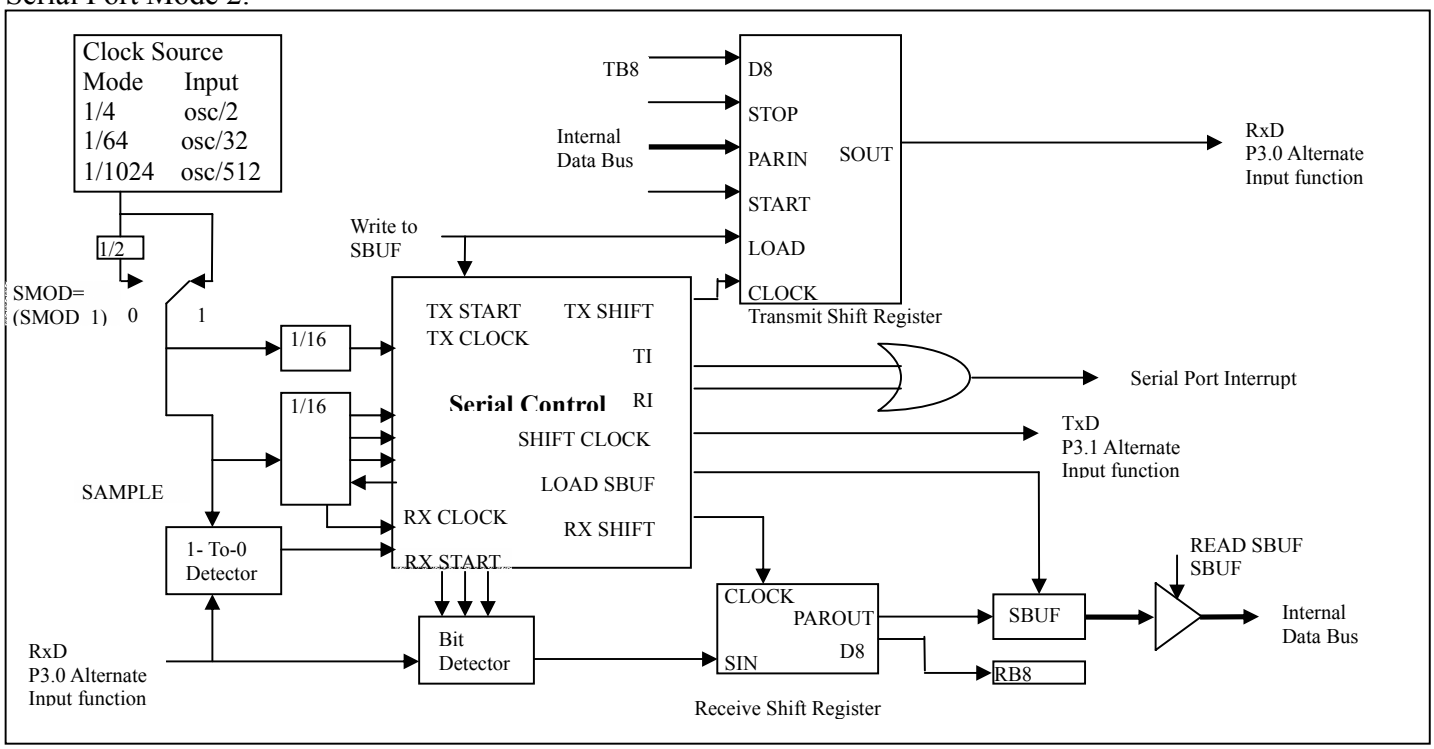
This mode uses a total of 11 bits in asynchronous full-duplex communication. The functional description is shown in the figure below. The frame consists of one start bit (0), 8 data bits (LSB first), a programmable 9th bit (TB8) and a stop bit (0). The 9th bit received is put into RB8. The baud rate is programmable to 1/32 or 1/64 of the oscillator frequency, which is determined by the SMOD bit in PCON SFR. Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin following the first rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide by 16 counter, and not directly to the write to SBUF signal. After all 9 bits of data are transmitted the stop bit is transmitted. The TI flag is set after the stop bit has been put out on TxD pin. This will be at the 11th rollover of the divide by 16 counter after a write to SBUF. Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 counter. The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three bases. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port.

If the first bit detected after the falling edge of RxD pin, is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF. After shifting in 9 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

RI must be 0 and Either SM2 = 0, or the received 9th bit = 1.

If these conditions are met, then the 9th bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

Serial Port Mode 2:



Mode 3

This mode is similar to Mode 2 in all respects; expect that the baud rate is programmable. The user must first initialize the Serial related SFR SCON before any communication can take place. This involves selection of the Mode and Baud rate. The Timer 1 should also be initialized if modes 1 and 3 are used. In all four modes, transmission is started by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 0. This will generate a clock on the TxD pin and shift in 8 bits on the RxD pin. Reception is initiated in the other modes by the incoming start bit if REN = 1. The external device will start the communication by transmitting the start bit.

Pulse Width Modulation (PWM)

The PWM output pins are P1.4 and P1.5.
The PWM clock is {Fosc/ (2xDivider)}, the PWM output frequency is {(PWM clock)/32} at 5 bits resolution and {(PWM clock)/256} at 8 bits resolution.
The PWM SFR is shown as below:

PWMC ($D3H and $D4H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					PBS	PFS1	PFS0

PBS: when set, the PWM is 5 bits resolution.
PFS [1:0]: The PWM clock divider select.

PFS1	PFS0	PWM clock divider select
0	0	1
0	1	2
1	0	4
1	1	8

PWMD ($B3H and $B4H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMD.7	PWMD.6	PWMD.5	PWMD.4	PWMD.3	PWMD.2	PWMD.1	PWMD.0

Real Time Clock (RTC)

The on-chip RTC keeps time of second and minute functions. Its time base is a 32.768 KHz crystal between pins X32OUT (alternate function of ALE) and X32IN (alternate function of PSEN). The RTC maintains time to a second. It also allows a user to read or write values of seconds and minute.
The RTC function used SFR descriptor as below:

RTCS ($A1H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RTCen	Stable	SEC.5	SEC.4	SEC.3	SEC.2	SEC.1	SEC.0

RTCen: When set to '1', enable the enable RTC function. When this bit set, the ALE and PSEN pins output will disable, and the ALE and PSEN pins will use for RTC function as X32OUT and X32IN.
Stable: Read only. The Stable bit will set to 1 when the RTC module stable. Please wait 2 seconds before used the RTC function.
SEC [5:0]: show the current second counter at RTC function. The range is from 00H to 3BH.

RTCC ($A2H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INT_SEL1	INT_SEL0	MIN.5	MIN.4	MIN.3	MIN.2	MIN.1	MIN.0

INT_SEL [1:0]: the interrupt distribution selection bit, the interrupt vector is 43H.
00: the interrupt is set as 0.5 second
01: the interrupt is set as 1 second
10: the interrupt is set as 30 second
11: the interrupt is set as 60 second
MIN [5:0]: show the current minute counter at RTC function. The range is from 00H to 3BH.

Starting and stopping the RTC:

RTCS ($A1H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RTCen	Stable	SEC.5	SEC.4	SEC.3	SEC.2	SEC.1	SEC.0

The RTC Function is enable by set the RTCS.7 (RTCen=1), then the ALE and /PSEN pins will switch to X32OUT and X32IN that for RTC function used, the ALE and PSEN signal output will disable; the crystal frequency is 32768Hz. See figure 17.

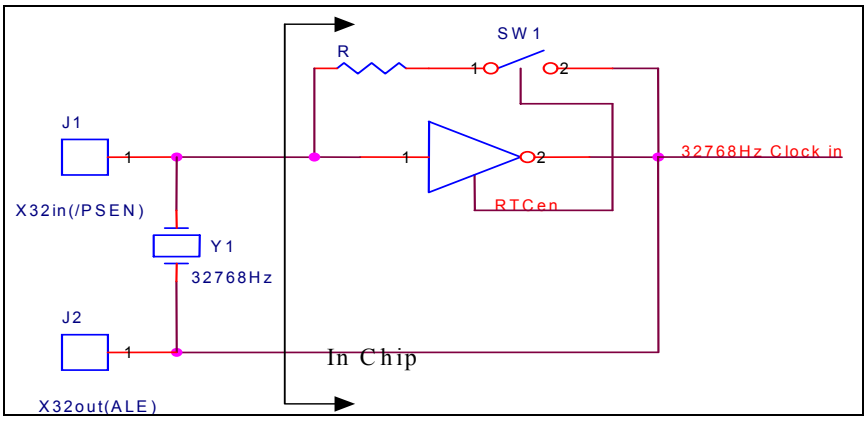


Figure 17 The RTC Crystal connect diagram

The stable bit (RTCS.6) will set to 1 when the RTC module stable. The design is about 31.25msec; suggest waiting 2 second to use the RTC function. This bit will clear when RTCen bit set again.
The SEC [5:0] will show the second counter (range from 00H to 3BH), and the MIN [5:0] will show the minute counter (range from 00H to 3BH) of RTC function. This two register will clear when RTCen bit set.

Interrupt:

The RTC can select each of 4 interrupt sources: 0.5 second, 1 second, 0.5 minute, and 1 minute. The interrupt vector is 43H, it's can wake-up CPU from POWER-DOWN mode.
The Interrupt functions are test at each test item. Like the int0 to int5 are test in PDWU function, the RTC interrupt are test at RTC function test, the ADC interrupt are test at ADC function test.
This test item is focus in the priority test and only checks the lower voltage by each crystal.
The interrupt SFRs show as below:

IE1 ($A9H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
				EADC	ERTC		

ERTC: When set to '1', enable the RTC interrupt. If you want to use the RTC interrupt function, must enable the EA bit in IE.7 and enable the ERTC bit in IE1.2.
EADC: When set to '1', enable the ADC interrupt. If you want to use the ADC interrupt function, must enable the EA bit in IE.7 and enable the EADC bit in IE1.3

RTCC ($A2H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INT_SEL1	INT_SEL0	MIN.5	MIN.4	MIN.3	MIN.2	MIN.1	MIN.0

Then select the interrupt distribution in INT_SEL [1:0] in RTCC [7:6].
The RTC can select each of 4 interrupt sources: 0.5 second, 1 second, 0.5 minute, and 1 minute. The interrupt vector is 43H, it can wake-up CPU from POWER-DOWN mode.

IFR ($AAH)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
				ADCIF	RTCIF		

ADCIF: When interrupt occupy the ADC interrupt flag (IFR.3) will set, and the CPU will execute the interrupt subroutine at the interrupt vector 4BH. The ADC Interrupt Flag must clear by software.
RTCIF: When interrupt occupy the RTC interrupt flag (IFR.2) will set, and the CPU will execute the interrupt subroutine at the interrupt vector 43H. The RTC Interrupt Flag must clear by software.

IP1 ($B9H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
				PADC	PRTC		

The interrupt priority can be set at IP1.2 or IP1.3.
PADC: When set to '1', enable the ADC interrupt priority.
PRTC: When set to '1', enable the RTC interrupt priority.

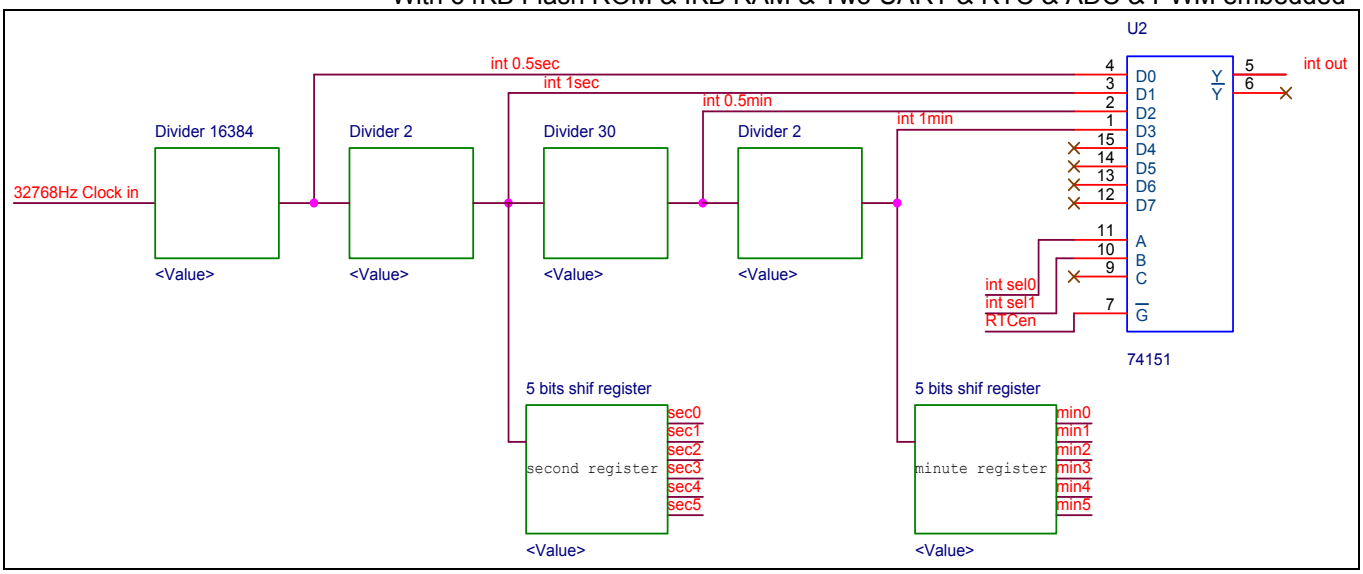


Figure 18 The RTC Block Diagram

LED Driving Capability Control

This function is set the sink current more then 10mA for each pin, 26mA for whole Port 0, 15mA for whole Port 1 or whole Port2 or whole Port3 or whole Port4, and total 71mA for whole chip.
The SFR shown as below:

Port Name	SFR Address	Iol(max) of pre port
Port0	$92H	26 mA
Port1	$93H	15 mA
Port2	$94H	15 mA
Port3	$95H	15 mA
Port4	$96H	15 mA

Power Saving Mode

The SM89T16R1 has several features that help the user to control the power consumption of the device. The powers saving features are basically the Power Down mode, Economy mode and the Idle mode of operation.

Idle Mode

The user can put the device into idle mode by writing 1 to the bit PCON.0. The instruction that sets the idle bit is the last instruction that will be executed before the device goes into Idle Mode. In the Idle Mode, the clock to the CPU is halted, but not to the Interrupt, Timer and Serial port blocks. This forces the CPU state to be frozen; the Program counter, the Stack Pointer, the Program Status Word, the Accumulator and the other registers hold their contents. The ALE and PSEN pins are held high during the idle state. The port pins hold the logical states they had at the time idle was activated. The idle mode can be terminated in two ways. Since the interrupt controller is still active, the activation of any enabled interrupt can wake up the processor. This will automatically clear the idle bit, terminate the idle mode, and the Interrupt Service Routine (ISR) will be executed. After the ISR, execution of the program will continue from the instruction that put the device into idle mode.
The Idle mode can also be exited by activating the reset. The device can be put into reset either applying a high on the external RST pin or a Power on reset condition. The external reset pin has to be held high for at least two machine cycles to be recognized as a valid reset. In the reset condition the program counter is reset to 0000H and all the SFRs are set to the reset condition. Since the clock is already running there is no delay and execution start immediately. When the SM89T16R1 is exiting from an idle mode with a reset, the instruction following the one that put the device into idle mode is not executed. So there is no danger of unexpected writes.

The Power Down Wake Up (PDWU) function

The device can be put into Power Down mode by writing 1 to bit PCON.1. The instruction that does this will be the last instruction to be executed before the device goes into Power Down mode. In the Power Down mode, all the clocks are stopped and the device comes to a halt. All activity is completely stopped and the power consumption is reduced to the lowest possible value. In this state the ALE and PSEN pins are pulled low. The port pins output the values held by their respective SFRs.
The SM89T16R1 will exit the Power Down mode with a reset or by a RTC (Real Time Clock) interrupt or by an external interrupts pin enabled as level detects.

1. An external reset can be used to exit the Power Down state. The high on RST pin terminates the Power Down mode, and restarts the clock. The program execution will restart from 0000H.
2. An external interrupt pin and RTC interrupt can be used to exit the Power Down state when the external interrupt or RTC interrupt actives and provided the corresponding interrupt is enabled, while the global enable (EA) bit is set and the external input has been set to a level detect mode or RTC interrupt set. If these conditions are met, then the low level on the external pin or RTC interrupt re-starts the oscillator. Then device executes the interrupt service routine for the corresponding external interrupt or RTC interrupt. After the interrupt service routine is completed, the program execution returns to the instruction after the one that put the device into Power Down mode and continues from there.

The status of external pins during Idle and Power Down:

Mode	Program Memory	ALE	/PSEN	PORT0	PORT1	PORT2	PORT3	PORT4
Idle	Internal	1	1	Data	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data	Data
Power Down	Internal	0	0	Data	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data	Data

PCON ($87H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SMOD	SMOD0					PD	IDLE

SMOD: This bit set to ‘1’ to make the UART baud-rate double.
SMOD0: This bit define the SCON.7 and SCON1.7 use as FE (FE1) or SM0 (SM0_1)
PD: When set to ‘1’, the MCU will into Power Down mode
IDLE: When set to ‘1’, the MCU will into IDLE mode

IE ($A8H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EA	ET1	ET2	ES0	ET1	EX1	ET0	EX0

EA: When set to ‘1’, enable interrupt global.
ET1: When set to ‘1’, enable Timer1 interrupt.
ET2: When set to ‘1’, enable Timer2 interrupt.
ES0: When set to ‘1’, enable UART interrupt.
ET1: When set to ‘1’, enable Timer1 interrupt.
EX1: When set to ‘1’, enable external interrupt 1.
ET0: When set to ‘1’, enable Timer0 interrupt.
EX0: When set to ‘1’, enable external interrupt 0.

IP ($B8H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		PT2	PS0	PT1	PX1	PT0	PX0

PT2: Timer2 interrupt priority.
PS0: UART interrupts priority.

PT1: Timer1 interrupt priority.
PX1: external interrupt 1 priority.
PT0: Timer0 interrupt priority.
PX0: external interrupt 0 priority.

EIP ($BAH)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
				PX5	PX4	PX3	PX2

PX5: When set to '1', external interrupt 5 priorities.
PX4: When set to '1', external interrupt 4 priorities.
PX3: When set to '1', external interrupt 3 priorities.
PX2: When set to '1', external interrupt 2 priorities.

EIE ($ABH)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
				EX5	EX4	EX3	EX2

EX5: When set to '1', enable external interrupt 5.
EX4: When set to '1', enable external interrupt 4.
EX3: When set to '1', enable external interrupt 3.
EX2: When set to '1', enable external interrupt 2.

TCON ($88H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

TF1: Timer 1 overflow flag.
TR1: Timer 1 run control bit.
TF0: Timer 0 overflow flag.
TR0: Timer 0 run control bit.
IE1: External Interrupt 1 edge flag.
IT1: Interrupt 1 type control bit.
IE0: External Interrupt 0 edge flag.
IT0: Interrupt 0 type control bit.

CKCON ($8EH)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		T2M	T1M	T0M	MD2	MD1	MD0

T2M: Timer 2 clock select. When "1" used divide by 4 clock; when "0" used divide by 12 clock.
T1M: Timer 1 clock select. When "1" used divide by 4 clock; when "0" used divide by 12 clock.
T0M: Timer 0 clock select. When "1" used divide by 4 clock; when "0" used divide by 12 clock.
MD [2:0]: Stretch MOVX selects bits

MD2	MD1	MD0	Stretch Value	MOVX duration
0	0	0	0	2 machine cycles
0	0	1	1	3 machine cycles (Default)
0	1	0	2	4 machine cycles
0	1	1	3	5 machine cycles
1	0	0	4	6 machine cycles
1	0	1	5	7 machine cycles
1	1	0	6	8 machine cycles
1	1	1	7	9 machine cycles

Dual DPTR Function

The DPS.0 define the instruction of INC DPTR AND DEC DPTR are working in DPTR0 or DPTR1.

DPS ($A6H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
							DPS

DPS = 1 the instruction of INC DPTR and DEC DPTR are working in DPTR1.
= 0 the instruction of INC DPTR and DEC DPTR are working in DPTR0.

DPH ($83H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

DPL ($82H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

DPH1 ($A5H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

DPL1 ($A4H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

Data SRAM

The Expand 768 bytes RAM test.
The SCONF.1 must set to '1' to enable the Expand 768 bytes RAM, and this Expand RAM area must read/write by using the MOVX instruction.

SCONF ($BFH)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SMOD_1			PDWUE			OME	ALEI

SMOD_1: This bit set to '1' to make the serial port 1 baud-rate double.
PDWUE: When set to '1', enable the PDWU function.
OME: When set to '1', enable the 768 bytes expanded RAM.
ALEI: When set to '1', it will stop ALE clock output for EMI reduce.

Power Management Mode (PMM)

Power Management Mode offers a complete scheme of reduced internal clock speeds that allow the CPU to run software but to use substantially less power. Normally, during default operation, the SM89T16R1 uses 4 clocks per machine cycle. Thus the instruction cycle (machine cycle clock) rate is clock/4. At 16 MHz crystal speed, the instruction cycle speed is 4 MHz. In Power Management Mode (PMM) the instruction cycle (machine cycle clock) rate is clock/1024. At same 16 MHz crystal speed, the instruction cycle speed is 15.6 KHz. The operation current is down from 20mA to 5mA. See Table 5.

Table 5

Crystal Speed	Full Operation (4 clocks/machine cycle)	PMM (1024 clocks/machine cycle)
	Instruction rate/operation current	Instruction rate/operation current
11.0592 MHz	2.765 MHz/19.6 mA	10.8 KHz/4.78 mA
16 MHz	4.0 MHz/20 mA	15.6 kHZ/5 mA
25 MHz	6.25 MHz/30 mA	24.4 kHz/5.6 mA

Economy Mode

The power consumption of microcontroller relates to operating frequency. The SM89T16R1 offers an Economy mode to reduce the internal clock rate dynamically without external components. By default, one machine cycle needs 4 clocks. In Economy mode, software can select 4, 64, or 1024 clocks per machine cycle. It keeps the CPU operating a acceptable speed but eliminates the power consumption. In the Idle mode, the clock of the core logic is stopped, but all clocked peripherals such as timer are still running at a rate of clock/4. In the Economy mode, all clocks peripherals run at the same reduced clocks rate as in core logic. So the Economy mode may provide lower power consumption than Idle mode.

Software invokes the Economy mode by setting the appropriate bits in the SFRs. Setting the bits CD0 (PMR.6), CD1 (PMR.7) decides the instruction cycle rate as below:

PMR ($D1H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CD1	CD0			XTOFF			

CD1	CD0	Clocks/machine cycle
0	0	Reserved
0	1	4
1	0	64
1	1	1024

Change Clock

Test Internal RC oscillator and External crystal switching

EXIF ($91H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IE5	IE4	IE3	IE2	XT/~RG			

IE5: When set to ‘1’, external interrupt 5 flag.
IE4: When set to ‘1’, external interrupt 4 flag.
IE3: When set to ‘1’, external interrupt 3 flag.
IE2: When set to ‘1’, external interrupt 2 flag.
XT/~RG: When set to ‘1’, the MCU used External Crystal.
When clear to ‘0’, the MCU used Internal RC Oscillator

This selection of instruction rate is going to take effect after a delay of one instruction cycle. Switching to divide by 64 or 1024 mode must first go from divide by 4 modes. This means software cannot switch directly between clock/64 and clock/1024 mode. The CPU has to return clock/4 mode first, then go to clock/64 or clock/1024 mode.

The SM89T16R1 allows the user to use internal RC oscillator instead of external crystal. Setting the XT/~RG bit (EXIF.3) selects the crystal or RC oscillator as the clock source. When invoking RC oscillator in Economy mode, software may set the XTOFF bit to turn off the crystal amplifier for saving power. The CPU would run at the clock rate of approximately 2-4 MHz divided by 4, 64 or 1024. The RC oscillator is not precise so that cannot be invoked to the operation that needs the accurate time-base such as serial communication. If crystal amplifier is disabled and RC oscillator is present clock source, software must first clear the XTOFF bit to turn on crystal amplifier before switch to crystal operation.

PMR ($D1H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CD1	CD0			XTOFF			

XTOFF: External Crystal off; if the XT/~RG bit set to 1, this bit (XTOFF) don’t care.

XT/~RG	XTOFF	Internal Clock Source
0	0	Internal RC Oscillator
0	1	Internal RC Oscillator(Ext-Crystal OFF)
1	0	External Crystal
1	1	External Crystal

The Priority structure and vector locations of interrupts:

Source	Flag	Priority level	Vector Address
External interrupt 0	IE0	1(highest)	03H
Timer 0 overflow	TF0	2	0BH
External interrupt 1	IE1	3	13H
Timer 1 overflow	TF1	4	1BH
UART interrupt	RI+TI	5	23H
Timer 2 overflow	TF2+EXF2	6	2BH
UART 1 interrupt	RI_1+TI_1	7	33H
RTC interrupt	RTCIF	8	43H
ADC interrupt	ADCIF	9	4BH
External interrupt 2	IE2	10	5BH
External interrupt 3	IE3	11	63H
External interrupt 4	IE4	12	6BH
External interrupt 5	IE5	13(lowest)	73H

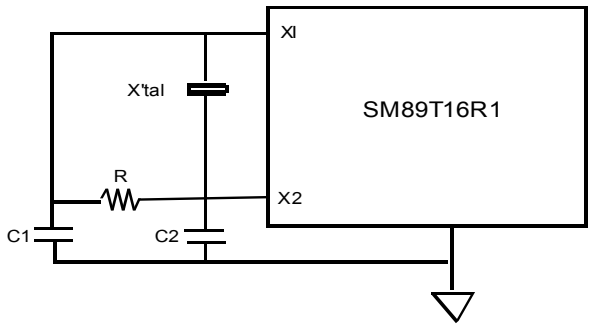
T2MOD ($C9H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
HC5	HC4	HC3	HC2	T2CR		T2OE	DCEN

HC5: Hardware Clear /INT5 flag
HC4: Hardware Clear /INT4 flag
HC3: Hardware Clear /INT3 flag
HC2: Hardware Clear /INT2 flag
T2CR: Timer 2 Capture Reset. In the Timer2 Capture Mode this bit enables/disables hardware automatically reset Timer2 while the value in TL2 and TH2 have been transferred into the capture register.
T2OE: Timer2 clock Output Enable bit. If set to 1, the Timer2 clock will output to P1.0.
DCEN: Down Count Enable. When set this bit then allows Timer2 to be configured as an up/down counter.

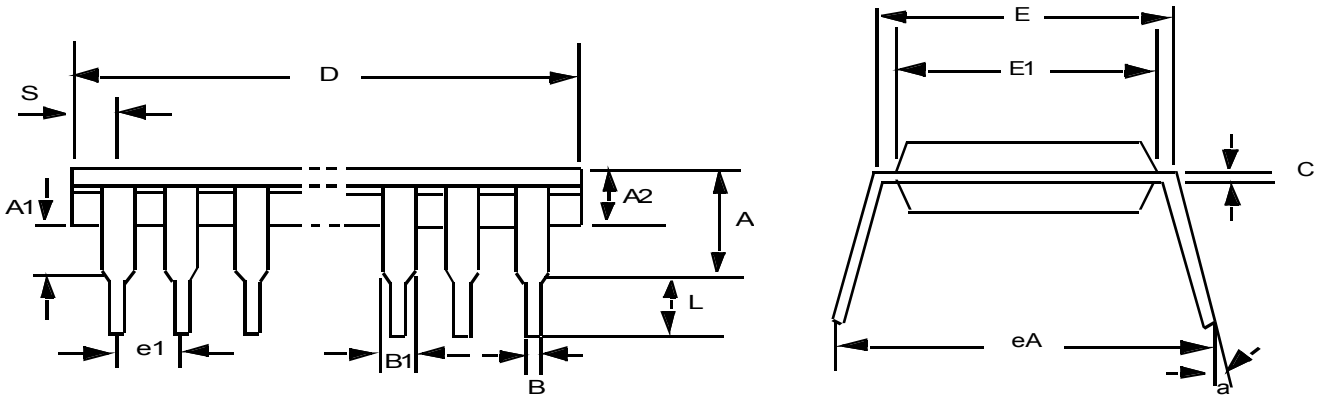
Application Reference

Valid for SM89T16R1				
X'tal	3MHz	6MHz	9MHz	12MHz
C1	30 pF	30 pF	30 pF	22 pF
C2	30 pF	30 pF	30 pF	22 pF
R	open	open	open	open
X'tal	16MHz	25MHz		
C1	30 pF	15 pF		
C2	30 pF	15 pF		
R	open	open		



Note:
Oscillation circuit may differs with different crystal or ceramic resonator in higher oscillation frequency which was due to each crystal or ceramic resonator has its own characteristics.
User should check with the crystal or ceramic resonator manufacturer for appropriate value of external components.

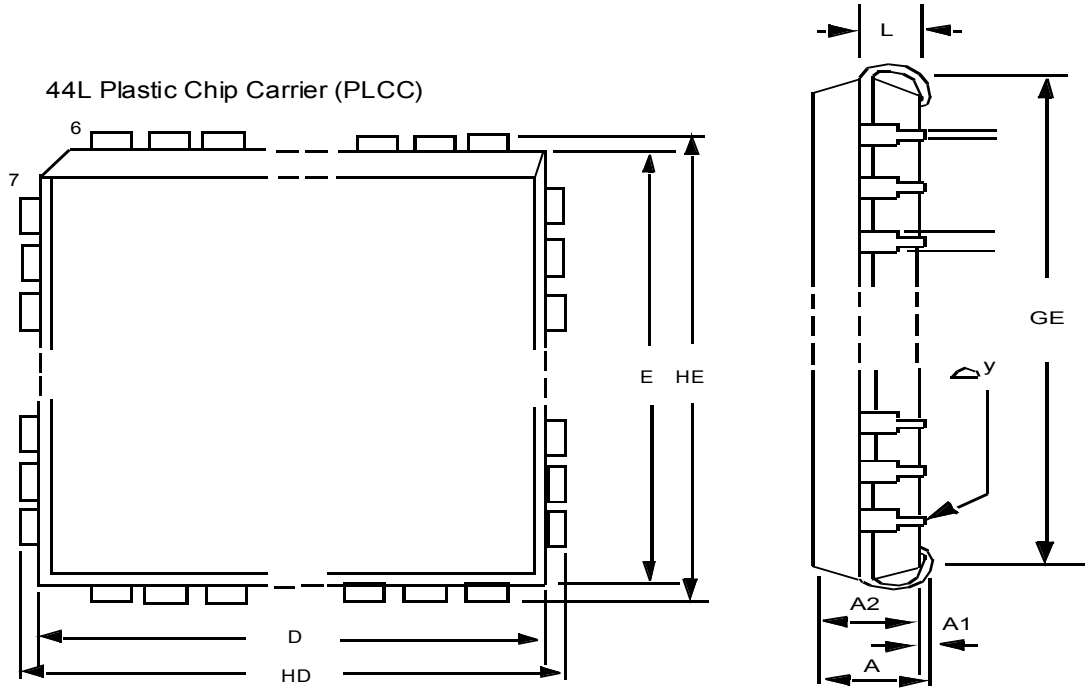
40L 600mil PDIP Information

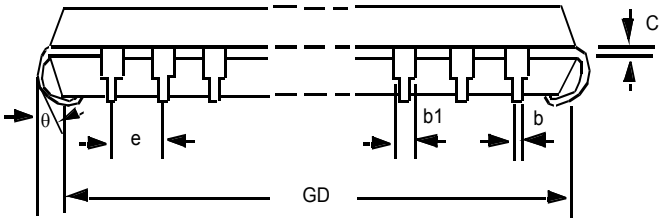


Note:
1. Dimension D Max & include mold flash or tie bar burrs.
2. Dimension E1 does not include inter lead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dam bar protrusion/ infusion.
5. Controlling dimension is inch.
6. General appearance spec. should base on final visual inspection spec.

Symbol	Dimension in inch Minimal / maximal	Dimension in inch Minimal / maximal
A	- / 0.210	- / 5.33
A1	0.010 / -	0.25 / -
A2	0.150 / 0.160	3.81 / 4.06
B	0.016 / 0.022	0.41 / 0.56
B1	0.048 / 0.054	1.22 / 1.37
C	0.008 / 0.014	0.20 / 0.36
D	- / 2.070	- / 52.58
E	0.590 / 0.610	14.99 / 15.49
E1	0.540 / 0.552	13.72 / 14.02
e1	0.090 / 0.110	2.29 / 2.79
L	0.120 / 0.140	3.05 / 3.56
a	0 / 15	0 / 15
eA	0.630 / 0.670	16.00 / 17.02
S	- / 0.090	- / 2.29

44L Plastic Chip Carrier (PLCC)

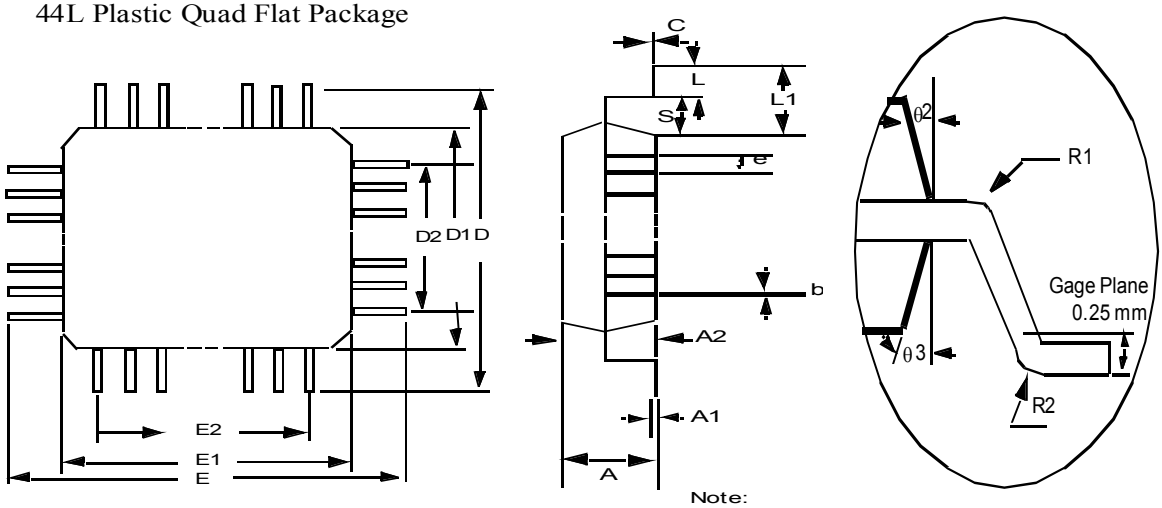


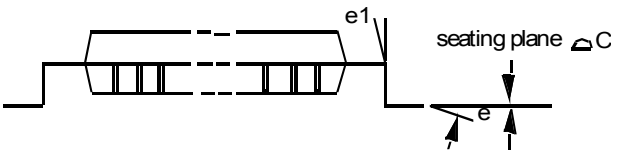


1. Dimension D & E does not include inter lead flash.
2. Dimension b1 does not include dam bar protrusion/ intrusion.
3. Controlling dimension: Inch
4. General appearance spec. should base on final visual inspection spec.

Symbol	Dimension in inch Minimal / maximal	Dimension in inch Minimal / maximal
A	- / 0.185	- / 4.70
A1	0.020 / -	0.51 / -
A2	0.145 / 0.155	3.68 / 3.94
b	0.026 / 0.032	0.66 / 0.81
b1	0.016 / 0.022	0.41 / 0.56
C	0.008 / 0.014	0.20 / 0.36
D	0.648 / 0.658	16.46 / 16.71
E	0.648 / 0.658	16.46 / 16.71
e	0.050 BSC	1.27 BSC
GD	0.590 / 0.630	14.99 / 16.00
GE	0.590 / 0.630	14.99 / 16.00
HD	0.680 / 0.700	17.27 / 17.78
HE	0.680 / 0.700	17.27 / 17.78
L	0.090 / 0.110	2.29 / 2.79
θ	- / 0.004	- / 0.10
y	/	/

44L Plastic Quad Flat Package





Note:
Dimension D1 and E1 do not include mold protrusion. Allowance protrusion is 0.25mm per side.
Dimension D1 and E1 do include mold mismatch and are determined datum plane.
Dimension b does not include dam bar protrusion. Allowance dam bar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dam bar cannot be located on the lower radius or the lead foot.

Symbol	Dimension in inch Minimal / maximal	Dimension in inch Minimal / maximal
A	- / 0.100	- / 2.55
A1	0.006 / 0.014	0.15 / 0.35
A2	0.071 / 0.087	1.80 / 2.20
b	0.012 / 0.018	0.30 / 0.45
c	0.004 / 0.009	0.09 / 0.20
D	0.520 BSC	13.20 BSC
D1	0.394 BSC	10.00 BSC
D2	0.315	8.00
E	0.520 BSC	13.20 BSC
E1	0.394 BSC	10.00 BSC
E2	0.315	8.00
e	0.031 BSC	0.80 BSC
L	0.029 / 0.041	0.73 / 1.03
L1	0.063	1.60
R1	0.005 / -	0.13 / -
R2	0.005 / 0.012℃	0.13 / 0.30
S	0.008 / -	0.20 / -
θ	0℃ / 7℃	as left
θ1	0℃ / -	as left
θ2	10℃ REF	as left
θ3	7℃ REF	as left
⌓C	0.004	0.10