AKD4705-A
AK4705 Evaluation Board Rev.0

GENERAL DESCRIPTION

AKD4705-A is an evaluation board for quickly evaluating the AK4705, 2ch DAC with AV SCART switch. Evaluation requires audio/video analog analyzers/generators, a digital audio signal source, and a power supply. AKM's ADC evaluation board can be also used for the audio source. Also included is a AK4112B digital audio interface receiver which receives S/PDIF compatible audio data. The digital audio data is available via optical connector or BNC.

AKD4705-A --- AK4705 Evaluation Board
(Cable for connecting with printer port of IBM-AT compatible PC and a control software are enclosed with board. This control software dose not support Windows NT.)

FUNCTION

- BNC connectors for analog audio input/output
- BNC connectors for analog video input/output
- On-board clock generator
- BNC connector for an external clock input
- Compatible with 2 types of digital interface

1. Serial interface: Direct interface with evaluation boards for AKM's A/D converter evaluation boards.
2. S/PDIF: On-board AK4112BVF as DIR that accepts optical input or BNC input

- 10pin header for serial control interface

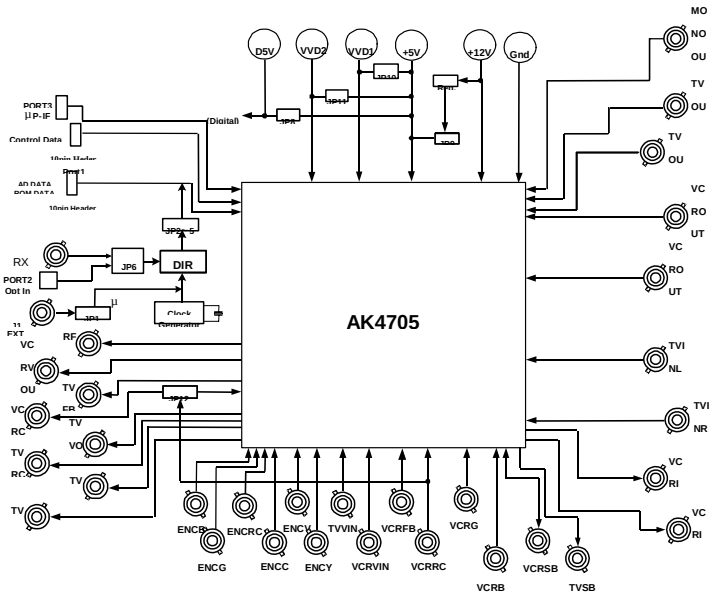


Figure 1. AKD4705-A Block Diagram

- Circuit diagram and PCB layout are attached at the end of this manual.

■ Operation sequence

1) Set up the power supply lines. (Note 1)

[+12V]	(Orange)	= +11.4 ~ +12.6V
[+5V]	(Red)	= +4.75 ~ +5.25V (Note 2)
[D5V]	(Red)	= +4.75~ +5.25V (Note 3)
[VVD1]	(Red)	= +4.75~ VVD2 (Note 4)
[VVD2]	(Blue)	= VDD1~ +5.25V (Note 4)
[AGND]	(Black)	= 0V
[DGND]	(Black)	= 0V
[VVSS2]	(Black)	= 0V

Note: 1. Each supply line should be distributed from the power supply unit.
2. JP9 (REG) should be open when the "+5V" jack is used.
3. JP8 (D-A) should be open when the "D5V" jack is used.
4. JP10 (VDD1) / JP11 (VDD2) should be open when the "VDD1" jack / "VDD2" jack are used independently.

2) Set-up the evaluation modes, jumper pins and DIP-switches. (Refer next sections.)

3) Connect the PORT3 (µP-I/F) with PC by the enclosed 10-wire flat cable.

4) Set up the PC and execute the enclosed control software. (Refer "CONTROL SOFTWARE MANUAL".)

5) Turn the power on.

6) Reset the AK4705 once by bringing the SW1 (PDN) "L", and return it to "H".

■ Evaluation mode

1) S/PDIF mode (Optical Link or BNC: default)

When the CM0 (DIP-switch S1_1 on board) is "L", the AK4112B (DIR) generates MCLK, BICK, LRCK and SDATA from the received bit stream through PORT2 (TORX176: optical link) or J2 (BNC). This mode is used for the evaluation using CD test disk. The PORT1 (EXT) should be open.

1)-1. DIP-switch set-up

No.	CM0	DIF2	DIF0	Audio Data Format of AK4112B	Notes	
1	"L"	"L"	"L"	16bit LSB justified	1	
2	"L"	"L"	"H"	18bit LSB justified	2	
3	"L"	"H"	"L"	24bit MSB justified	3	
4	"L"	"H"	"H"	24bit I^2S	4	(Default)

Table 1. DIP-switch set-up

(Note) AK4112B: DIF1="L"

Much the data format of the AK4705 via I^2C-bus control as following notes.

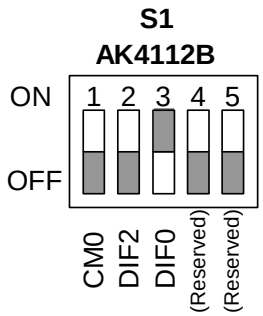
Note 1. 16bit LSB justified

Set up the DIP-switch as follows.

Set up the control registers DIF1/0 of the AK4705 by enclosed software as follows.

Note 2. 18bit LSB justified

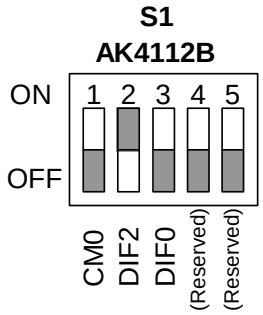
Set up the DIP-switch as follows.



Set up the control registers DIF1/0 of the AK4705 by enclosed software as follows.

Note 3. 24bit MSB justified

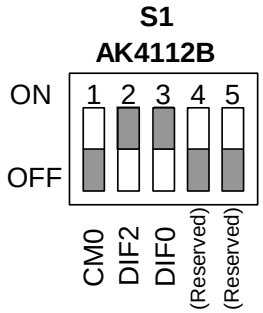
Set up the DIP-switch as follows.



Set up the control registers DIF1/0 of the AK4705 by enclosed software as follows.

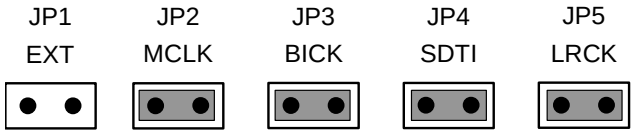
Note 4. 24bit I^2S (Default)

Set up the DIP-switch as follows.



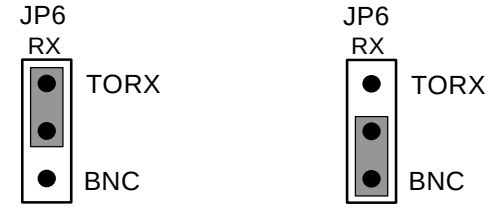
Set up the control registers DIF1/0 of the AK4705 by enclosed software as follows.

1)-2. Jumper pins set up



JP1	JP2	JP3	JP4	JP5
(Open)	(Short)	(Short)	(Short)	(Short)
(Default)	(Default)	(Default)	(Default)	(Default)

The JP6 selects the input port of S/PDIF bit stream form Port2 (TOTX176) or J2 (BNC RX).



2) On-board X'tal mode/ Feeding external MCLK via BNC

When the CM0 (DIP-switch S1_1 on board) is "H", the AK4112B generates MCLK, BICK and LRCK from on-board X'tal or external clock form J1. SDATA should be fed via PORT1.

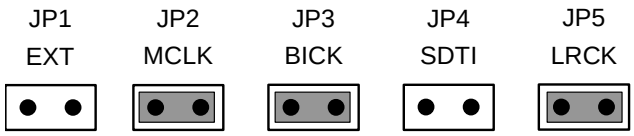
2)-1. DIP-switch set-up

No.	CM0	DIF1	DIF0
1	"H"	Don't care	Don't care

Table 2. DIP-switch set-up

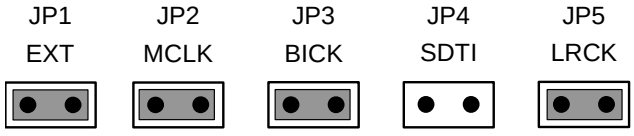
2)-2. Jumper pins set up

2)-2-a. Using on-board X'tal



JP6: Don't care.

2)-2-b. Using external clock via BNC connector J1



JP6: Don't care.
Remove the on-board X'tal.

3) Feeding all clocks from external

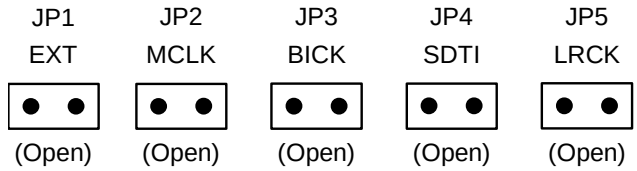
Under the following set-up, all external signals can be fed to the AK4705 through POTR1 (EXT).
The AKM's evaluation board for ADC can be used.

3)-1. DIP-switch set-up

No.	CM0	DIF1	DIF0
1	Don't care	Don't care	Don't care

Table 3. DIP-switch set-up

3)-2. Jumper pins set up



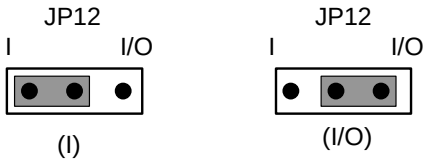
JP6: Don't care.

■ Other jumper pins set up

[JP12](VCRRC): Input Jack selection for the VCRRC pin of AK4705

When the VCRC pin of the AK4705 outputs 0V by setting CIO bit to "1", the signal can be fed through the J27 (VCRCOUT) to VCRRC pin.

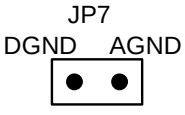
"I": The signal is fed through the J18 (VCRRC) to VCRRC pin. (Default)
"I/O": The signal is fed through the J27 (VCRCOUT) to VCRRC pin.
The CIO bit of AK4705 should be set to "1".



(Default)

[JP7](GND): Analog ground and digital ground

Open: separated. (Default)
Short: connected. (The jack "DGND" can be open.)



(Default)

■ DIP-switch (S1) List

No.	Switch Name	Default	Function
1	CM0	OFF	S/P DIF mode (Refer the evaluation mode)
2	DIF0	ON	24 bit I2S mode (Refer the evaluation mode)
3	DIF2	ON	
4	-	OFF	(Reserved)
5	-	OFF	(Reserved)

Table 4. DIP-switch list

■ Jumper List

No.	Jumper Name	Function
1	EXT	MCLK source set-up when CM0="H". Open: X'tal (Default). Short: External clock via BNC (J1). Remove the on-board X'tal.
2,3, 4,5	MCLK, BICK, LRCK, SDTI	Clock source set-up Short: Connect the DIR (AK4112B). (Default) Open: Separate the DIR. Supply clocks via Port1.
6	RX	S/PDIF's port set-up when CM0="L". TORX: Optical connector PORT2. (Default) BNC: BNC connector J2.
7	GND	Analog ground and digital ground Open: separated (Default). Short: connected (The connector "DGND" can be open.).
8	D-A	Power supply source set-up for digital section of AKD4705-A. Open: from the "D5V" Jack. Short: from the regulator or the "+5V" Jack. Don't connect anything to the "D5V" Jack. (Default)
9	REG	Power supply source set-up for VD of AK4705. Open: from the "+5V" Jack. Short: from the regulator. Don't connect anything the "+5V" Jack. (Default)
10	VVD1	Power supply source set-up for VVD1 of AK4705. Open: from the "VVD1" Jack. Short: from the regulator or the "+5V" Jack. Don't connect anything to the "VVD1" Jack. (Default)
11	VVD2	Power supply source set-up for VVD1 of AK4705. Open: from the "VVD2" Jack. Short: from the regulator or the "+5V" Jack. Don't connect anything to the "VVD2" Jack. (Default)
12	VCRRC	Input Selection for VCRRC "I" side: Input to VCRRC from VCRRC jack. (Default) "I/O" side: Input to VCRC from VCRC jack. (Note: Refer CIO bit of AK4705)

Table 5. Jumper list

■ Serial Control

The AK4705-A can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT3 (µP-IF) with PC by 10 wire flat cable packed with the AKD4705-A.

Be careful connector direction. Flat cable should be connected 10-pin header, red line put on 10pin header 5 and 6 pin.

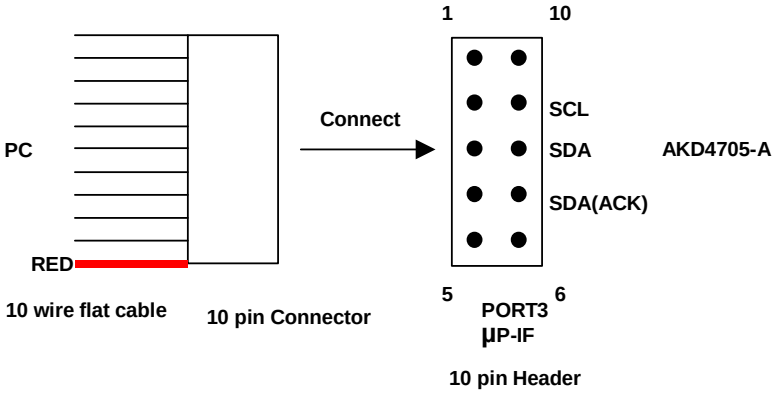


Figure 2. Connection of 10 pin flat cable for PORT3

■ Input/Output port List

		Signal Name	Notes
Audio	Input	J5 (VCRINL), J3 (VCRINR), J9 (TVINL), J8 (TVINR)	Max: 2Vrms
	Output	J12 (VCROUTL), J10 (VCROUTR), J6 (TVOUTL), J7 (TVOUTR), J4 (MONOOUT)	Max: 3Vrm
Digital	Input	Port2 (TORX176) or J2 BNC (RX)	Max: D5V+0.3V
Video	Input	J13 (ENCB), J15 (ENCG), J17 (ENCRC), J19 (ENCC), J21 (ENCV), J23(ENCY), J25(TVVIN), J14(VCRVIN), J18(VCRRC; Note), J20(VCRG), J22(VCRB)	Max: 1.5Vp-p
	Output	J27 (VCRCOUT; Note), J29 (TVVOUT), J30 (TVRC), J31 (TVG), J32 (TVB), J33 (RFV), J34 (VCRVOUT)	Max: 3Vp-p
Slow Blanking	Input	J24 (VCRSB)	Max: VP+0.3V
	Output	J24 (VCRSB) , J28 (TVSB)	Max: VP
Fast Blanking	Input	J16 (VCRFB)	Max: VVD1+0.3V
	Output	J26 (TVFB)	Max: VVD2

Note: Refer JP12 and CIO bit of the AK4705.

Table 6. Input/Output port List

■ The indication content for LED

LED turns on during each output is “H”.

[LE1] Indicates unlock or parity error of S/PDIF. Connected to the ERF pin of DIR (AK4112B). (Normally off.)

[LE2] Indicates the validity status of S/PDIF. Connected to the V pin of DIR (AK4112B). (Normally off.)

■ Toggle switch (SW1 on board) operation

“H”: AK4705 is active.

“L”: AK4705 is powered down.

(Note: When the power of AKD4705-A is ON at first, SW1 should be switched from “L” to “H”.)

4) Control Software Manual

■ Set-up of evaluation board and control software

1. Set up the AKD4705-A according to previous term.

2. Connect IBM-AT compatible PC with AKD4705-A by 10-line type flat cable (packed with AKD4705-A). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer “Installation Manual of Control Software Driver by AKM device control software”. In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)

3. Insert the CD-ROM labeled “AK4705 Evaluation Kit” into the CD-ROM drive.

4. Access the CD-ROM drive and double-click the icon of “akd4705.exe” to set up the control program.

5. Then please evaluate according to the follows.

■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click “Port Reset” button.
3. Click “Write default” button

■ Explanation of each buttons

1. [Port Reset]: Set up the USB interface board (AKDUSBIF-A) when using the board.
2. [Write default]: Initialize the register of AK4705.
3. [All Write]: Write all registers that is currently displayed.
4. [Function1]: Dialog to write data by keyboard operation.
5. [Function2]: Dialog to write data by keyboard operation.
6. [Function3]: The sequence of register setting can be set and executed.
7. [Function4]: The sequence that is created on [Function3] can be assigned to buttons and executed.
8. [Function5]: The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed.
9. [SAVE]: Save the current register setting.
10. [OPEN]: Write the saved values to all register.
11. [Write]: Dialog to write data by mouse operation.

■ Indication of data

Input data is indicated on the register map. Red letter indicates “H” or “1” and blue one indicates “L” or “0”. Blank is the part that is not defined in the datasheet.

■ Explanation of each dialog

1. [Write Dialog]: Dialog to write data by mouse operation

There are dialogs corresponding to each register.

Click the [Write] button corresponding to each register to set up the dialog. If you check the check box, data becomes "H" or "1". If not, "L" or "0".

If you want to write the input data to the AK4705, click [OK] button. If not, click [Cancel] button.

2. [Function1 Dialog] : Dialog to write data by keyboard operation

Address Box: Input registers address in 2 figures of hexadecimal.
Data Box: Input registers data in 2 figures of hexadecimal.

If you want to write the input data to the AK4705, click [OK] button. If not, click [Cancel] button.

3. [Function2 Dialog] : Dialog to evaluate DATT

There are dialogs corresponding to register of 02h.

Address Box: Input registers address in 2 figures of hexadecimal.
Start Data Box: Input starts data in 2 figures of hexadecimal.
End Data Box: Input end data in 2 figures of hexadecimal.
Interval Box: Data is written to AK4705 by this interval.
Step Box: Data changes by this step.
Mode Select Box:

If you check this check box, data reaches end data, and returns to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09 09 08 07 06 05 04 03 02 01 00

If you do not check this check box, data reaches end data, but does not return to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09

If you want to write the input data to the AK4705, click [OK] button. If not, click [Cancel] button.

4. [SAVE] and [OPEN]

4-1. [SAVE]

All of current register setting values displayed on the main window are saved to the file. The extension of file name is “akr”.

<Operation flow>
(1) Click [SAVE] Button.
(2) Set the file name and click [SAVE] Button. The extension of file name is “akr”.

4-2. [OPEN]

The register setting values saved by [SAVE] are written to the AK4705. The file type is the same as [SAVE].

<Operation flow>
(1) Click [OPEN] Button.
(2) Select the file (*.akr) and Click [OPEN] Button.

5. [Function3 Dialog]

The sequence of register setting can be set and executed.

(1) Click [F3] Button. The following is displayed.

(2) Set the control sequence.
Set the address, Data and Interval time. Set “-1” to the address of the step where the sequence should be paused.

(3) Click [START] button. Then this sequence is executed.

The sequence is paused at the step of Interval="-1". Click [START] button, the sequence restarts from the paused step.

This sequence can be saved and opened by [SAVE] and [OPEN] button on the Function3 window. The extension of file name is “aks”.

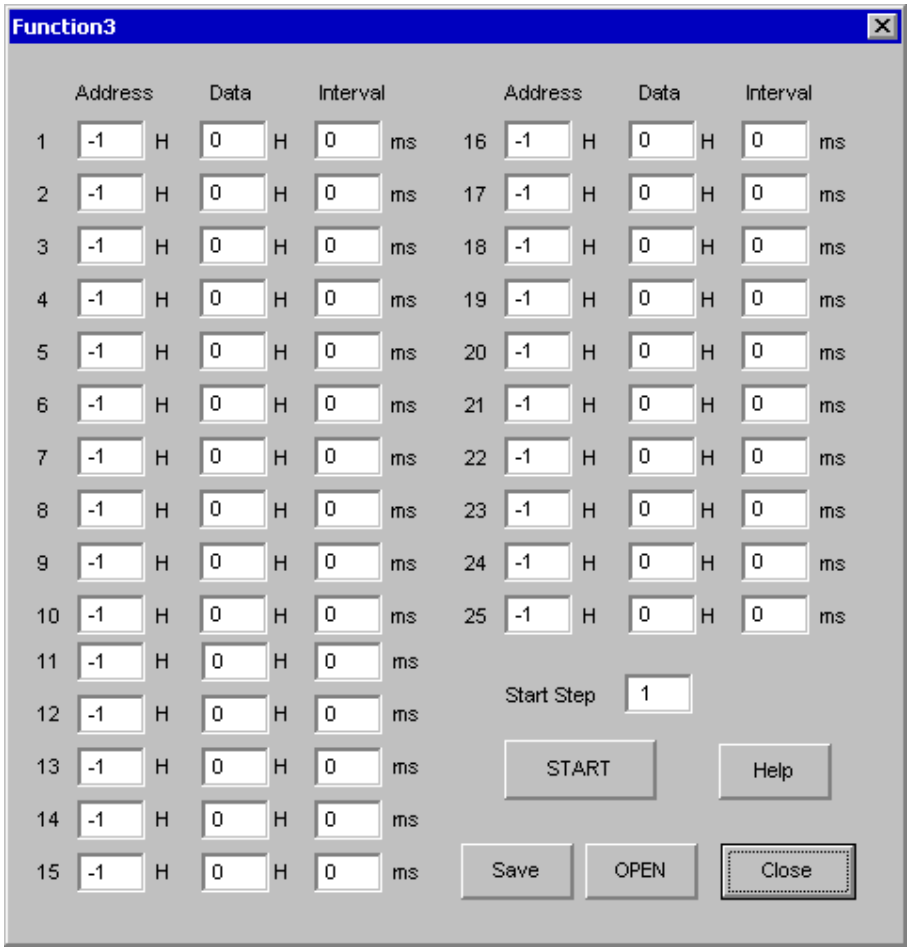


Figure 1. Window of [F3]

6. [Function4 Dialog]

The sequence file (*.aks) saved by [Function3] can be listed up to 10 files, assigned to buttons and then executed. When [F4] button is clicked, the window as shown in Figure 2 opens.

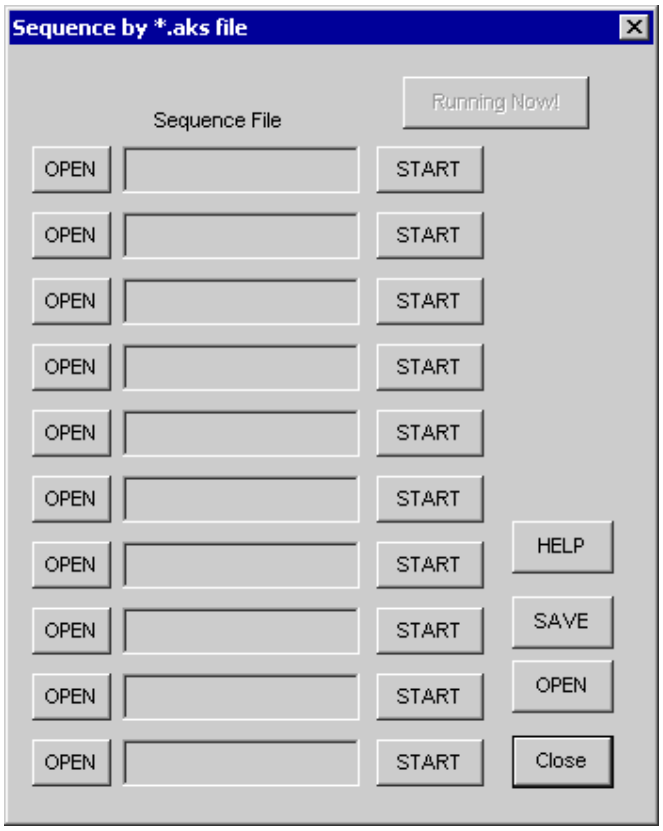


Figure 2. [F4] window

6-1. [OPEN] buttons on left side and [START] buttons

(1) Click [OPEN] button and select the sequence file (*.aks) saved by [Function3].

The sequence file name is displayed as shown in Figure 3. (In case that the selected sequence file name is "DAC_Stereo_ON.aks")

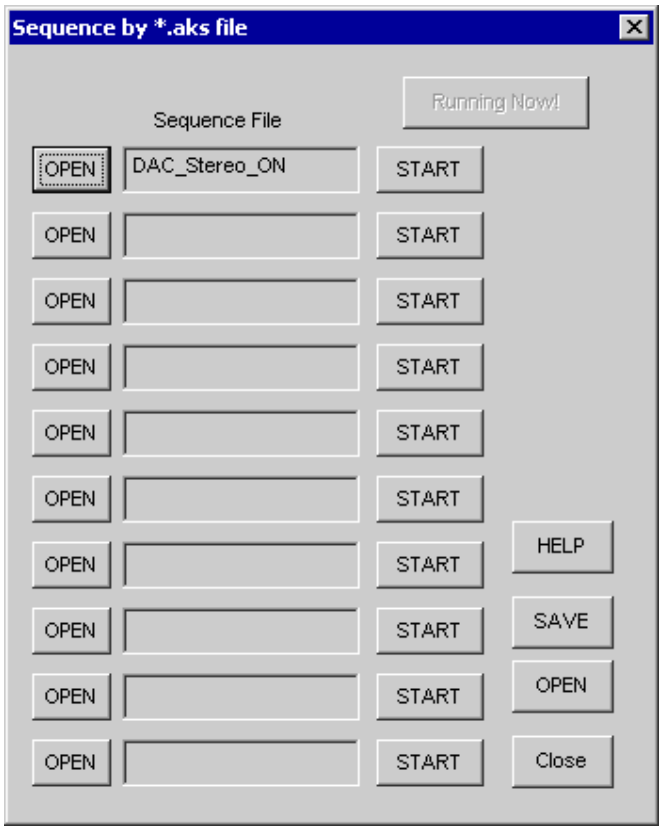


Figure 3. [F4] window(2)

(2) Click [START] button, then the sequence is executed.

6-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The name assign of sequence file displayed on [Function4] window can be saved to the file. The file name is "*.ak4".

[OPEN] : The name assign of sequence file(*.ak4) saved by [SAVE] is loaded.

6-3. Note

(1) This function doesn't support the pause function of sequence function.

(2) All files used by [SAVE] and [OPEN] function on right side need to be in the same folder.

(3) When the sequence is changed in [Function3], the sequence file (*.aks) should be loaded again in order to reflect the change.

7. [Function5 Dialog]

The register setting file(*.akr) saved by [SAVE] function on main window can be listed up to 10 files, assigned to buttons and then executed. When [F5] button is clicked, the window as shown in Figure 4 opens.

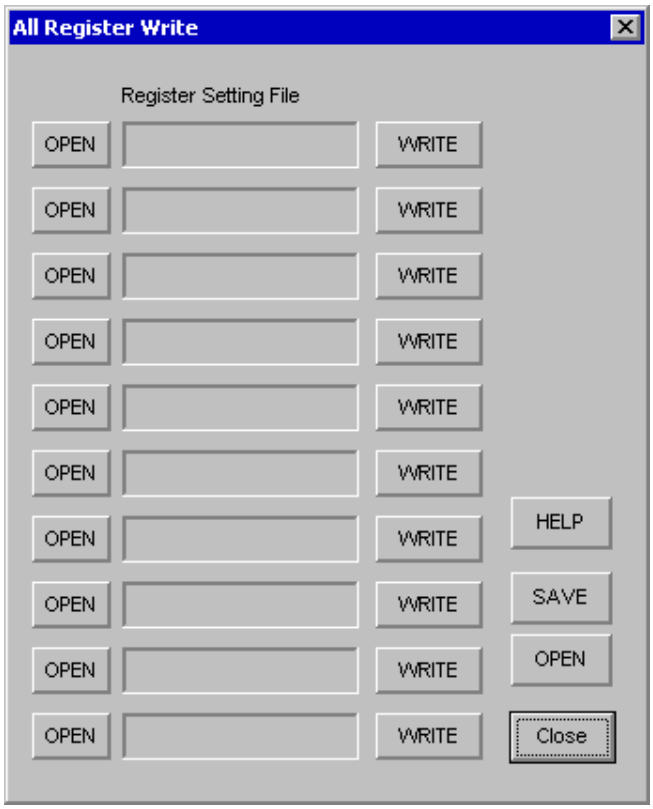


Figure 4. [F5] window

7-1. [OPEN] buttons on left side and [WRITE] button

(1) Click [OPEN] button and select the register setting file (*.akr).

The register setting file name is displayed as shown in Figure 5. (In case that the selected file name is "DAC_Output.akr")

(2) Click [WRITE] button, then the register setting is executed.

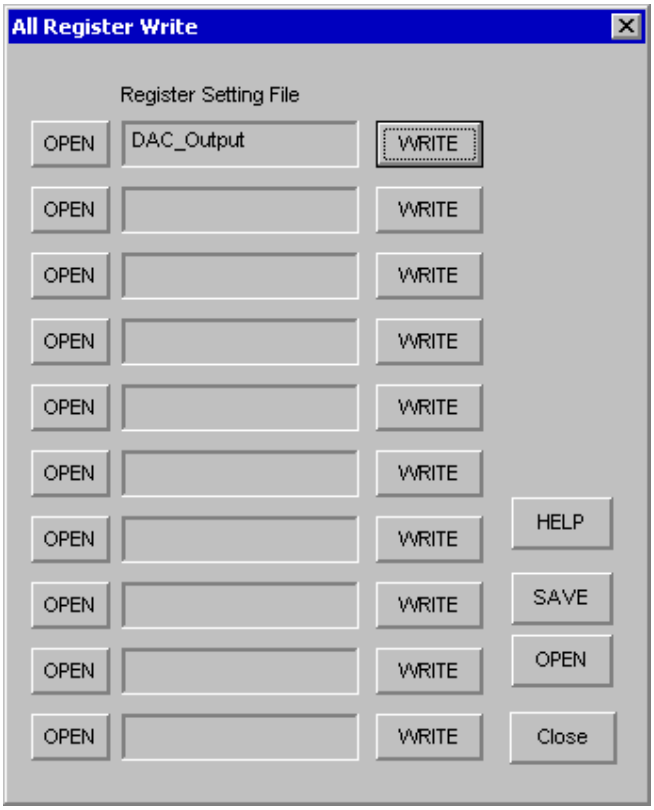


Figure 5. [F5] windows(2)

7-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The name assign of register setting file displayed on [Function5] window can be saved to the file. The file name is "*.ak5".
[OPEN] : The name assign of register setting file(*.ak5) saved by [SAVE] is loaded.

7-3. Note

(1) All files used by [SAVE] and [OPEN] function on right side need to be in the same folder.

(2) When the register setting is changed by [SAVE] Button on the main window, the register setting file (*.akr) should be loaded again in order to reflect the change.

MEASUREMENT RESULTS

■ Audio

[Measurement condition]

- Measurement unit: Audio Precision System two Cascade
- MCLK : 256fs
- BICK : 64fs
- fs : 48kHz
- BW : 10Hz~20kHz
- Bit : 18bit
- Power Supply : VD=5V, VDD1=5V, VDD2=5V, VP=12V
- Interface : DIR
- Temperature : Room
- Volume#0=Volume#1=0dB
- Measurement signal line path: DAC → Volume#0 → Volume#1 → TVOUTL/R

Parameter	Input signal	Measurement filter	Results [dB]
S/(N+D) at 2Vrms Output	1kHz, 0dBFS	20kLPF	93.3
DR	1kHz, -60dBFS	22kLPF, A-weighted	96.8
S/N	"0" data	22kLPF, A-weighted	97.0

Plots

Figure 1-1. FFT (1kHz, 0dBFS input) at 2Vrms output
Figure 1-2. FFT (1kHz, -60dBFS input)
Figure 1-3. FFT (Noise floor)
Figure 1-4. FFT (Out-of band noise)
Figure 1-5. THD+N vs. Input Level (fin=1kHz)
Figure 1-6. THD+N vs. fin (Input Level=0dBFS)
Figure 1-7. Linearity (fin=1kHz)
Figure 1-8. Frequency Response (Input Level=0dBFS)
Figure 1-9. Crosstalk (Input Level=0dBFS)

■ Video

[Measurement condition]

- Signal Generator : Sony Tectonics TG2000
- Measurement unit: Sony Tectonics VM700T
- Power Supply : VD=5V, VDD1=5V, VDD2=5V, VP=12V
- Interface : BNC
- Temperature : Room
- Measurement signal line path: ENCV → TVVOUT, ENCRC → TVRC

Parameter	Measurement conditions	Results	Unit
S/N	Input = 0% flat field Filter = Uni-weighted, BW= 15kHz to 5MHz	73.1	dB
Crosstalk	Input = 100%red(ENCRC), Measured at TVVOUT	-58.9	dB
DG	Input = Modulated Lamp	0.67	%
DP	Input = Modulated Lamp	0.83	deg.

Plots

Figure 2-1. Noise spectrum (Input=0%flat field, BW=15kHz to 5MHz, uni weighted)
Figure 2-3 Crosstalk (Input= 100% red (ENCRC), measured at TVVOUT)
Figure 2-4 DG, DP (Input= Modulated Lamp)

Plots (Audio)

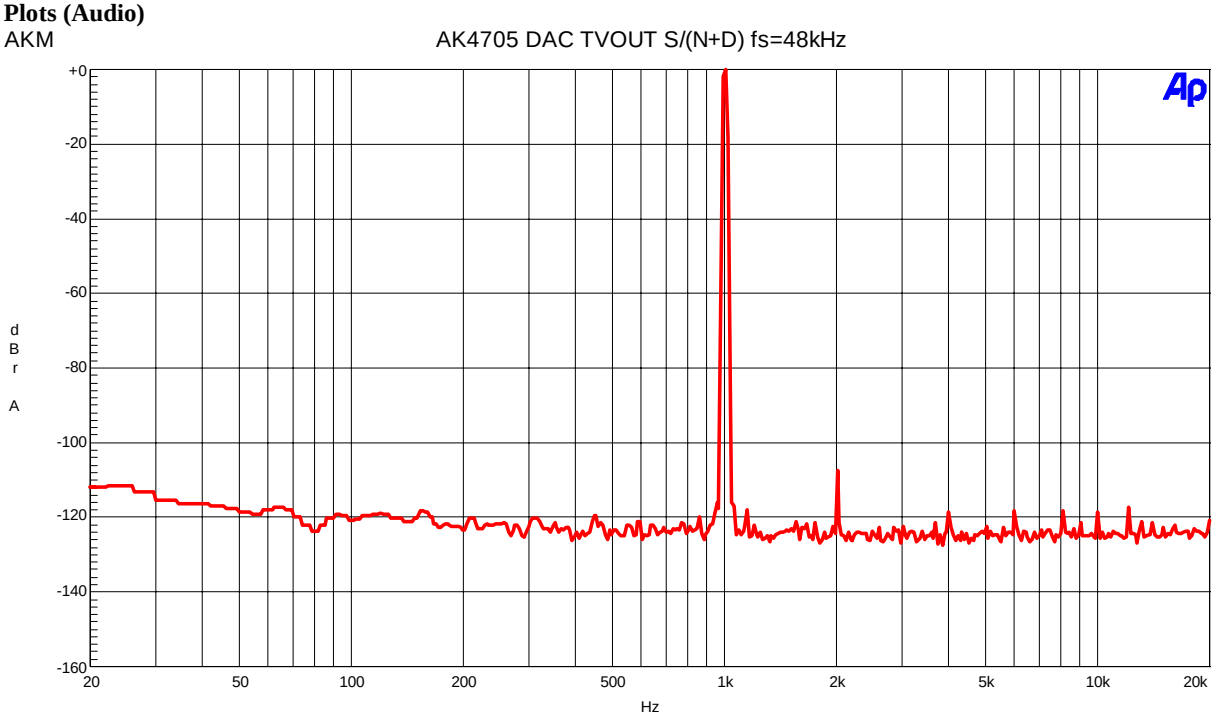


Figure1-1. FFT (fin=1kHz Input Level=0dBFS)

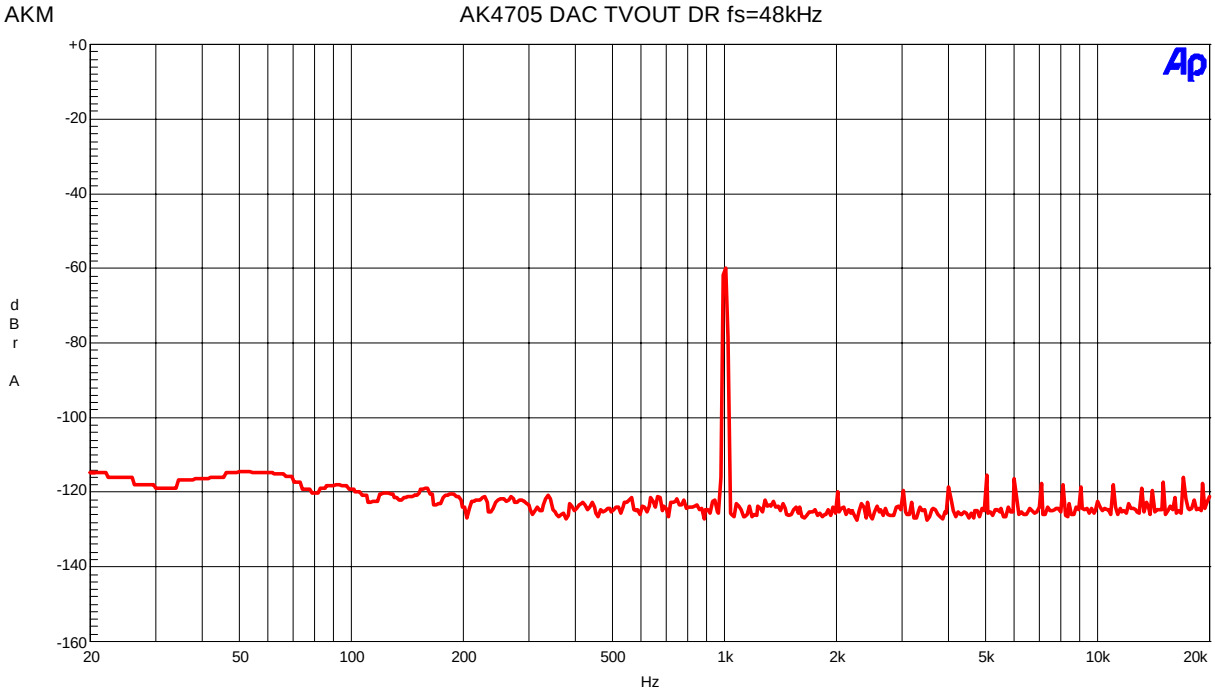


Figure-1-2. FFT (fin=1kHz Input Level=-60dBFS)

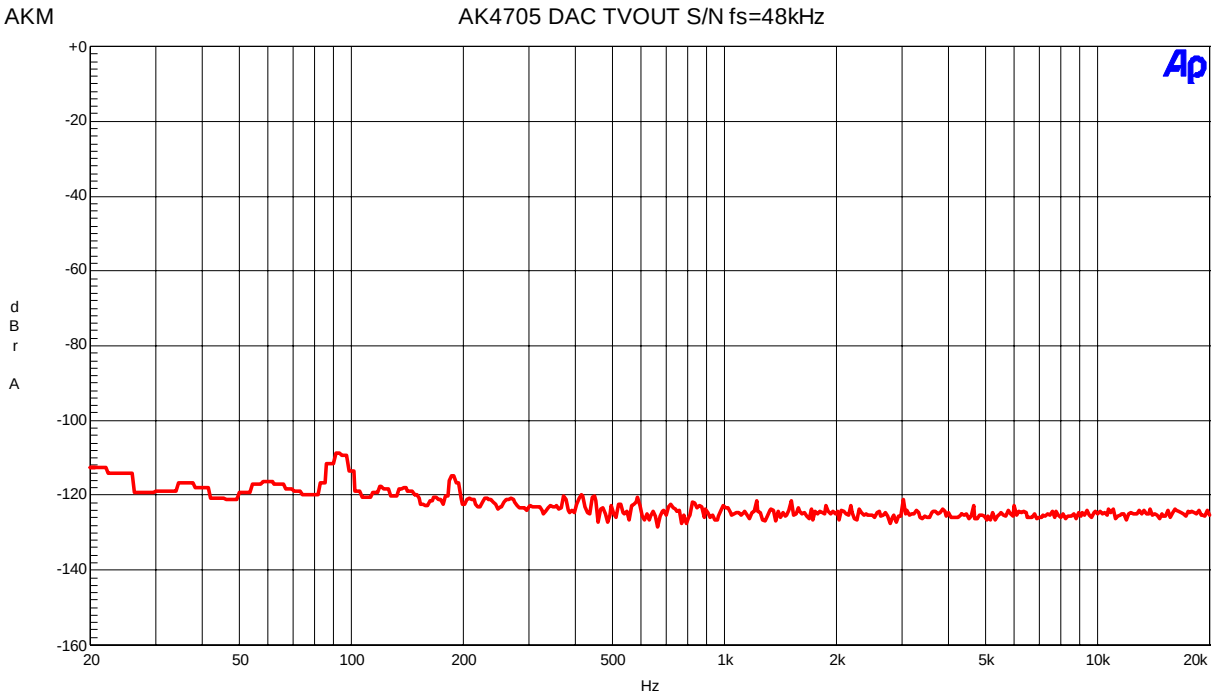


Figure1-3. FFT (Noise Floor)

Figure1-4. FFT (Outband Noise)

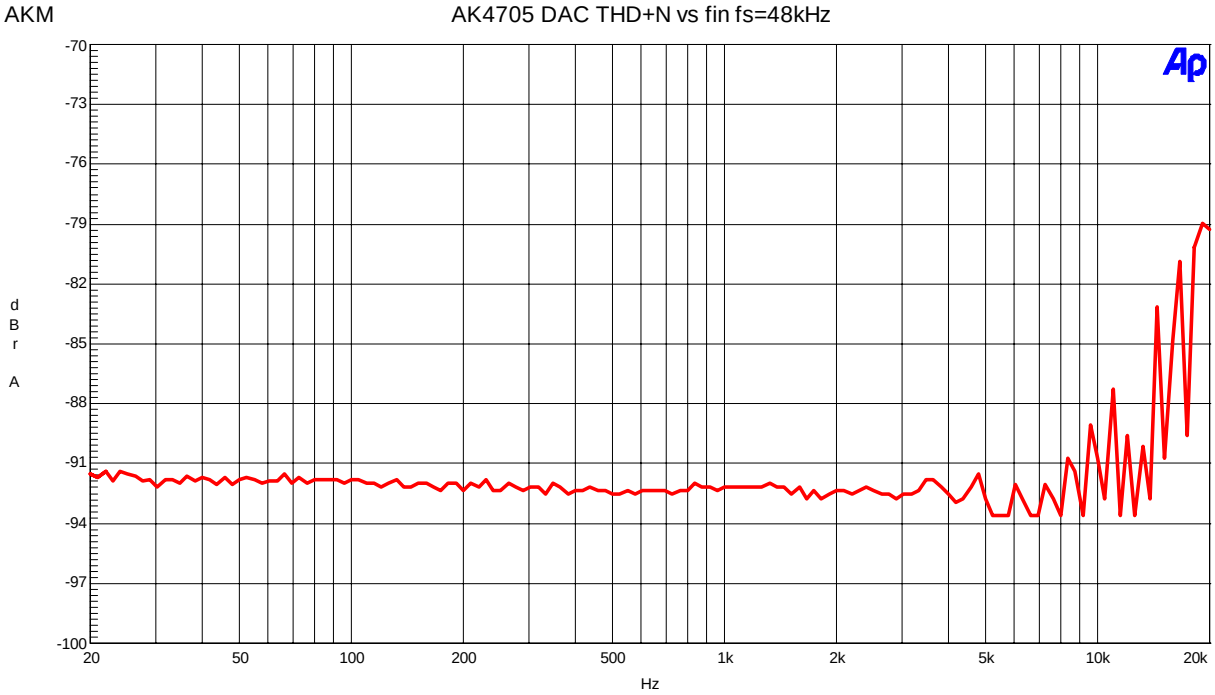


Figure1-5. THD+N vs. Input level (fin=1kHz)

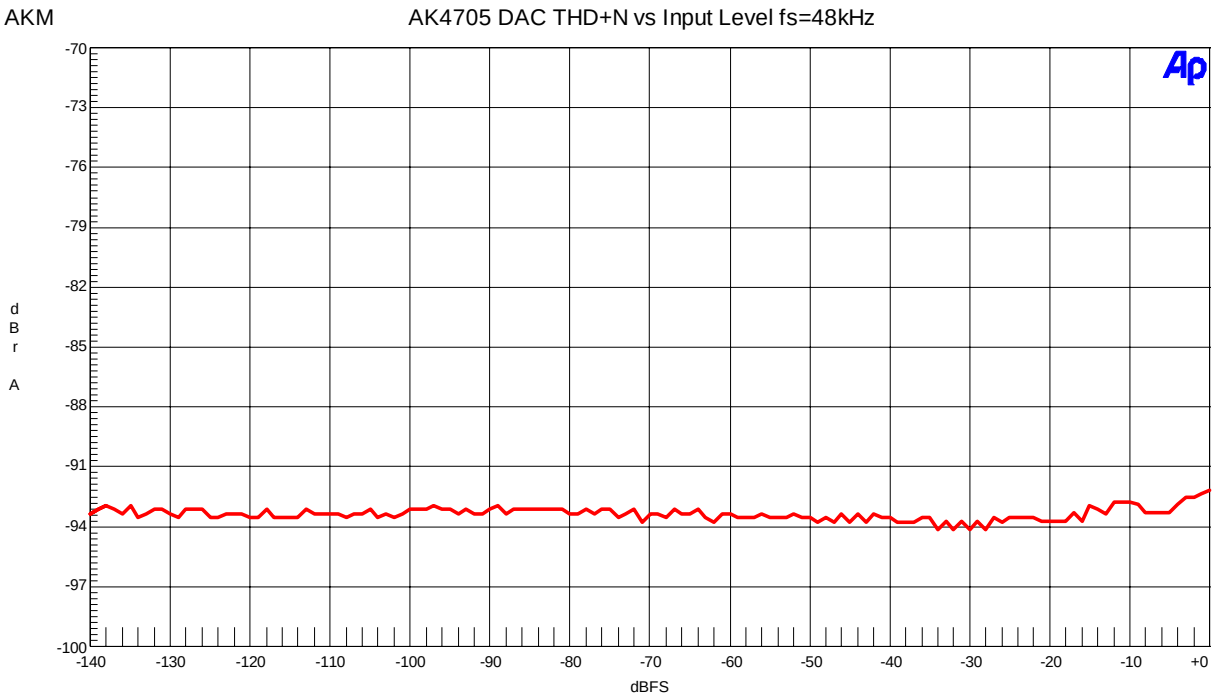


Figure1-6. THD+N vs. Input Frequency (Input level=0dBFS)

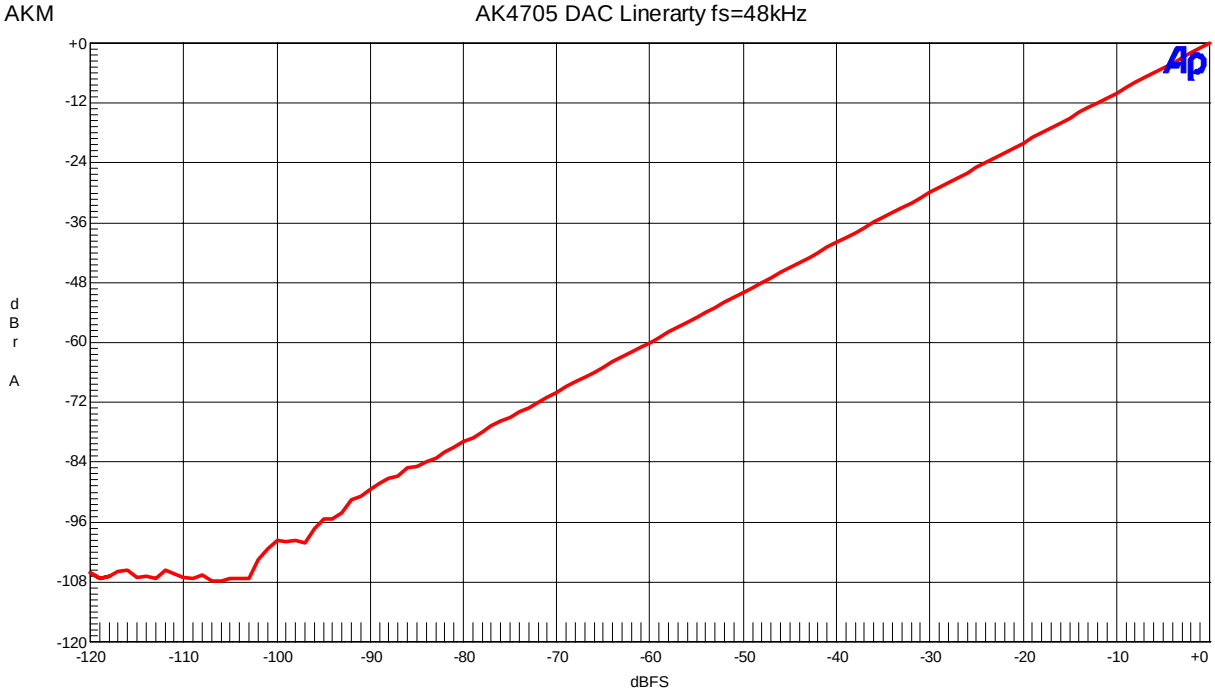


Figure1-7.Linearity (fin=1kHz)

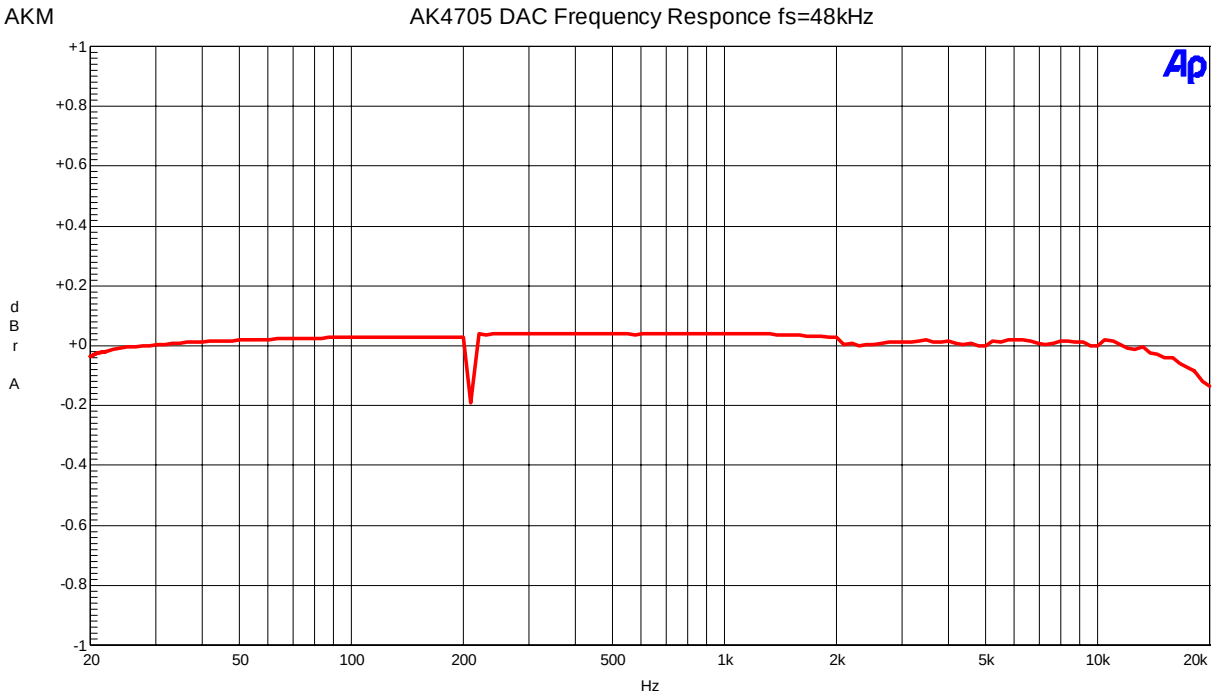


Figure1-8. Frequency Response (Input level=0dBFS)

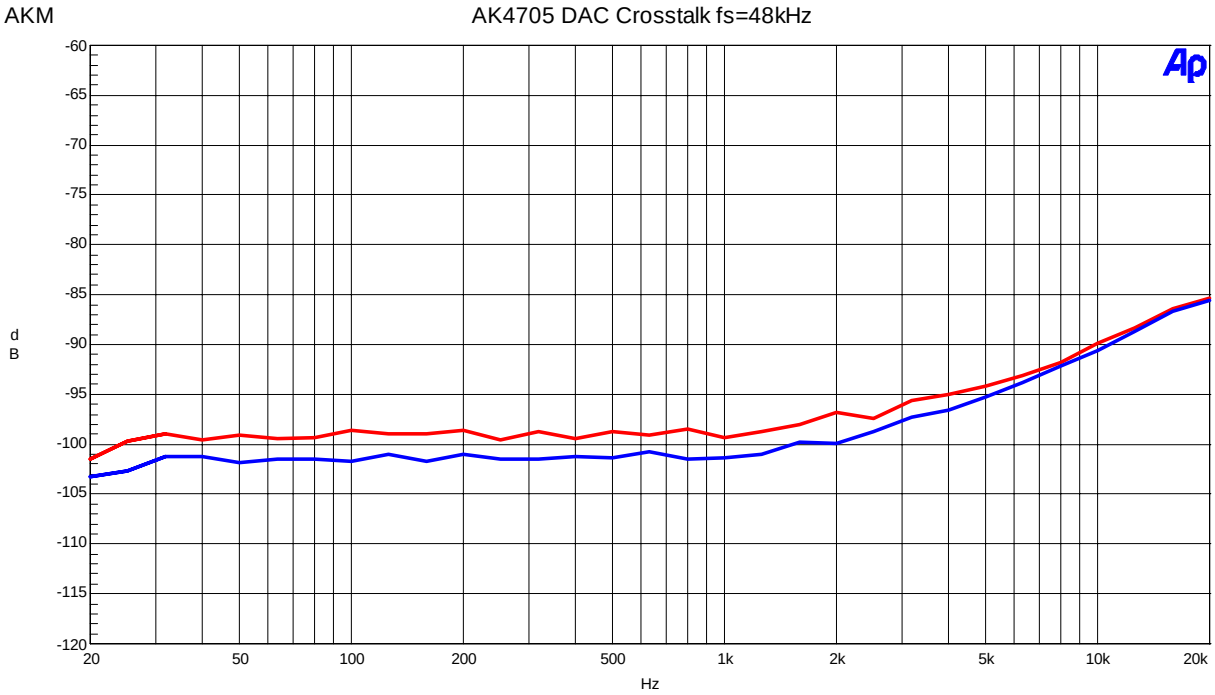


Figure1-9. Crosstalk (Input level=0dBFS)

Plots(Video)

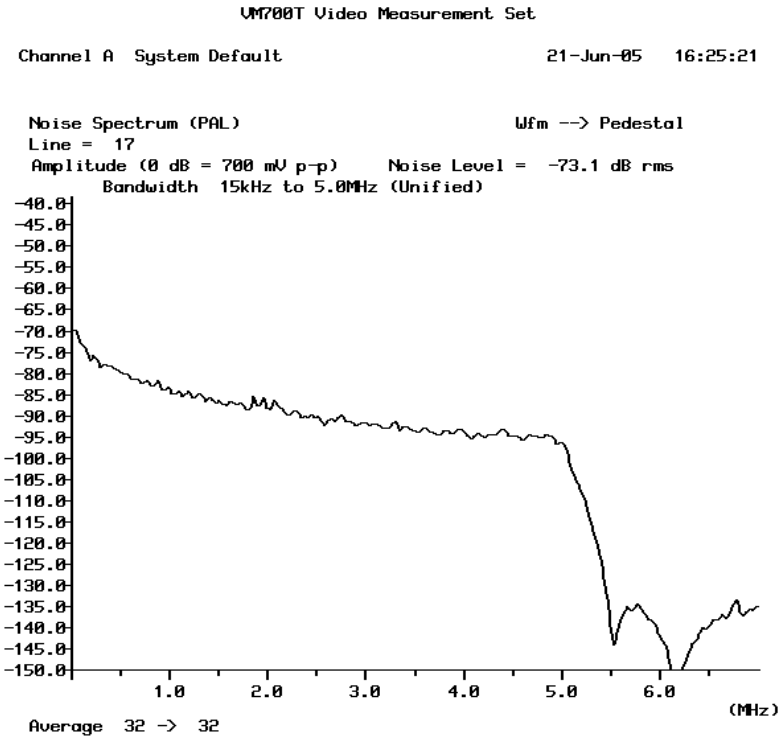


Figure 2-1. Noise spectrum (Input=0%flat field, BW=15kHz to 5MHz, uni weighted)

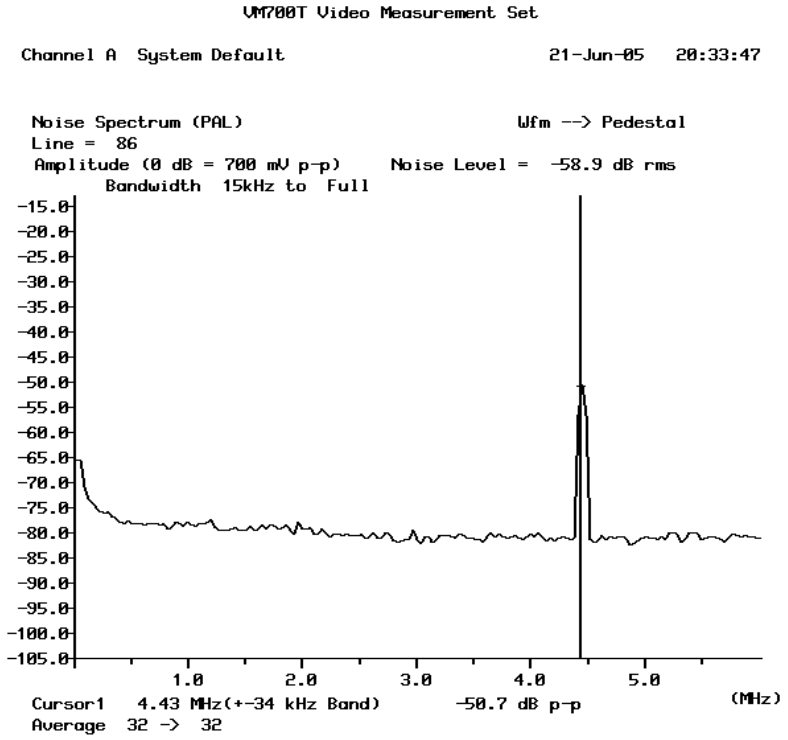


Figure 2-3 Crosstalk (Input= 100% red (ENCRC), measured at TVVOUT)

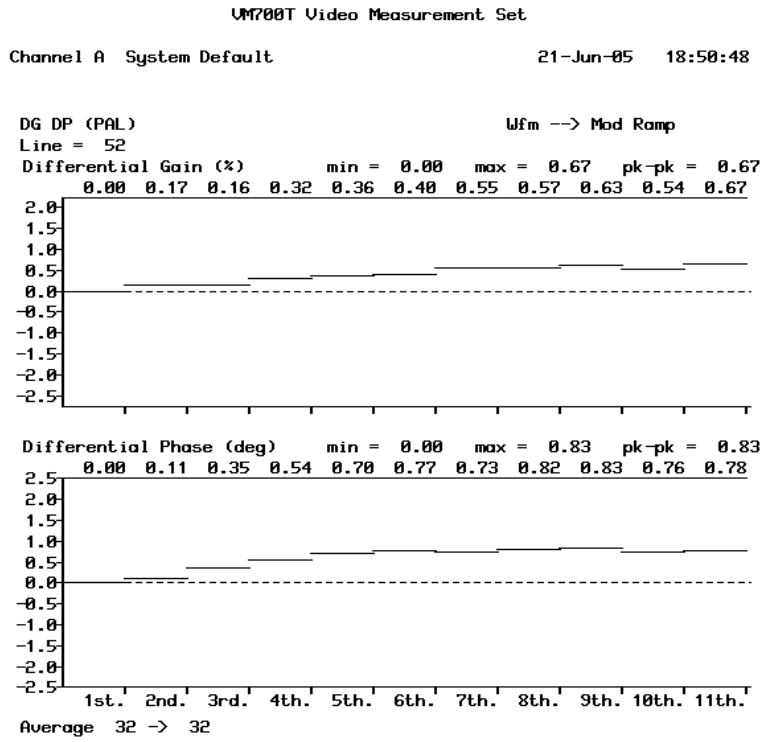


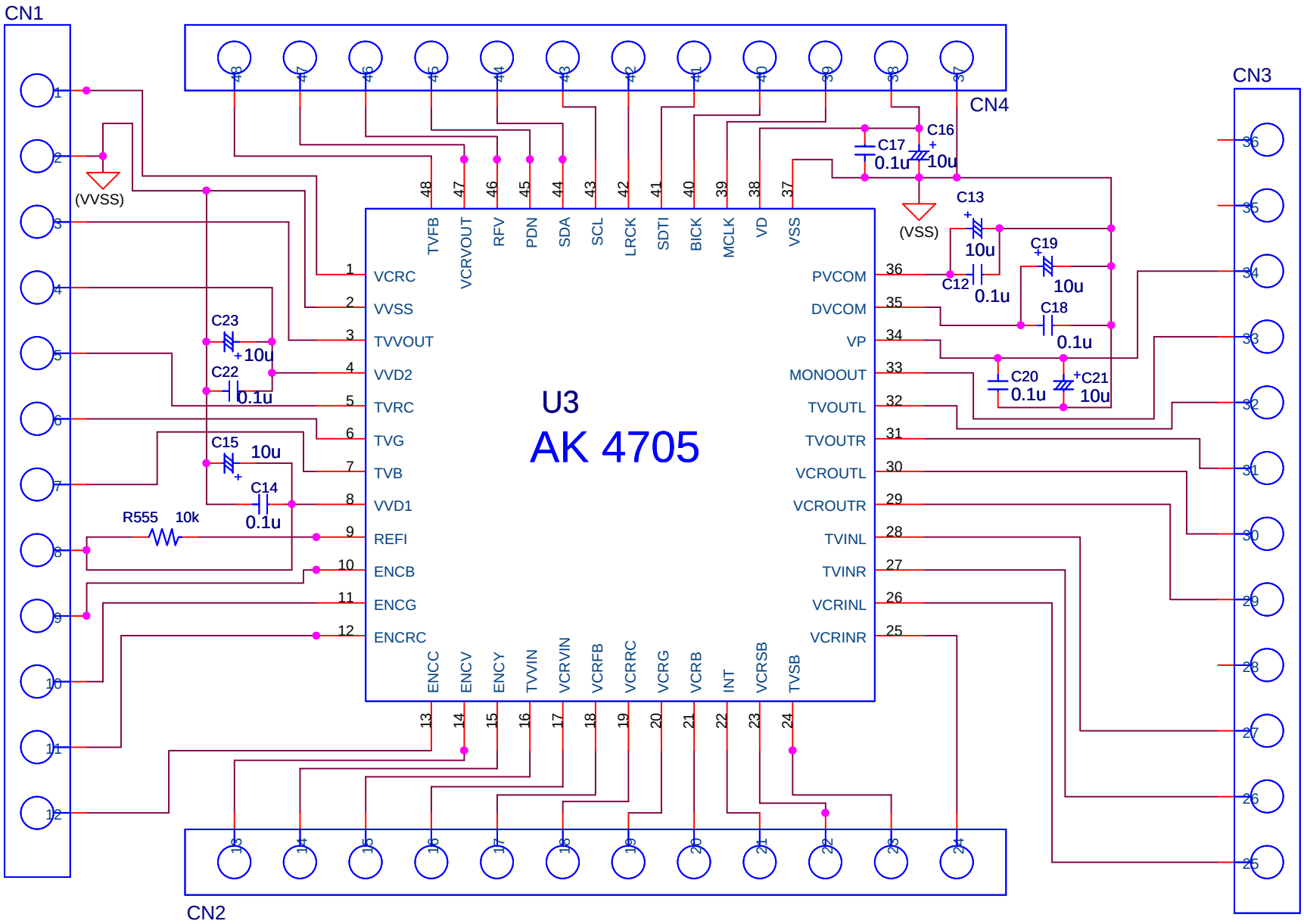
Figure 2-4 DG, DP (Input= Modulated Lamp)

Revision History

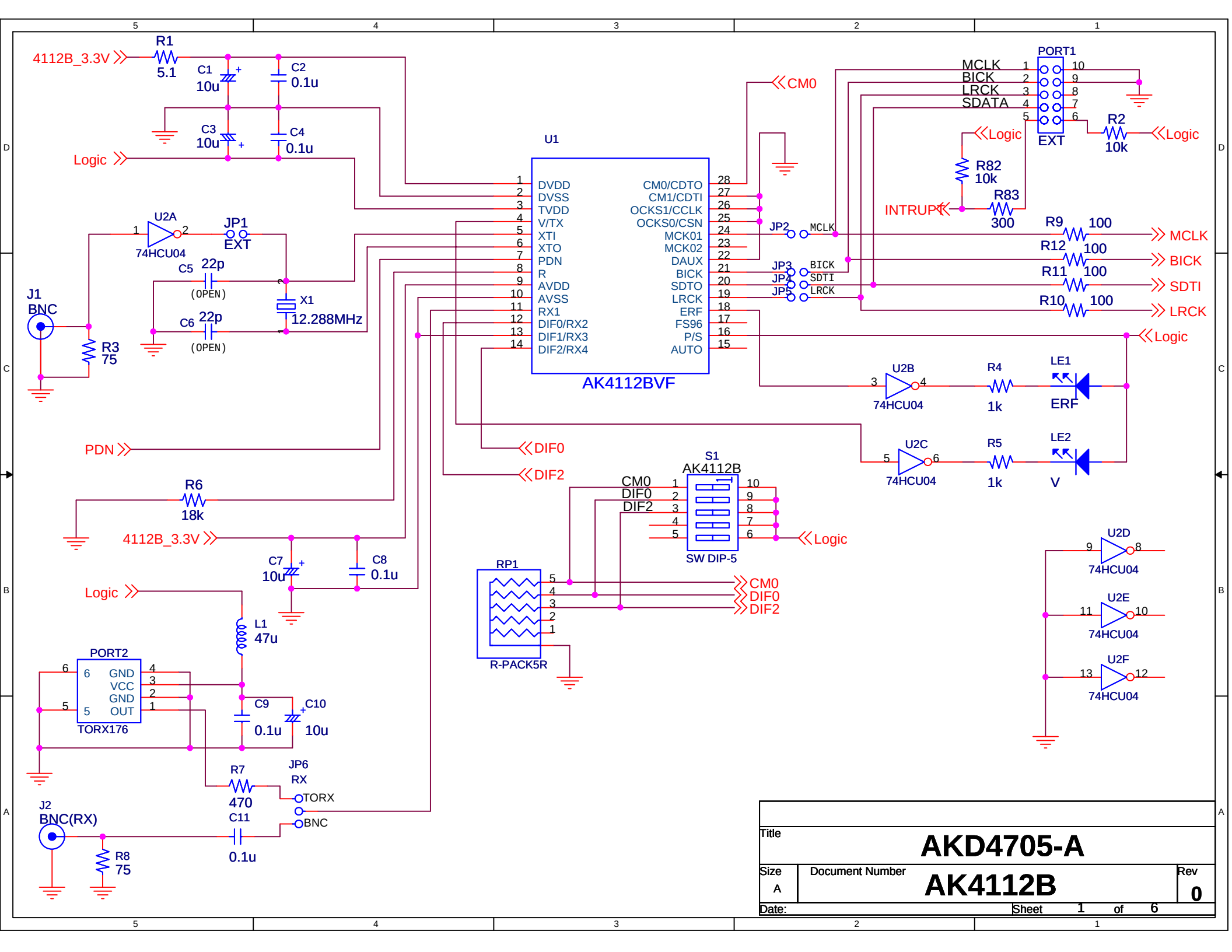
Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents
05/09/27	KM078600	0	First Edition	
06/08/30	KM078601	0	Modification	P1. Title: Evaluation board Rev.0 for AK4705 → AK4705 Evaluation Board Rev.0
			Comment addition	P3. 1)-1 DIP switch set-up: Table1 Add (Note) AK4112B: DIF1="L" Add "Default " P4. Notes 4. 24bit I2S → 24bit I2S (Default)
			Modification	P4. Note3, Note4: Delete the check mark of MUTE, STBY
			Comment addition	P5-P7. JP1 (EXT), JP2 (MCLK), JP3 (BICK), JP4 (SDTI), JP5 (LRCK), JP7 (GND): Add "Short", "Open", "Default " JP6 (RX): Add "TORX", "BNC", "Default " JP12 (VCRRC): Add "I", "I/O", "Default "
			Error Correct	P8. DIP-switch (S1) List: Switch Name: DIF0, Default: OFF→ON Switch Name: DIF2: Default: OFF→ON P8. Jumper List: No.1: EXT Short: X'tal (default)→ Open: X'tal (Default) Open: External clock via BNC (J1)→ Short: External clock via BNC (J1) No.8: D-A Open: from the "D-5V" Jack.(default) → Open: from the "D-5V" Jack. No.12: VCRRC "I" side: Input to VCRRC from VCRRC jack→ "I" side: Input to VCRRC from VCRRC jack (Default) P25. Figure 2-3. Y/C Crosstalk: Plot Correct

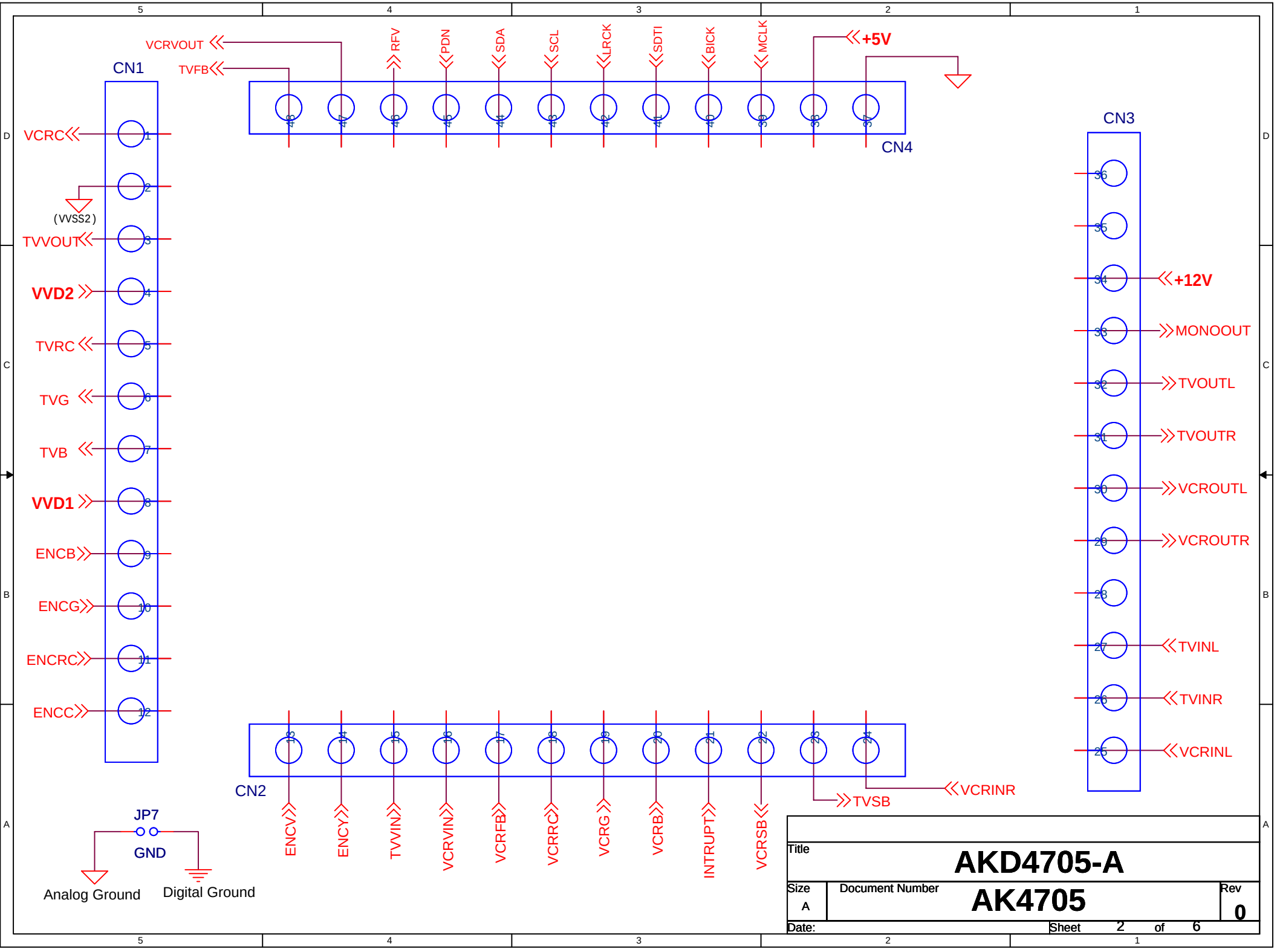
IMPORTANT NOTICE

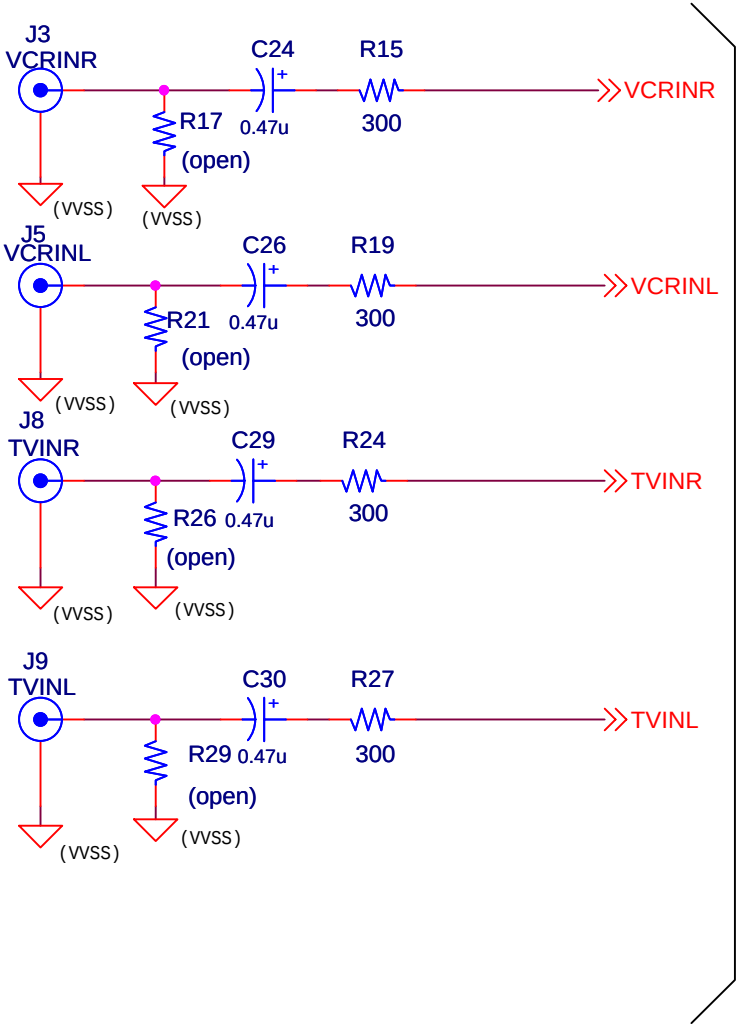
- These products and their specifications are subject to change without notice. Before considering any use or application, consult the Asahi Kasei Microsystems Co., Ltd. (AKM) sales office or authorized distributor concerning their current status.
- AKM assumes no liability for infringement of any patent, intellectual property, or other right in the application or use of any information contained herein.
- Any export of these products, or devices or systems containing them, may require an export license or other official approval under the law and regulations of the country of export pertaining to customs and tariffs, currency exchange, or strategic materials.
- AKM products are neither intended nor authorized for use as critical components in any safety, life support, or other hazard related device or system, and AKM assumes no responsibility relating to any such use, except with the express written consent of the Representative Director of AKM. As used here:
  (a) A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
  (b) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
- It is the responsibility of the buyer or distributor of an AKM product who distributes, disposes of, or otherwise places the product with a third party to notify that party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKM harmless from any and all claims arising from the use of said product in the absence of such notification.



Title	AKD4705-A-48LQFP		
Size A	Document Number AK4705		Rev 0
Date:		Sheet 1 of 1	

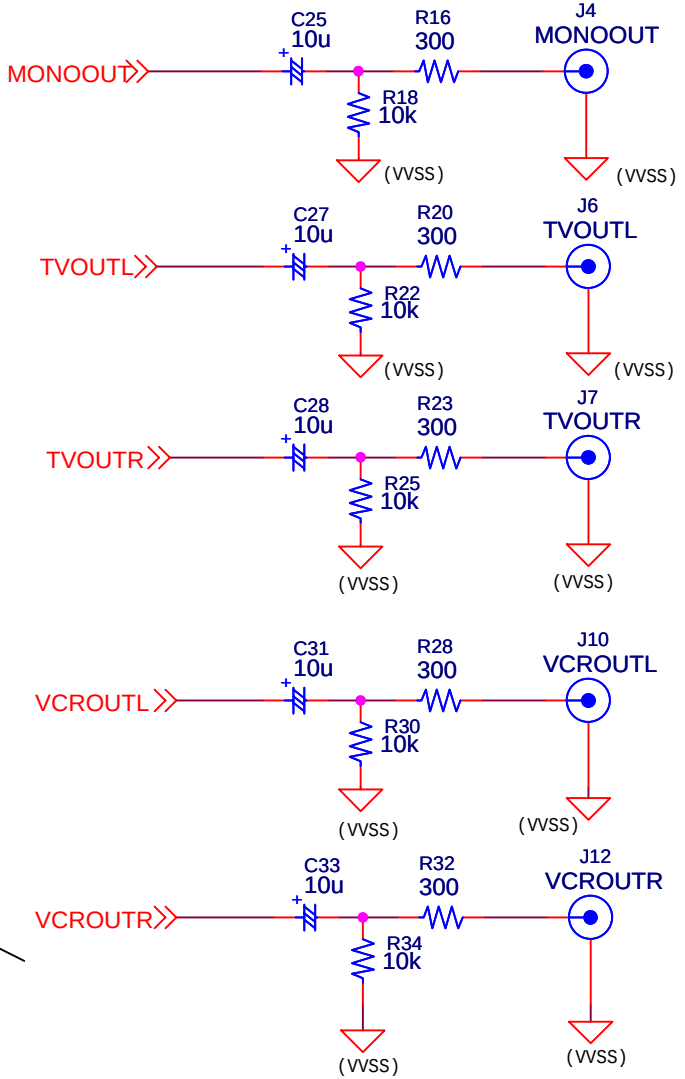

4112B_3.3V
R1
5.1
C1
10u
C2
0.1u
C3
10u
C4
0.1u
Logic
U1
AK4112BVF
DVDD
DVSS
TVDD
V/TX
XTI
XTO
PDN
R
AVDD
AVSS
RX1
DIF0/RX2
DIF1/RX3
DIF2/RX4
CM0/CDTO
CM1/CDTI
OCKS1/CCLK
OCKS0/CSN
MCK01
MCK02
DAUX
BICK
SDTO
LRCK
ERF
FS96
P/S
AUTO
CM0
PORT1
MCLK
BICK
LRCK
SDATA
EXT
R2
10k
Logic
R82
10k
INTRUP
R83
300
U2A
74HCU04
JP1
EXT
C5
22p
(OPEN)
C6
22p
(OPEN)
X1
12.288MHz
J1
BNC
R3
75
JP2
JP3
JP4
JP5
MCLK
BICK
SDTI
LRCK
R9
100
R12
100
R11
100
R10
100
MCLK
BICK
SDTI
LRCK
U2B
74HCU04
R4
1k
LE1
ERF
U2C
74HCU04
R5
1k
LE2
V
PDN
DIF0
DIF2
R6
18k
4112B_3.3V
C7
10u
C8
0.1u
Logic
S1
AK4112B
SW DIP-5
CM0
DIF0
DIF2
Logic
RP1
R-PACK5R
CM0
DIF0
DIF2
U2D
74HCU04
U2E
74HCU04
U2F
74HCU04
L1
47u
PORT2
GND
VCC
GND
OUT
TORX176
C9
0.1u
C10
10u
R7
470
JP6
RX
TORX
BNC
J2
BNC(RX)
C11
0.1u
R8
75
Title
AKD4705-A
Size
A
Document Number
AK4112B
Rev
0
Date:
Sheet
1
of
6


CN1
VCRC
(VVSS2)
TVVOUT
VVD2
TVRC
TVG
TVB
VVD1
ENCB
ENCG
ENCRC
ENCC
VCRVOUT
TVFB
RFV
PDN
SDA
SCL
LRCK
SDTI
BICK
MCLK
+5V
CN4
CN3
+12V
MONOOUT
TVOUTL
TVOUTR
VCROUTL
VCROUTR
TVINL
TVINR
VCRINL
CN2
ENCV
ENCY
TVVIN
VCRVIN
VCRFB
VCRRC
VCRG
VCRB
INTRUPT
VCRSB
TVSB
VCRINR
JP7
GND
Analog Ground
Digital Ground
Title
AKD4705-A
Size
A
Document Number
AK4705
Rev
0
Date:
Sheet 2 of 6

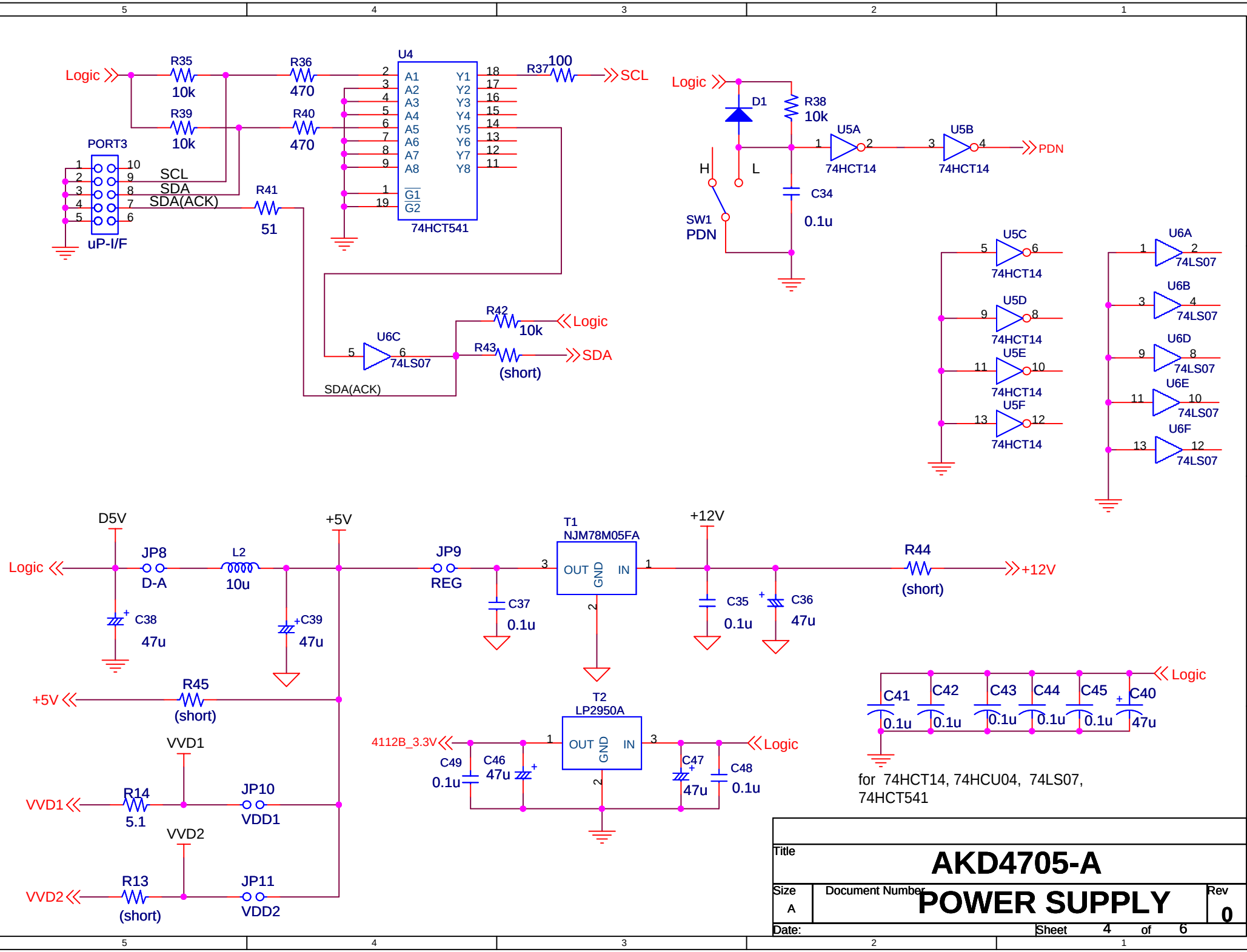


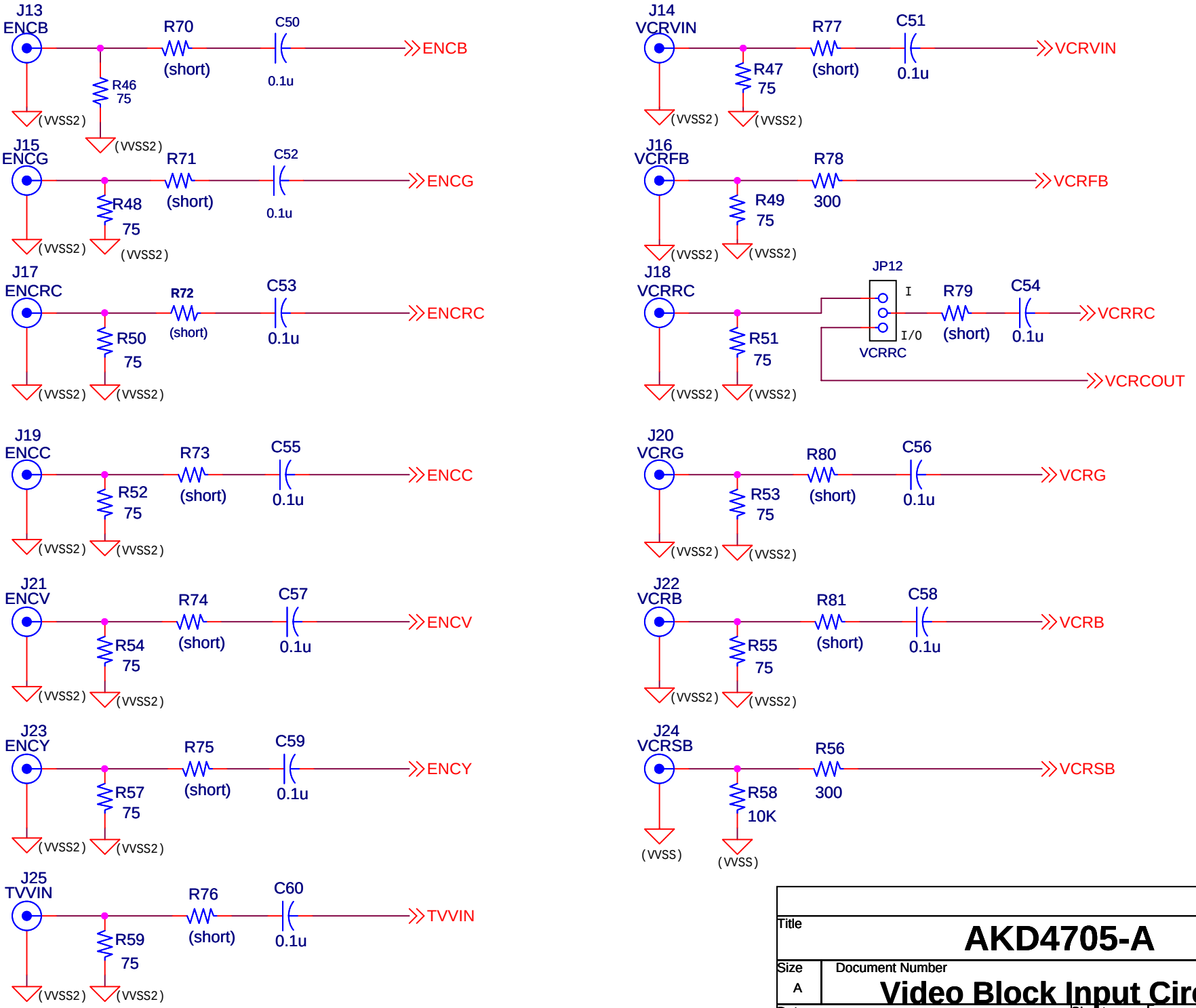
FOR Analog input

From Analog output

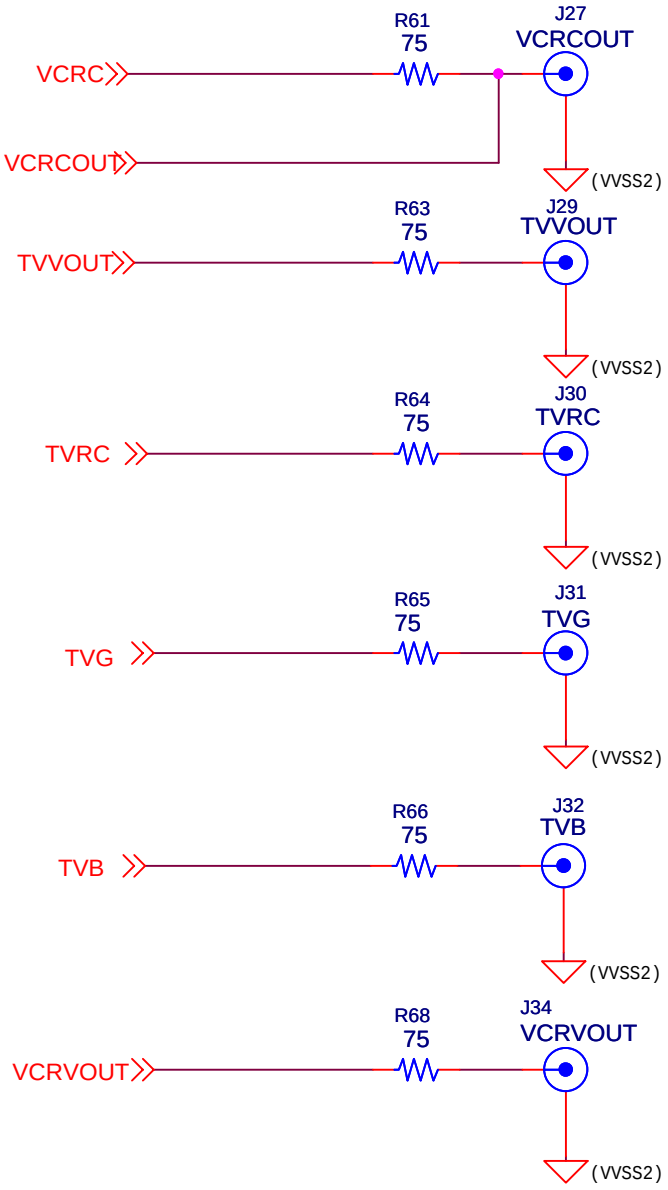


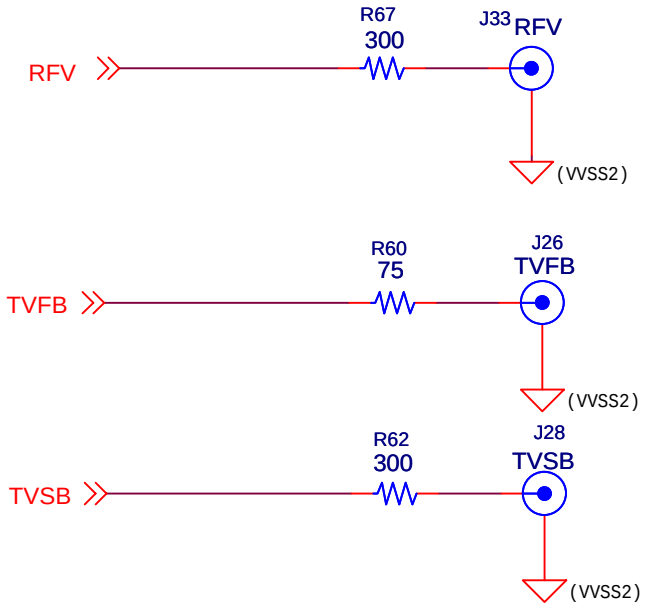
Title	**AKD4705-A**	
Size: A	Document Number: **Analog Input/Output Circuit**	Rev: 0
Date: Thursday, August 17, 2006	Sheet 3 of 6	


Logic
R35
10k
R36
470
R37
100
SCL
R39
10k
R40
470
U4
74HCT541
PORT3
uP-I/F
SCL
SDA
SDA(ACK)
R41
51
R42
10k
R43
(short)
U6C
74LS07
SDA(ACK)
D1
R38
10k
U5A
U5B
74HCT14
PDN
H
L
SW1
PDN
C34
0.1u
U5C
U5D
U5E
U5F
74HCT14
U6A
U6B
U6D
U6E
U6F
74LS07
D5V
+5V
+12V
JP8
D-A
L2
10u
JP9
REG
T1
NJM78M05FA
OUT
GND
IN
C38
47u
+C39
47u
C37
0.1u
C35
0.1u
C36
47u
R44
(short)
+12V
R45
(short)
VVD1
R14
5.1
JP10
VDD1
VVD2
R13
(short)
JP11
VDD2
4112B_3.3V
T2
LP2950A
C49
0.1u
C46
47u
C47
47u
C48
0.1u
C41
C42
C43
C44
C45
C40
0.1u
47u
for 74HCT14, 74HCU04, 74LS07,
74HCT541
Title
AKD4705-A
Size
A
Document Number
POWER SUPPLY
Rev
0
Date:
Sheet 4 of 6

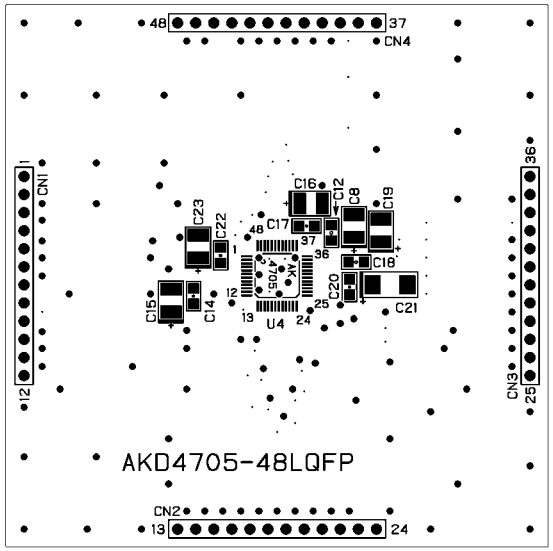


Title	**AKD4705-A**	
Size: A	Document Number: **Video Block Input Circuit**	Rev: 0
Date:	Sheet 5 of 6	



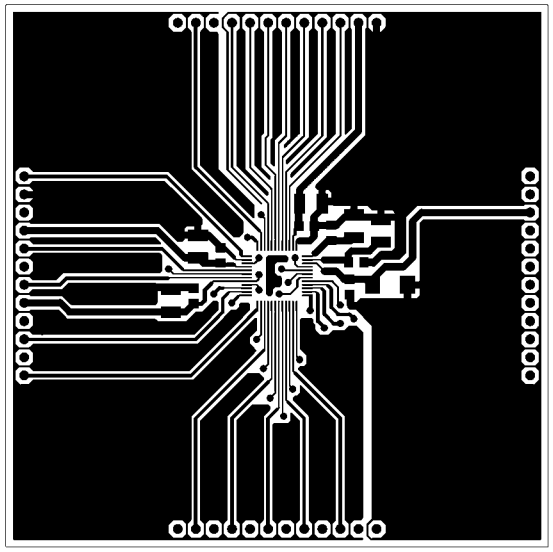


Title	AKD4705-A	
Size: A	Document Number: Video Block Output Circuit	Rev: 0
Date:	Sheet 6 of 6	



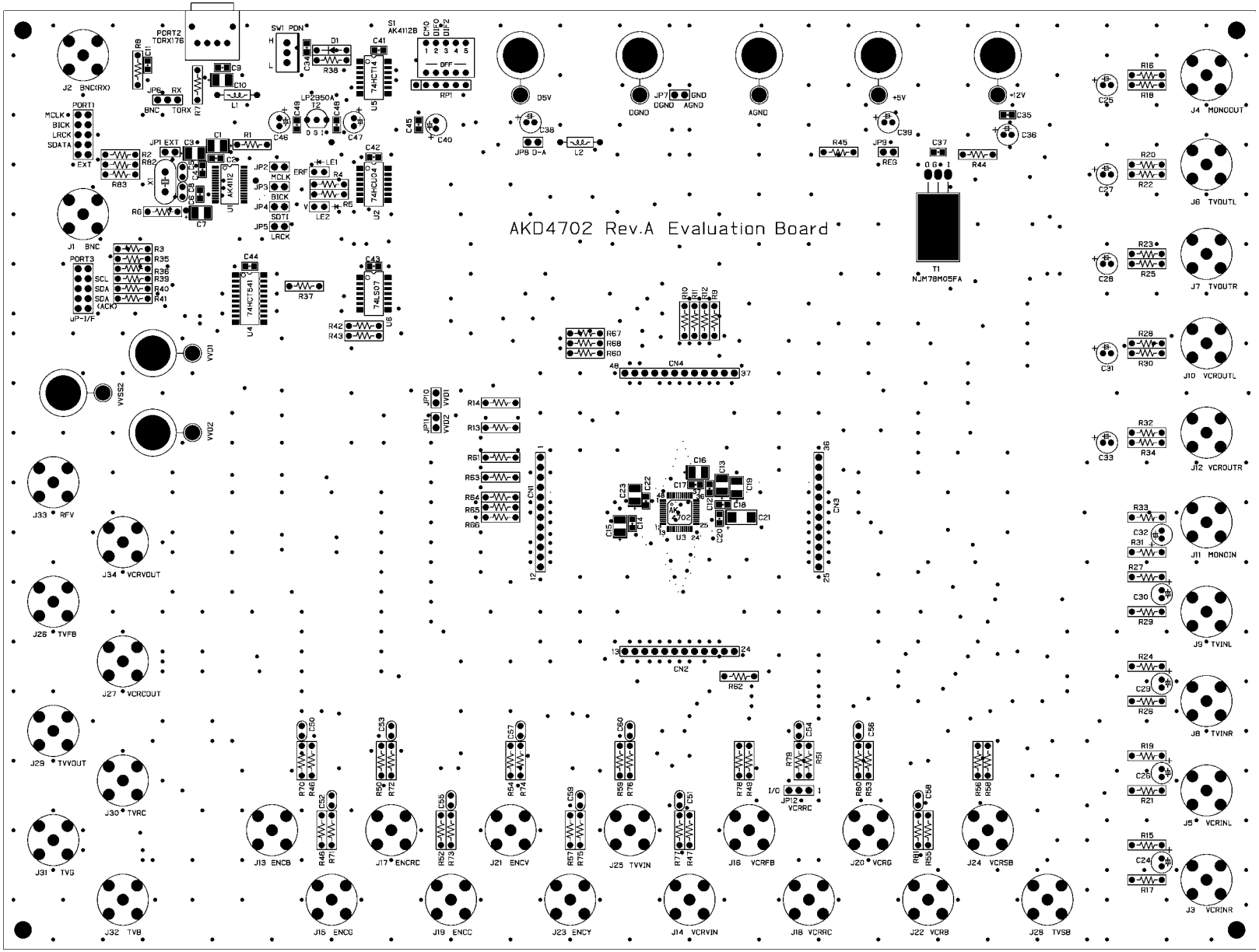
AKD4705 Rev.0 48LQFP L1 SR SILK

AKD4705 Rev.0 48LQFP L2 SR SILK

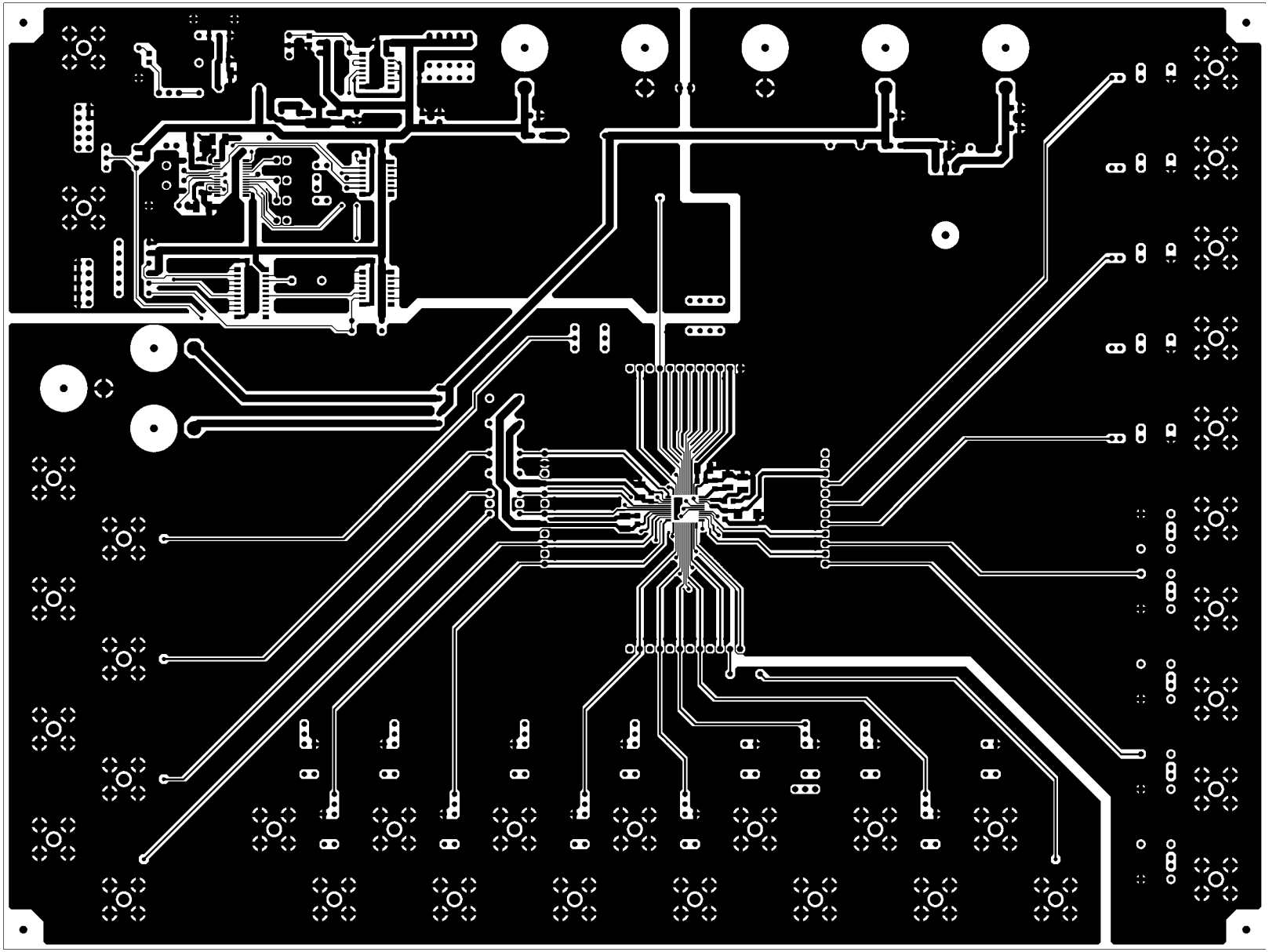


AKD4705 Rev.0 48LQFP L1

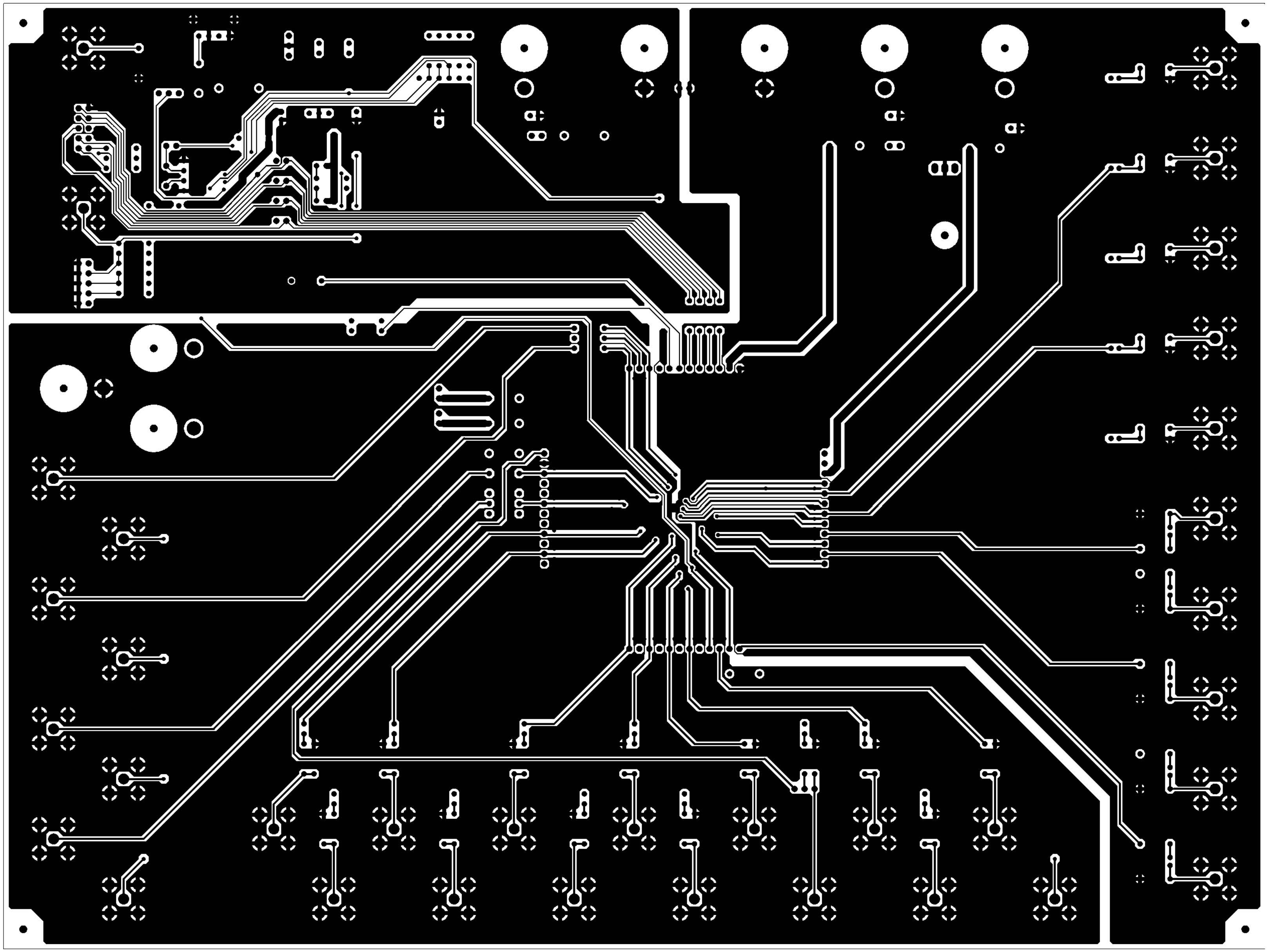
AKD4705 Rev.0 48LQFP L2


AKD4702 Rev.A Evaluation Board
J2 BNC(RX)
J1 BNC
PORT1
PORT3
I/F
J33 RFV
J34 VCRVOUT
J26 TVFB
J27 VCRCOUT
J29 TVVOUT
J30 TVRC
J31 TVG
J32 TVB
J13 ENCB
J15 ENCG
J17 ENCRC
J19 ENCC
J21 ENCV
J23 ENCY
J25 TVVIN
J14 VCRVIN
J16 VCRFB
J18 VCRRC
J20 VCRG
J22 VCRB
J24 VCRSB
J28 TVSB
J4 MONOOUT
J6 TVOUTL
J7 TVOUTR
J10 VCROUTL
J12 VCROUTR
J11 MONOIN
J9 TVINL
J8 TVINR
J5 VCRINL
J3 VCRINR
T1 NJM78M05FA
SW1 PDN
S1 AK4112B
RP1
U1 AK4112
U2 74HC04
U3 24
U4 74HCT541
U5 74HCT14
U6 74LS07
X1
CN1
CN2
CN3
CN4
JP1 EXT
JP2 MCLK
JP3 BICK
JP4 SDTI
JP5 LRCK
JP6 RX
JP7 DGND AGND
JP8 D-A
JP9 REG
JP10 VVD1
JP11 VVD2
JP12 VCRRC
D5V
+5V
+12V
DGND
AGND
VVD1
VVD2
VVSS2
LP2950
L1 SRSILK
L2

LZ SR



L1 パターン



LZ 1/9-Y