200mA Low-Dropout Linear Regulator with Pin-Selectable Dual-Voltage Level Output

FEATURES

- **Very Low Dropout: 230mV Typical at 200mA**
- **3% Accuracy Over Load/Line/Temperature**
- **Low I_Q: 50μA in Active Mode**
- **Available in Fixed-Output Voltages From 0.9V to 3.6V Using Innovative Factory EEPROM Programming**
- **VSET Pin Toggles Output Voltage Between Two Preset Levels**
  - **Preset Output Voltage Levels Can Be EEPROM-Programmed To Any Combination**
- **High PSRR: 65dB at 1kHz**
- **Stable with a 1.0μF Ceramic Capacitor**
- **Thermal Shutdown and Over-Current Protection**
- **Available in Wafer-Level Chip Scale and 2mm x 2mm SON Packages**

APPLICATIONS

- **Power Rails with Programming Mode**
- **Dual Voltage Levels for Power-Saving Mode**
- **Leakage Reduction for 90nm and 65nm Processors**
- **Wireless Handsets, Smart Phones, PDAs**
- **MP3 Players and Other Handheld Products**

DESCRIPTION

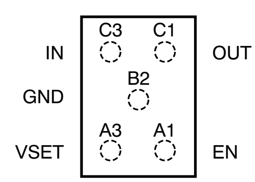
The TPS728xx series of low-dropout linear regulators (LDOs), with a selectable dual-voltage level output, is designed specially for applications that require two levels of output voltage regulation. Programming fuses and memory cards, reducing leakage effects, and conserving power in nanometric processes are some application examples.

The VSET pin is used to select one of two output voltage levels preset through innovative factory EEPROM programming. A precision bandgap and error amplifier provides an overall 3% accuracy over load, line, and temperature extremes.

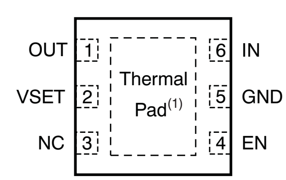
Ultra-small wafer chip scale (WCSP) and 2mm x 2mm SON packages make the TPS728xx series ideal for handheld applications.

This family of devices is fully specified over a temperature range of T_J = –40°C to +125°C.

TPS728xx Series
YZU PACKAGE
WCSP-5
(TOP VIEW)



TPS728xx Series
DRV PACKAGE
2mm x 2mm SON-6
(TOP VIEW)



(1) It is recommended that the SON package thermal pad be connected to ground.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT} (2)
TPS728**vvvxxx*yyyz***	**VVV** is the nominal output voltage for V_{OUT1} and corresponds to V_{SET} = Low. **XXX** is the nominal output voltage for V_{OUT2} and corresponds to V_{SET} = High. **YYY** is package designator. **Z** is Tape and reel quantity (R = 3000, T = 250).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Output voltages from 0.9V to 3.6V in 50mV increments are available through the use of innovative factory EEPROM programming; minimum order quantities may apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS(1)

At T_J = –40°C to +125°C (unless otherwise noted). All voltages are with respect to GND.

PARAMETER		TPS728xx Series	UNIT
Input voltage range, V_{IN}		–0.3 to +7.0	V
Enable and VSET voltage range, V_{EN} and V_{SET}		–0.3 to V_{IN} + 0.3(2)	V
Output voltage range, V_{OUT}		–0.3 to +7.0	V
Maximum output current, I_{OUT}		Internally limited	
Output short-circuit duration		Indefinite	
Total continuous power dissipation, P_{DISS}		See Dissipation Ratings Table	
ESD rating	Human body model (HBM)	2	kV
	Charged device model (CDM)	500	V
Operating junction temperature range, T_J		–55 to +150	°C
Storage temperature range, T_{STG}		–55 to +150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) V_{EN} and V_{SET} absolute maximum rating is V_{IN} + 0.3V or +7.0V, whichever is less.

DISSIPATION RATINGS

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = +25°C	T_A < +25°C	T_A = +70°C	T_A = +85°C
High-K(1)	DRV	20°C/W	65°C/W	15.4mW/°C	1540mW	845mW	615mW
High-K(1)	YZU	85°C/W	268°C/W	3.7mW/°C	370mW	205mW	150mW

(1) The JEDEC high-K (2s2p) board used to derive this data was a 3- × 3-inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

ELECTRICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.7V, whichever is greater; I_{OUT} = 0.5mA, V_{SET} = V_{EN} = V_{IN}, C_{OUT} = 1.0µF, unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range				2.7		6.5	V
V_{OUT} (1)	DC output accuracy	Nominal	T_J = +25°C, V_{SET} = high/low		–2.5		+2.5	mV
		Over V_{IN}, I_{OUT}, temperature	V_{OUT} + 0.5V ≤ V_{IN} ≤ 6.5V, 0mA ≤ I_{OUT} ≤ 200mA, V_{SET} = high/low		–3.0		+3.0	%
ΔV_{OUT}	Load transient		100µA to 200mA in 1µs, 200mA to 100µA in 1µs, C_{OUT} = 1µF			±60.0		mV
V_O	Output voltage range				0.9		3.6	V
$\Delta V_O/\Delta V_{IN}$	Line regulation		$V_{OUT(NOM)}$ + 0.5V ≤ V_{IN} ≤ 6.5V, I_{OUT} = 5mA			130		µV/V
$\Delta V_O/\Delta I_{OUT}$	Load regulation		0mA ≤ I_{OUT} ≤ 200mA			75		µV/mA
V_{DO}	Dropout voltage (2)		V_{IN} = $V_{OUT(NOM)}$ – 0.1V, I_{OUT} = 200mA			230	400	mV
I_{CL}	Output current limit		V_{OUT} = 0.9 × $V_{OUT(NOM)}$		240	340	575	mA
I_{GND}	Ground pin current		I_{OUT} = 0mA			50	80	µA
			I_{OUT} = 200mA			120		µA
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.4V, 2.7V ≤ V_{IN} < 4.5V, T_J = –40°C to +85°C			0.10	1.0	µA
PSRR	Power-supply rejection ratio		V_{IN} = 3.8V, V_{OUT} = 2.8V, I_{OUT} = 200mA	f = 100Hz		65		dB
				f = 1kHz		65		dB
				f = 10kHz		55		dB
				f = 100kHz		40		dB
V_N	Output noise voltage		BW = 100Hz to 100kHz, V_{IN} = 3.3V, V_{OUT} = 2.8V, I_{OUT} = 10mA			75 × V_{OUT}		$µV_{RMS}$
t_{TR}	Transition time (low-to-high) V_{OUT} = V_{OUT_LOW} to V_{OUT_HIGH} V_{OUT} = 97% × V_{OUT_HIGH}		V_{OUT_LOW} = 1.8V, V_{OUT_HIGH} = 3.15V, I_{OUT} = 10mA			60		µs
t_{STR}	Startup time (3)		C_{OUT} = 1.0µF			160		µs
t_{SHUT}	Shutdown time (4)		R_L = ∞, C_{OUT} = 1.0µF, V_{OUT} = 2.8V			180 (5)		µs
V_{HI}	VSET high (output V_{OUT2} selected), or enable pin high (enabled)				1.2		V_{IN}	V
V_{LO}	VSET low (output V_{OUT1} selected), or enable pin low (disabled)				0		0.4	V
I_{EN}, I_{VSET}	Enable and select pin currents		EN = VSET = 6.5V			0.04	1.0	µA
UVLO	Undervoltage lockout		V_{IN} rising, V_{SET} = high/low		2.38	2.51	2.65	V
	Hysteresis		V_{IN} falling, V_{SET} = high/low			230		mV
T_{SD}	Thermal shutdown temperature		Shutdown, temperature increasing			+160		°C
			Reset, temperature decreasing			+140		°C
T_J	Operating junction temperature				–40		+125	°C

(1) The output voltage for V_{SET} = low/high is programmed at the factory.
(2) V_{DO} is not measured for devices with $V_{OUT(NOM)}$ < 2.8V because minimum V_{IN} = 2.7V.
(3) Time from V_{EN} = 1.2V to V_{OUT} = 97% ($V_{OUT(NOM)}$).
(4) Time from V_{EN} = 0.4V to V_{OUT} = 5% ($V_{OUT(NOM)}$).
(5) See *Shutdown* in the *Application Information* section for more details.

DEVICE INFORMATION

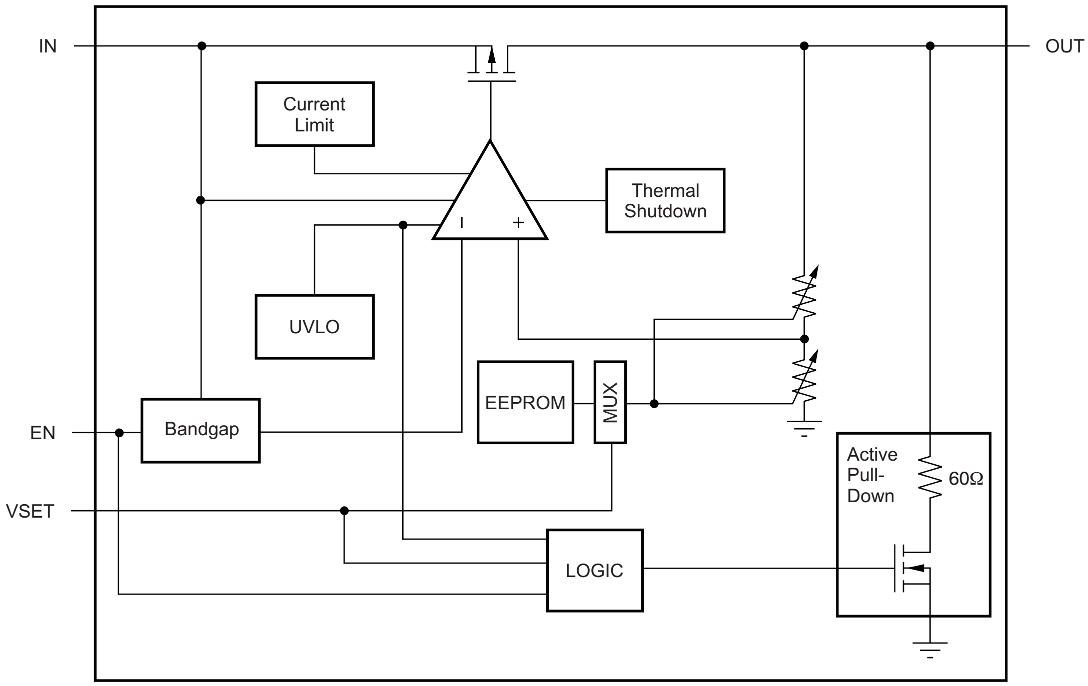
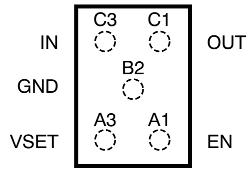
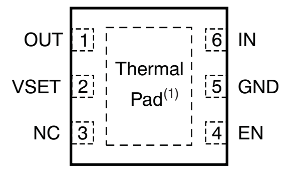


Figure 1. Functional Block Diagram

**YZU PACKAGE
WCSP-5
(TOP VIEW)**



**DRV PACKAGE
SON-8
(TOP VIEW)**



(1) It is recommended that the SON package thermal pad be connected to ground.

PIN DESCRIPTIONS

TPS728xx Series			
NAME	**DRV**	**YZU**	**DESCRIPTION**
OUT	1	C1	Regulated output voltage pin. A small 1μF ceramic capacitor is needed from this pin to ground to assure stability. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.
VSET	2	A3	Select pin. Driving VSET below 0.4V selects preset output voltage V_{OUT1}. Driving VSET over 1.2V selects preset output voltage V_{OUT2}.
NC	3	—	No connection.
EN	4	A1	Enable pin. Driving EN over 1.2V turns on the regulator. Driving EN below 0.4V puts the regulator into shutdown mode, thus reducing the operating current to 100nA, nominal.
GND	5	B2	Ground pin (connect DRV thermal pad to ground)
IN	6	C3	Input pin. A small capacitor is needed from this pin to ground to assure stability. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.

TYPICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.7V, whichever is greater; I_{OUT} = 0.5mA, V_{EN} = V_{SET} = V_{IN}, C_{OUT} = 1.0μF, unless otherwise noted. Typical values are at T_J = +25°C.

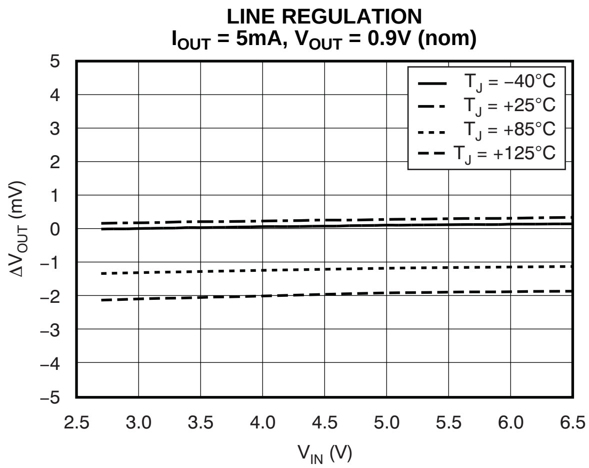


Figure 2.

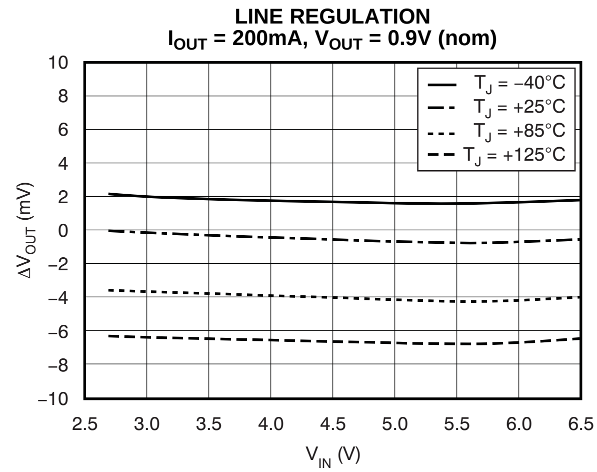


Figure 3.

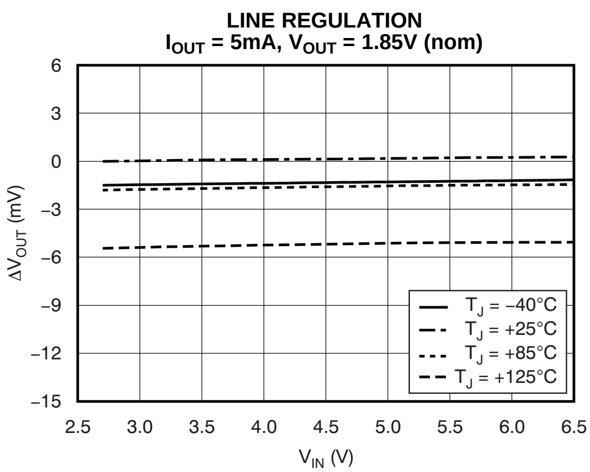


Figure 4.

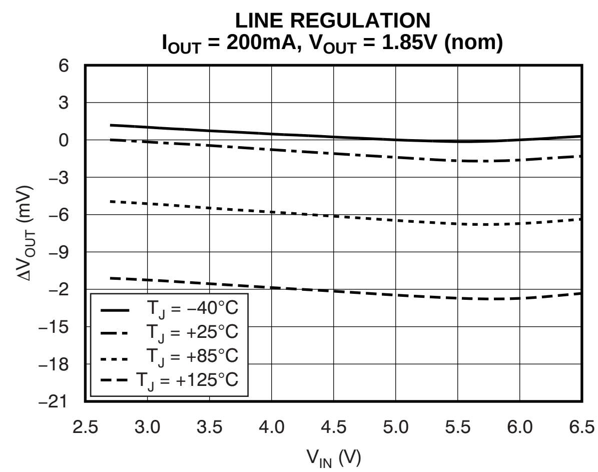


Figure 5.

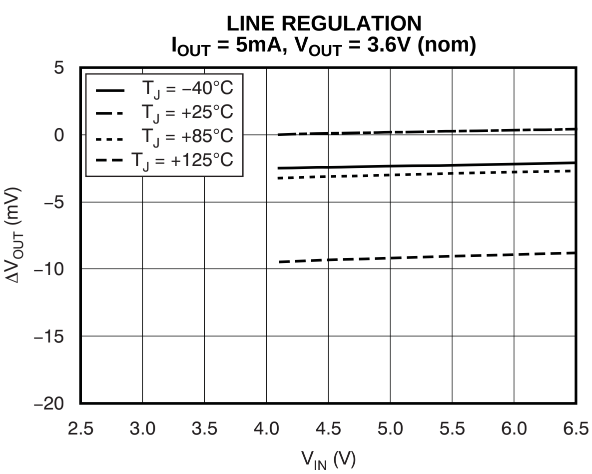


Figure 6.

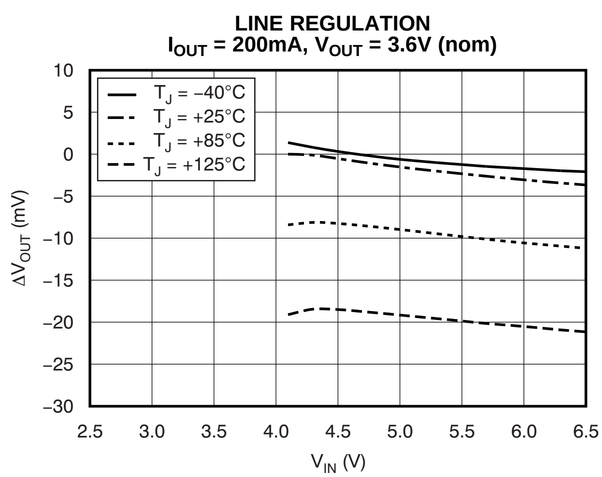


Figure 7.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.7V, whichever is greater; I_{OUT} = 0.5mA, V_{EN} = V_{SET} = V_{IN}, C_{OUT} = 1.0μF, unless otherwise noted. Typical values are at T_J = +25°C.

LOAD REGULATION UNDER LIGHT LOADS
V_{OUT} = 0.9V (nom)

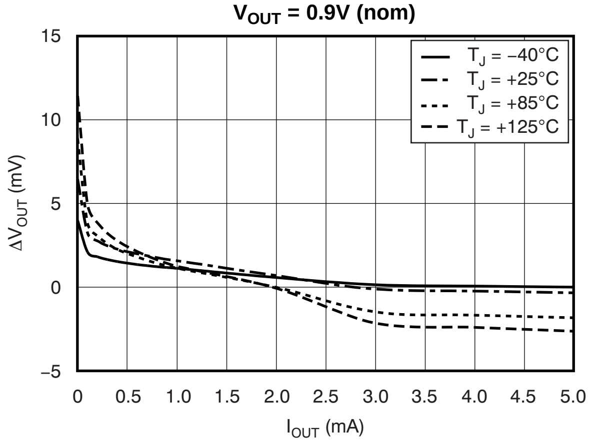


Figure 8.

LOAD REGULATION
V_{OUT} = 0.9V (nom)

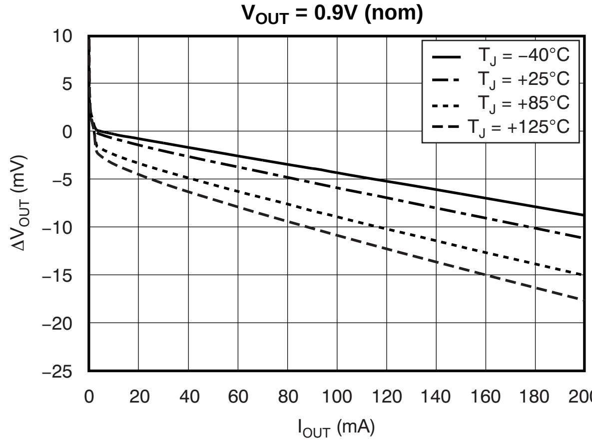


Figure 9.

LOAD REGULATION UNDER LIGHT LOADS
V_{OUT} = 1.85V (nom)

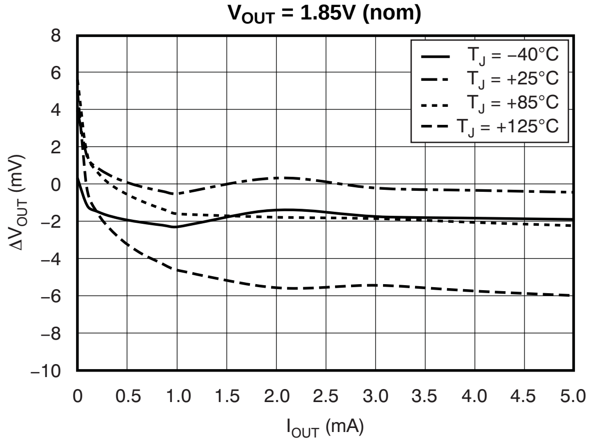


Figure 10.

LOAD REGULATION
V_{OUT} = 1.85V (nom)

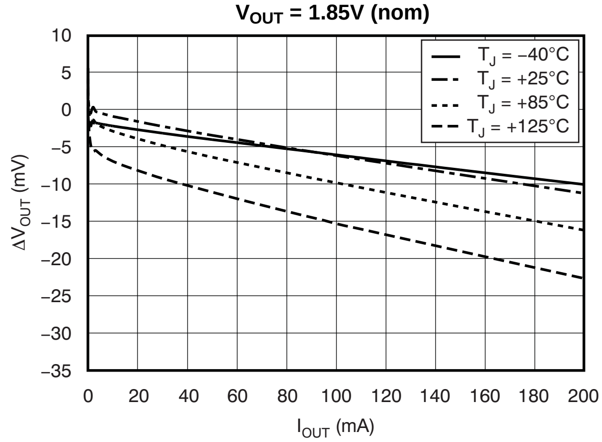


Figure 11.

LOAD REGULATION UNDER LIGHT LOADS
V_{OUT} = 3.6V (nom)

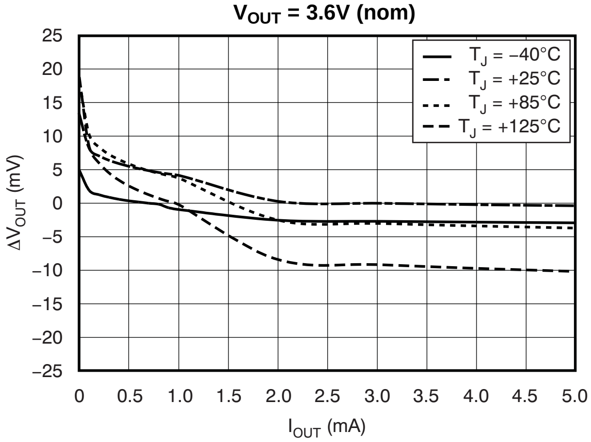


Figure 12.

LOAD REGULATION
V_{OUT} = 3.6V (nom)

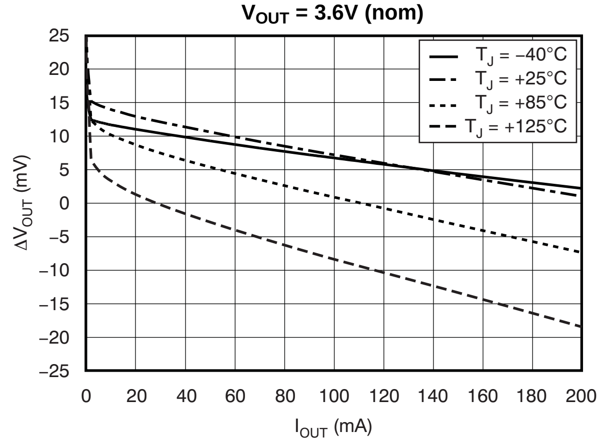


Figure 13.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.7V, whichever is greater; I_{OUT} = 0.5mA, V_{EN} = V_{SET} = V_{IN}, C_{OUT} = 1.0μF, unless otherwise noted. Typical values are at T_J = +25°C.

DROPOUT VOLTAGE vs OUTPUT CURRENT

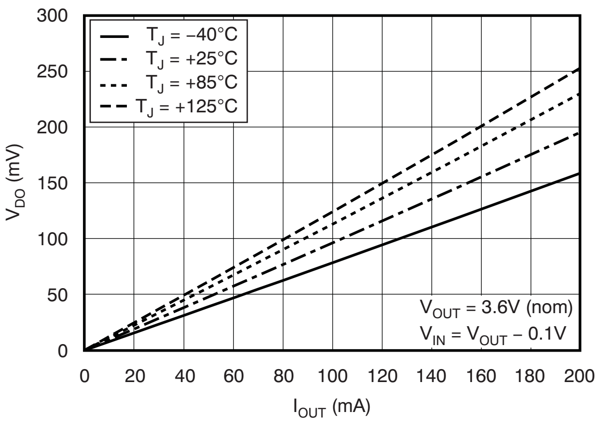


Figure 14.

OUTPUT VOLTAGE vs TEMPERATURE

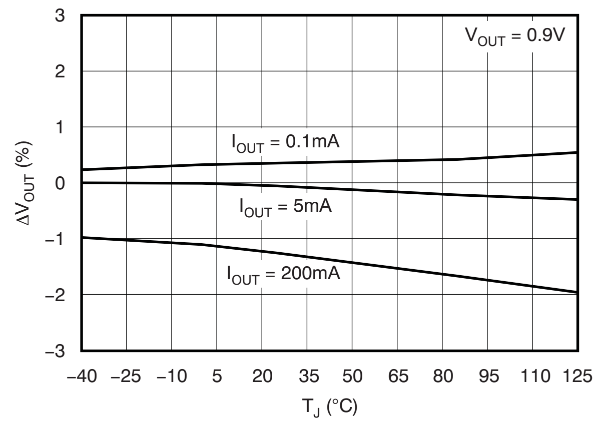


Figure 15.

OUTPUT VOLTAGE vs TEMPERATURE

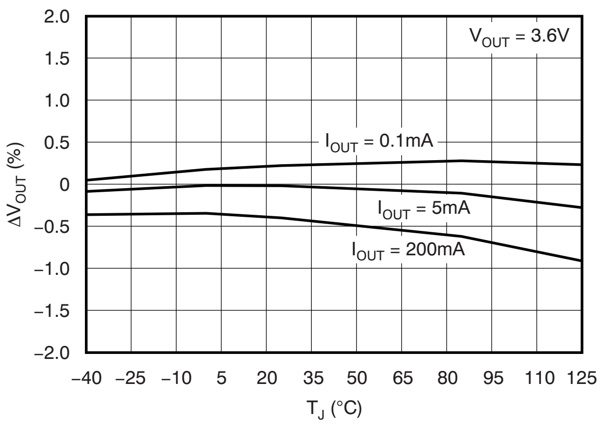


Figure 16.

GROUND PIN CURRENT vs INPUT VOLTAGE

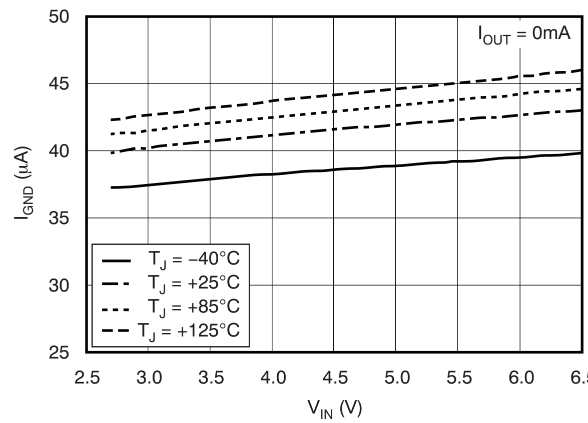


Figure 17.

GROUND PIN CURRENT vs OUTPUT CURRENT

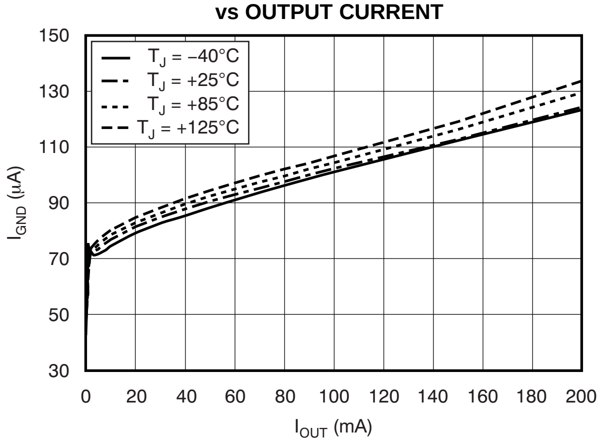


Figure 18.

GROUND PIN CURRENT vs TEMPERATURE

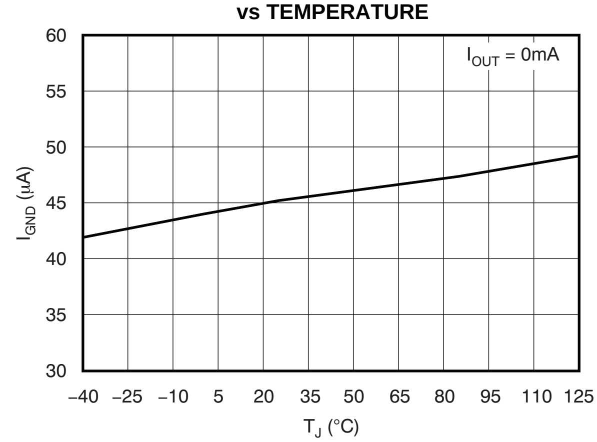


Figure 19.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.7V, whichever is greater; I_{OUT} = 0.5mA, V_{EN} = V_{SET} = V_{IN}, C_{OUT} = 1.0μF, unless otherwise noted. Typical values are at T_J = +25°C.

SHUTDOWN CURRENT vs INPUT VOLTAGE

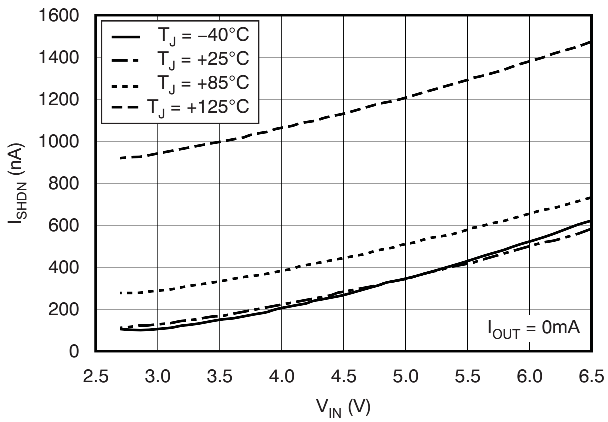


Figure 20.

CURRENT LIMIT vs INPUT VOLTAGE

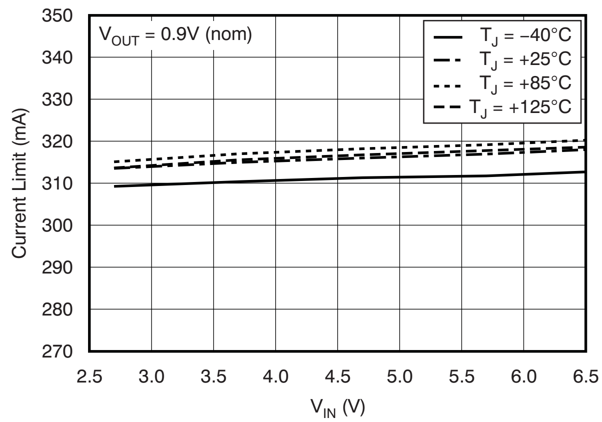


Figure 21.

CURRENT LIMIT vs INPUT VOLTAGE

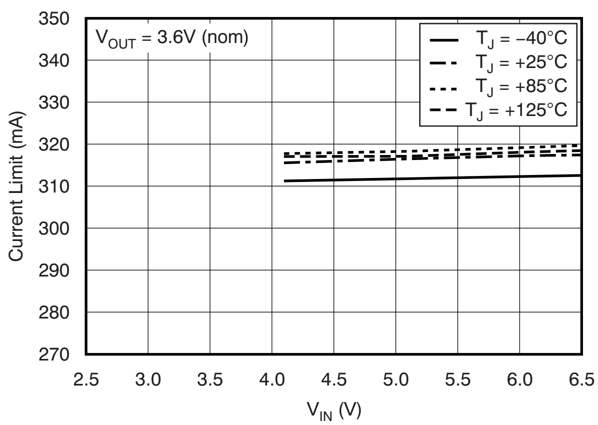


Figure 22.

TPS728185315 POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (V_{IN} – V_{OUT} = 0.85V)

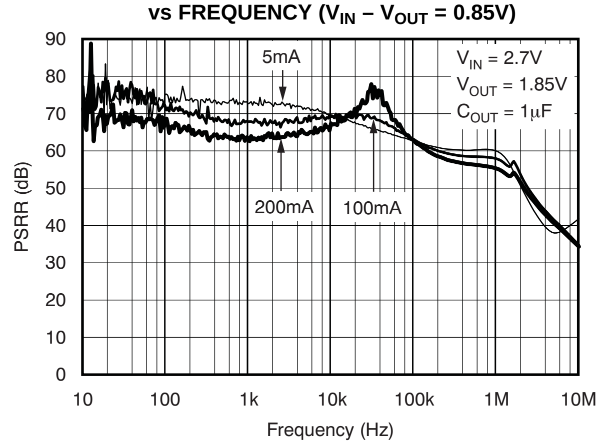


Figure 23.

TPS728185315 POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (V_{IN} – V_{OUT} = 1.0V)

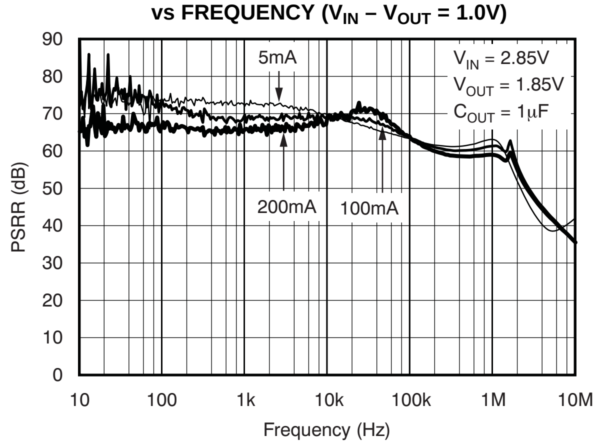


Figure 24.

TPS728185315 POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (V_{IN} – V_{OUT} = 0.5V)

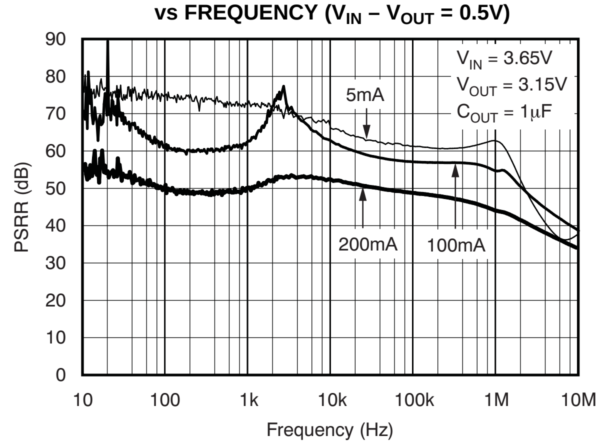


Figure 25.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.7V, whichever is greater; I_{OUT} = 0.5mA, V_{EN} = V_{SET} = V_{IN}, C_{OUT} = 1.0µF, unless otherwise noted. Typical values are at T_J = +25°C.

TPS728185315 POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (V_{IN} – V_{OUT} = 1.0V)

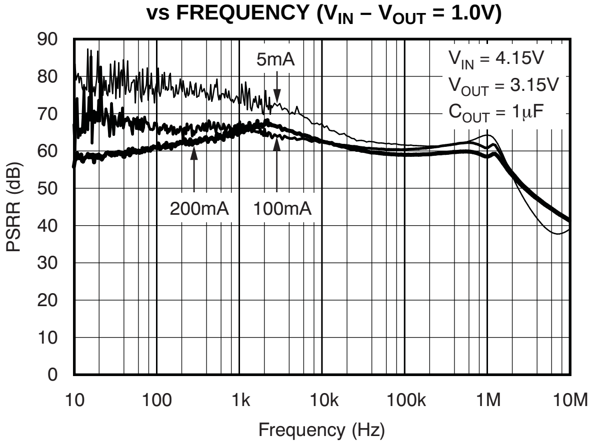


Figure 26.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

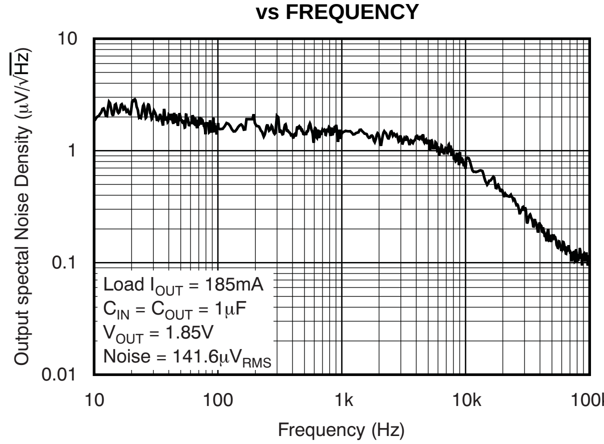


Figure 27.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

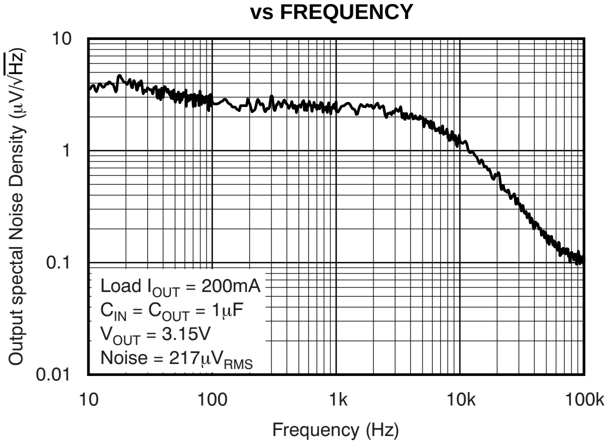


Figure 28.

LINE TRANSIENT RESPONSE

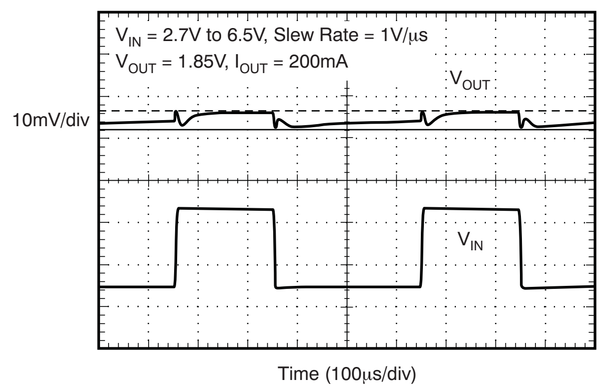


Figure 29.

LINE TRANSIENT RESPONSE

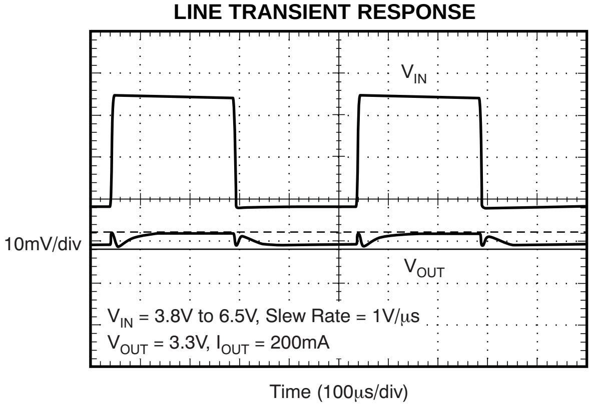


Figure 30.

LOAD TRANSIENT RESPONSE

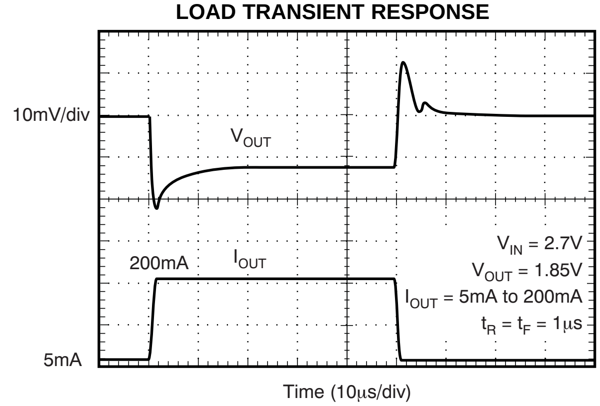


Figure 31.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.7V, whichever is greater; I_{OUT} = 0.5mA, V_{EN} = V_{SET} = V_{IN}, C_{OUT} = 1.0µF, unless otherwise noted. Typical values are at T_J = +25°C.

LOAD TRANSIENT RESPONSE

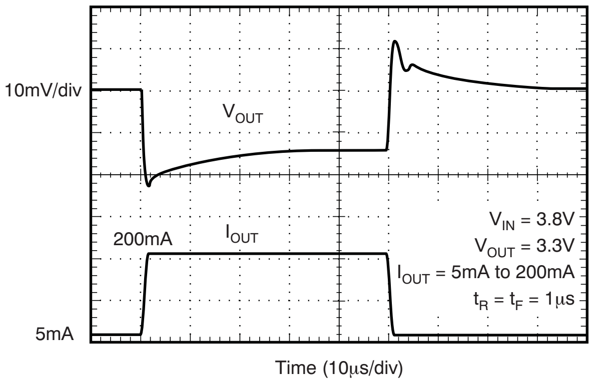


Figure 32.

ENABLE TRANSIENT RESPONSE

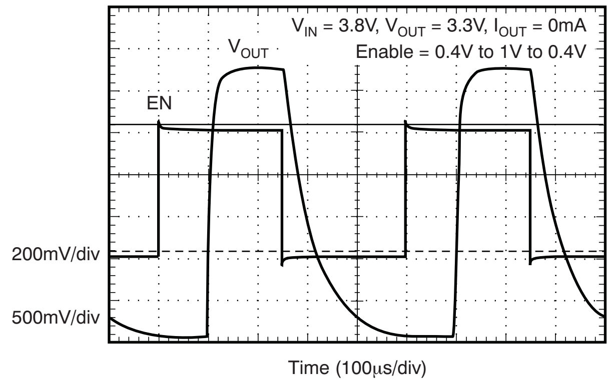


Figure 33.

V_{IN} RAMP UP AND RAMP DOWN RESPONSE

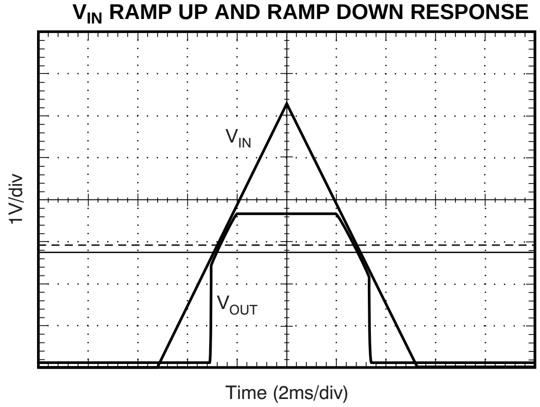


Figure 34.

VSET PIN TOGGLE

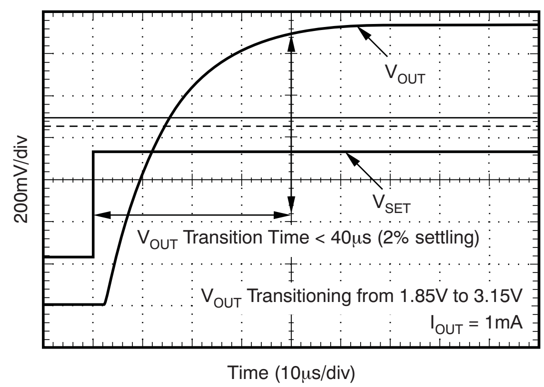


Figure 35.

VSET PIN TOGGLE

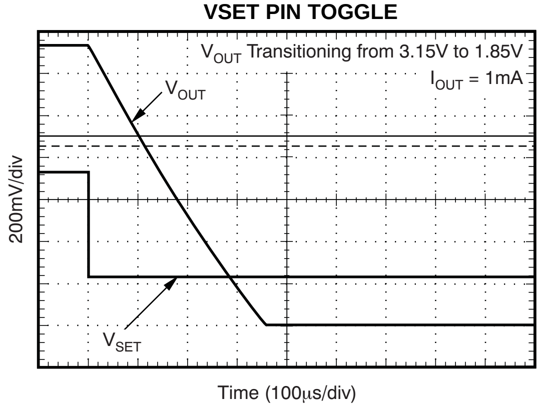


Figure 36.

VSET PIN TOGGLE

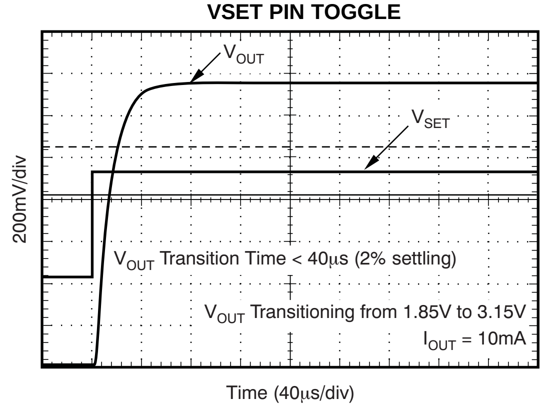


Figure 37.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.7V, whichever is greater; I_{OUT} = 0.5mA, V_{EN} = V_{SET} = V_{IN}, C_{OUT} = 1.0μF, unless otherwise noted. Typical values are at T_J = +25°C.

VSET PIN TOGGLE

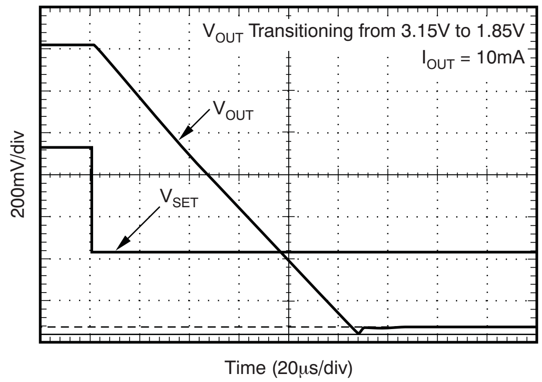


Figure 38.

APPLICATION INFORMATION

The TPS728xx series belongs to a family of new generation LDO regulators that use innovative circuitry to achieve ultra-wide bandwidth and high loop gain, resulting in extremely high PSRR (up to 1MHz) at very low headroom (V_{IN} – V_{OUT}). These features, combined with low noise, low ground pin current, and ultra-small packaging, make this device ideal for portable applications. This family of regulators offers sub-bandgap output voltages, current limit and thermal protection, and is fully specified from –40°C to +125°C.

Figure 39 shows the basic circuit connections.

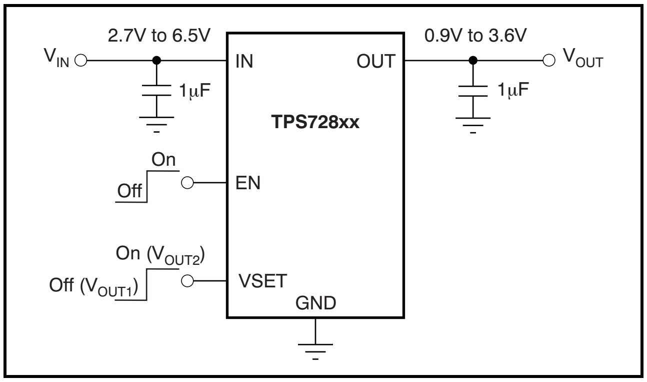


Figure 39. Typical Application Circuit

APPLICATION EXAMPLES

EEPROM-based applications require the programming voltage to be higher than the operating voltage. The TPS728xx suits such applications where the maximum programming voltage of the EEPROM is higher than the operating voltage. The VSET logic pin allows the application to transition between the higher EEPROM programming voltage and the lower operating voltage. For example, the TPS728xx typically takes less than 40μs to transition from a lower voltage of 1.85V to a higher voltage of 3.15V under an output load of 1mA to 10mA, as shown in Figure 35 and Figure 37, respectively. The special circuitry in the TPS728xx helps transition from the higher voltage to the lower voltage under no load. The load on the output at the end of the programming cycle is typically under 10mA. Output voltage overshoots and undershoots are minimal under this load condition. The TPS728xx typically takes less than 1ms of transition time going from 3.15V to 1.85V, as shown in Figure 36 and Figure 38, respectively. Both output states of the TPS728xx are programmable between 0.9V to 3.6V.

Another area where the TPS728xx can be used effectively is in dynamic voltage scaling (DVS) applications. In DVS applications, it is required to dynamically switch between a high operational voltage to a low standby voltage in order to balance performance of processors and achieve power savings. Modern multimillion gate microprocessors fabricated with the latest sub-micron processes save on power by transitioning to a lower voltage to reduce leakage currents without losing content. This architecture enables the microprocessor to transition quickly into an operational state (wake up) without requiring reloading of the states from external memory, or a reboot.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1μF to 1.0μF low equivalent series resistance (ESR) capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located near the power source. If source impedance is not sufficiently low, a 0.1μF input capacitor may be necessary to ensure stability.

The TPS728xx is designed to be stable with standard ceramic capacitors with values of 1.0μF or larger at the output. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be less than 1.0Ω.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device. High ESR capacitors may degrade PSRR.

INTERNAL CURRENT LIMIT

The TPS728xx internal current limits help protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in a current limit state for extended periods of time.

The PMOS pass element in the TPS728xx has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of rated output current may be appropriate.

SHUTDOWN

The enable pin (EN) is active high and is compatible with standard and low voltage, TTL-CMOS levels. When shutdown capability is not required, EN can be connected to the IN pin, as shown in Figure 40. Figure 41 shows when both EN and VSET are tied to IN. The TPS728xx, with internal active output pulldown circuitry, discharges the output to within 5% of V_{OUT} with a time (t) of:

$$t = 3\left(\frac{60 \times R_L}{60 + R_L}\right) \times C_{OUT}$$

Where:

R_L = output load resistance

C_{OUT} = output capacitance

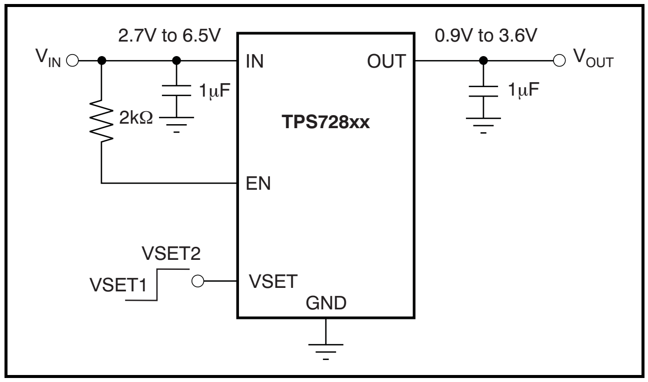


Figure 40. Circuit Showing EN Tied High when Shutdown Capability is Not Required

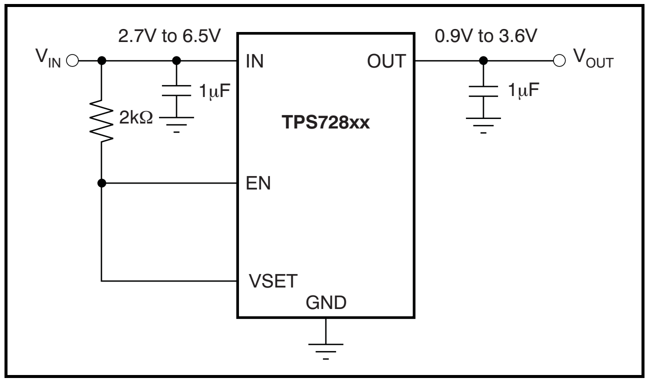


Figure 41. Circuit to Tie Both EN and VSET High

DROPOUT VOLTAGE

The TPS728xx uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} approximately scales with output current because the PMOS device behaves like a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in Figure 25 and Figure 26 in the Typical Characteristics section.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

UNDERVOLTAGE LOCK-OUT (UVLO)

The TPS728xx uses an undervoltage lock-out circuit to keep the output shut off until the internal circuitry is operating properly. The UVLO circuit has a deglitch feature so that it typically ignores undershoot transients on the input if they are less than 5μs duration. The UVLO circuit triggers at approximately 2.3V on an undershooting or a falling input voltage. On the TPS728xx, the active pulldown discharges V_{OUT} when the device is in UVLO off condition. However, the input voltage must be greater than 0.8V for the active pulldown to work.

MINIMUM LOAD

The TPS728xx is stable with no output load. Traditional PMOS LDO regulators suffer from lower loop gain at very light output loads. The TPS728xx employs an innovative, low-current mode circuit under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current.

THERMAL INFORMATION

Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS728xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS728xx into thermal shutdown degrades device reliability.

Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Dissipation Ratings* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in Equation 1:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{1}$$

Package Mounting

Solder pad footprint recommendations for the TPS728xx are available from the Texas Instruments web site at www.ti.com.

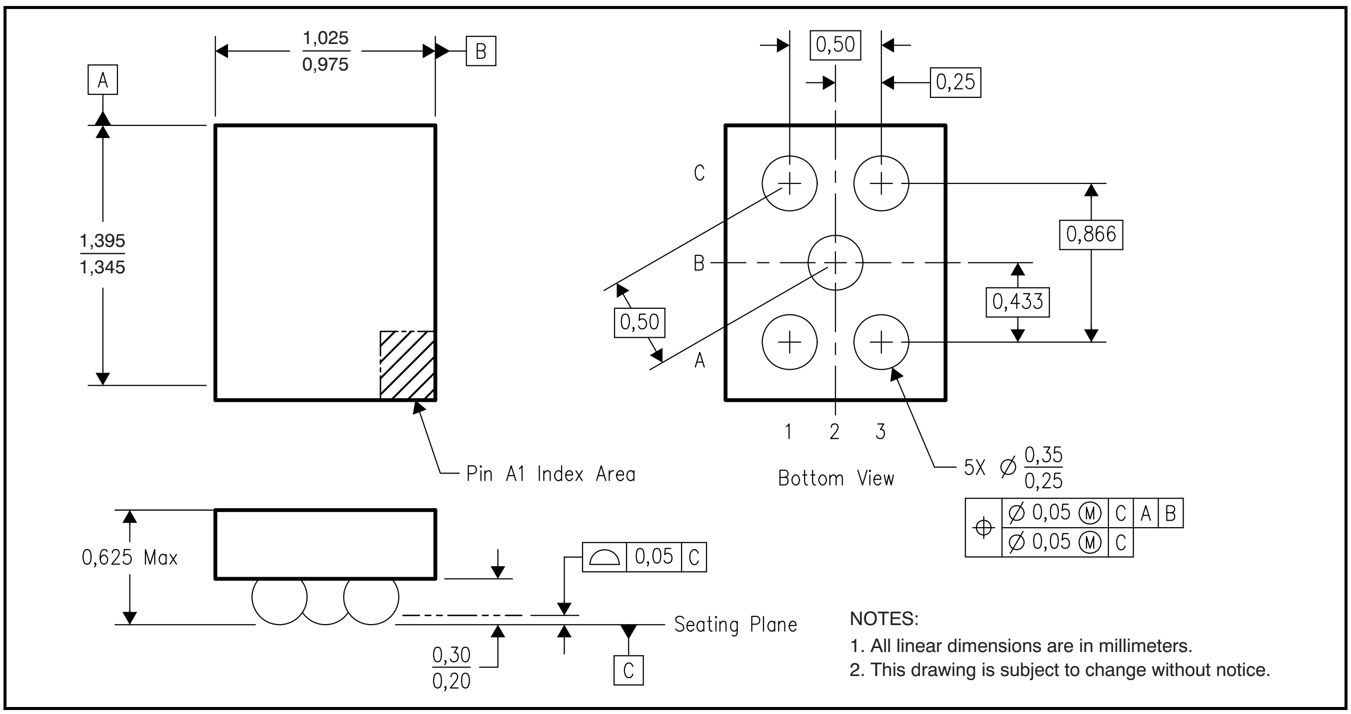


Figure 42. YZU Wafer Chip-Scale Package Dimensions (in mm)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS728185315DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS728185315DRVRG4	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS728185315DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS728185315DRVTG4	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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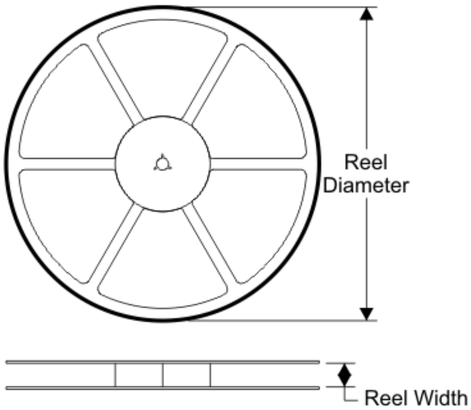
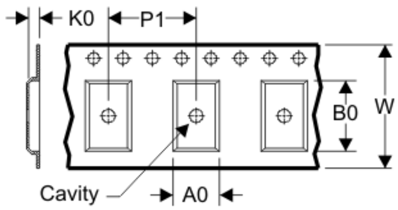
TAPE AND REEL BOX INFORMATION

REEL DIMENSIONS

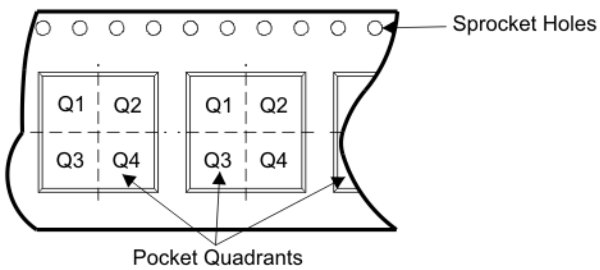


TAPE DIMENSIONS



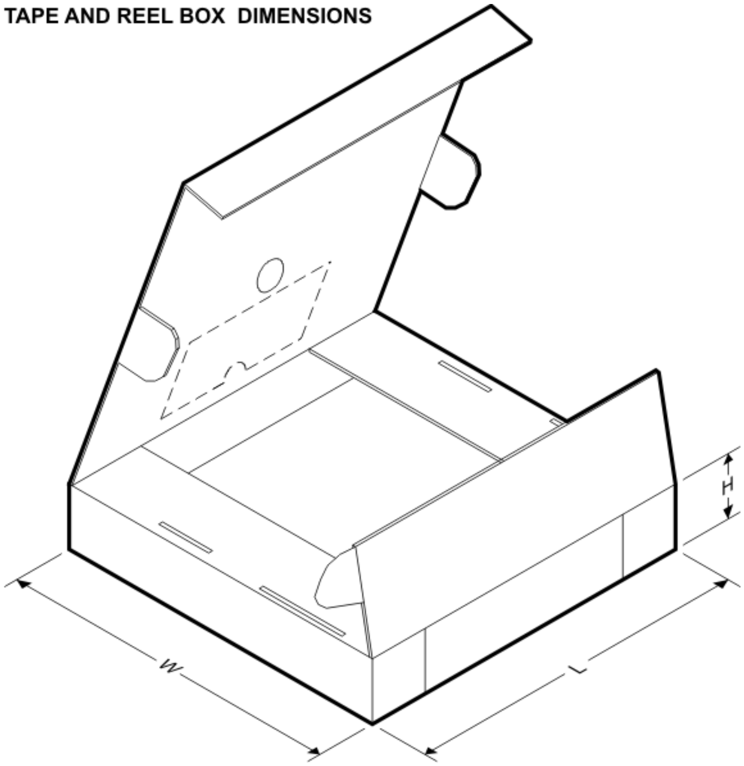
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



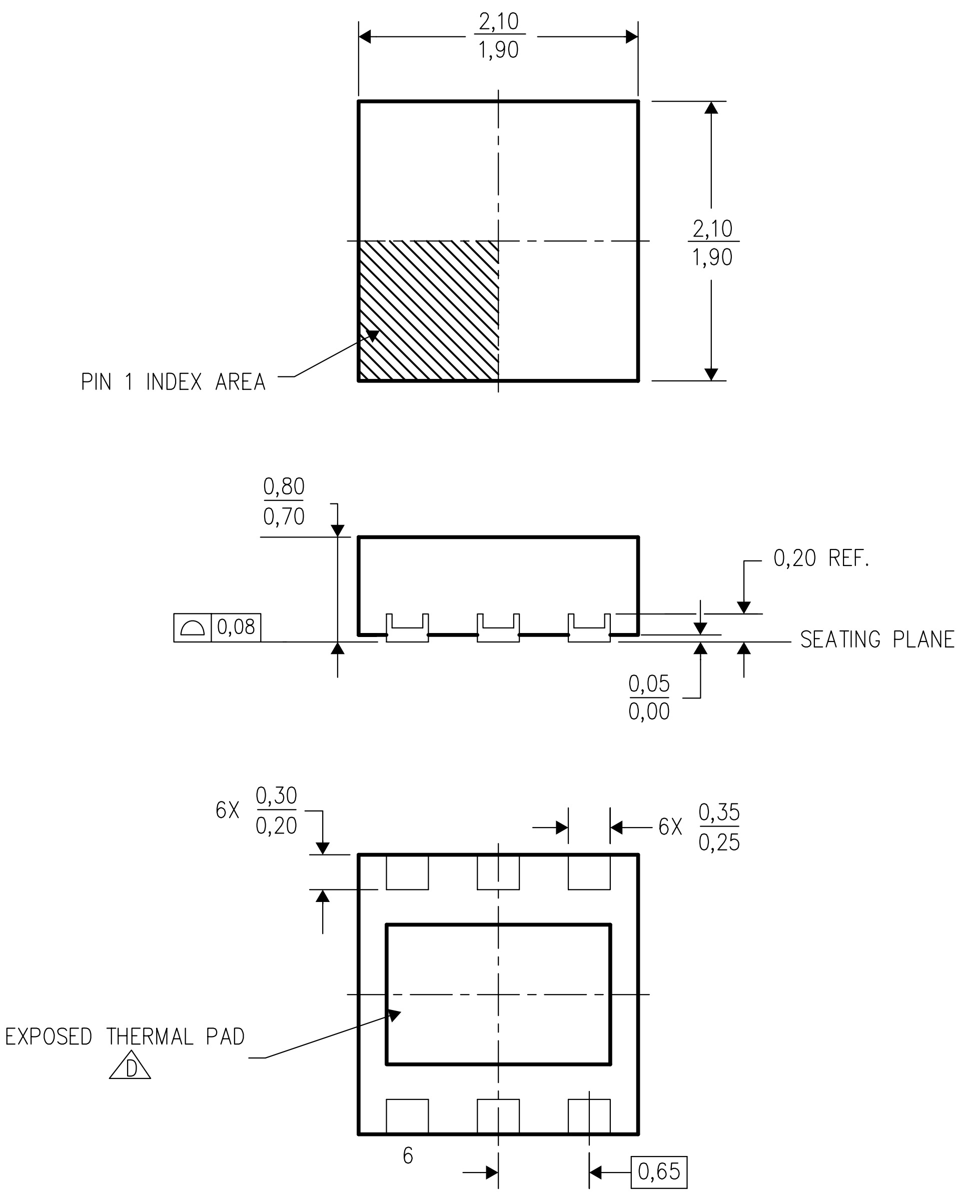
Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS728185315DRVR	DRV	6	SITE 48	179	8	2.2	2.2	1.2	4	8	Q2
TPS728185315DRVT	DRV	6	SITE 48	179	8	2.2	2.2	1.2	4	8	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
TPS728185315DRVR	DRV	6	SITE 48	195.0	200.0	45.0
TPS728185315DRVT	DRV	6	SITE 48	195.0	200.0	45.0

DRV (S-PDSO-N6) PLASTIC SMALL OUTLINE



4206925/C 01/07

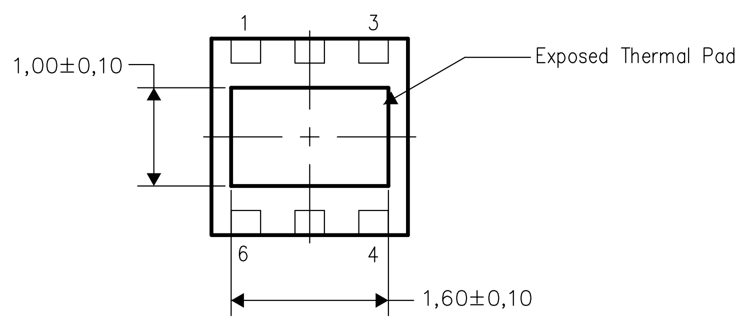
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

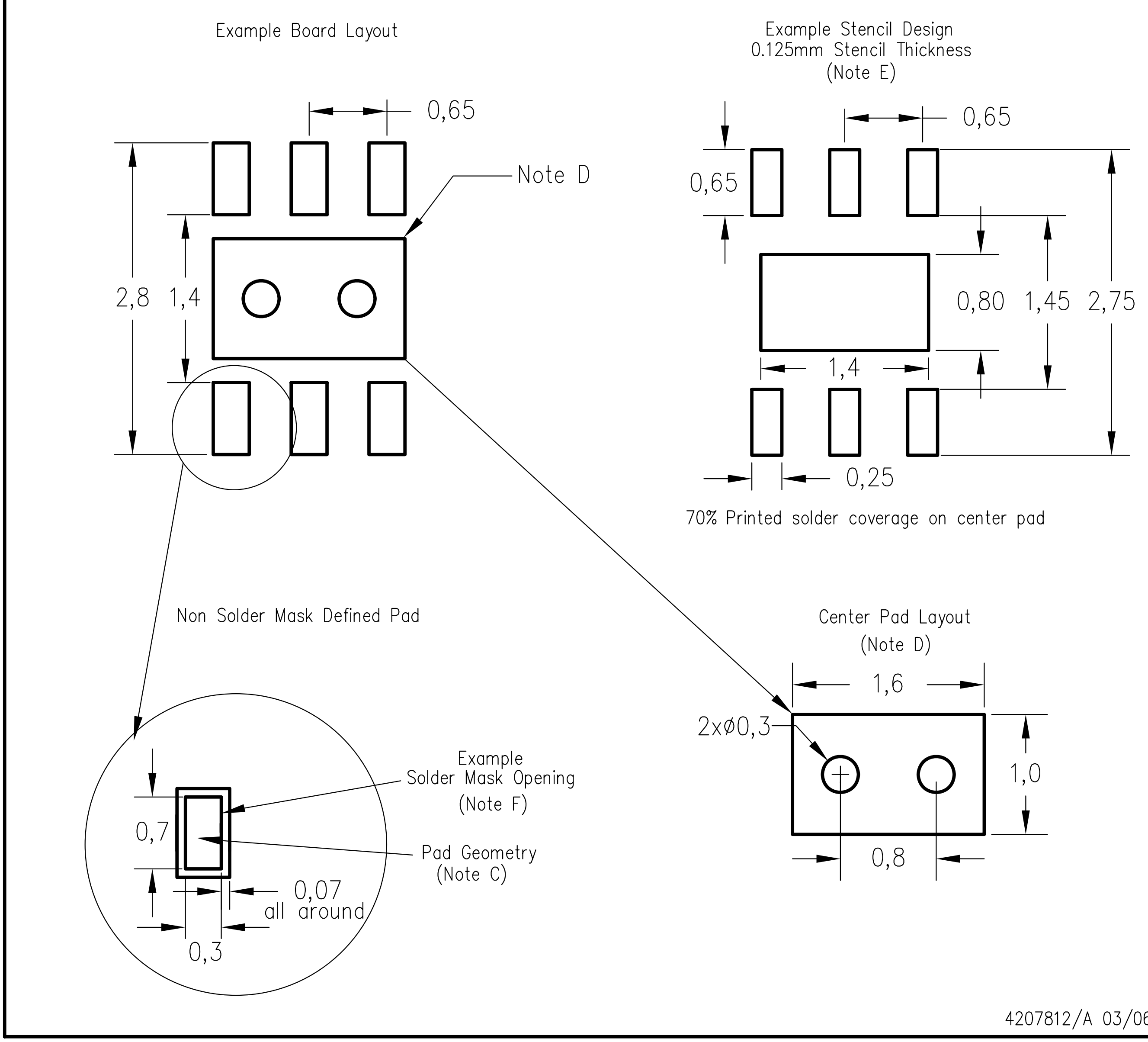


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRV (S–PDSO–N6)



4207812/A 03/06

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for solder mask tolerances.