CBT3253A

Dual 1-of-4 FET multiplexer/demultiplexer

Rev. 02 — 8 February 2007 Product data sheet

1. General description

The CBT3253A is a dual 1-of-4 high-speed TTL-compatible FET multiplexer/demultiplexer. The low on-resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

$1\overline{OE}$, $2\overline{OE}$, S0, and S1 select the appropriate B output for the A-input data.

The CBT3253A is characterized for operation from –40 °C to +85 °C.

2. Features

- 5 Ω switch connection between two ports
- TTL-compatible input levels
- Minimal propagation delay through the switch
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA

3. Ordering information

Table 1. Ordering information

T_{amb} = –40 °C to +85 °C

Type number	Topside mark	Package		
		Name	Description	Version
CBT3253AD	CBT3253AD	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
CBT3253ADB	C3253A	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
CBT3253ADS	CT3253A	SSOP16[1]	plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT519-1
CBT3253APW	CT3253A	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

[1] Also known as QSOP16.

4. Functional diagram

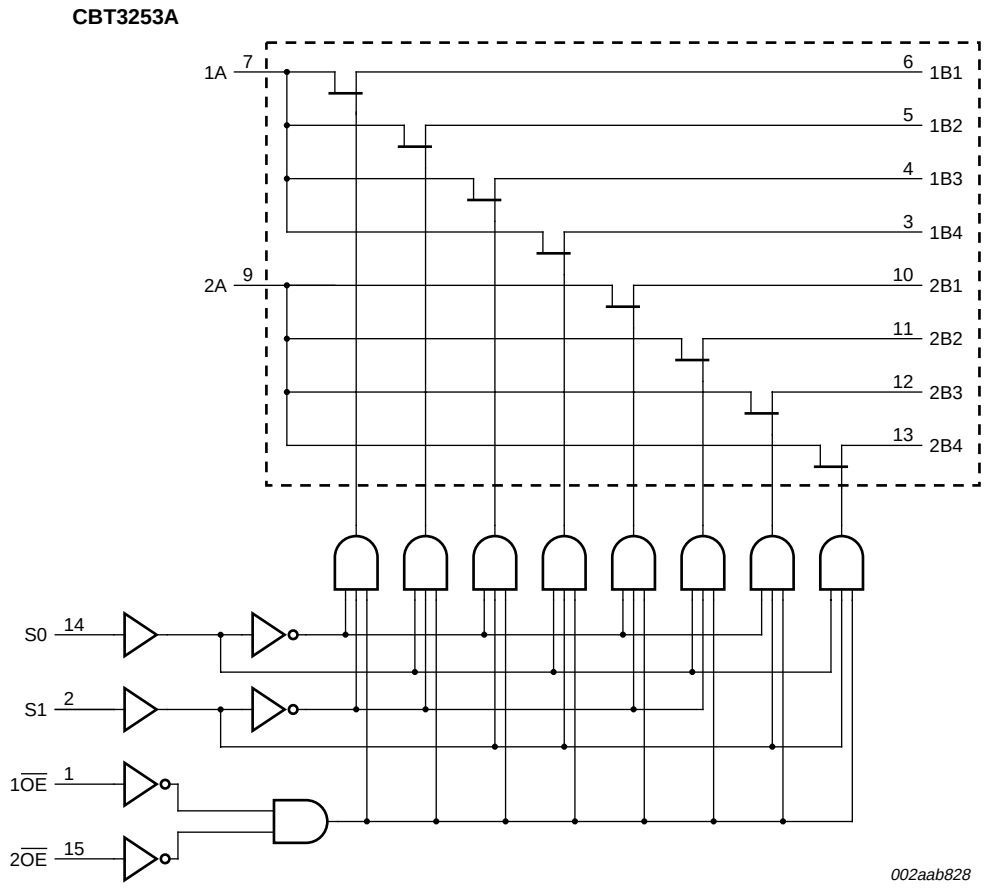


Fig 1. Logic diagram of CBT3253A (positive logic)

5. Pinning information

5.1 Pinning

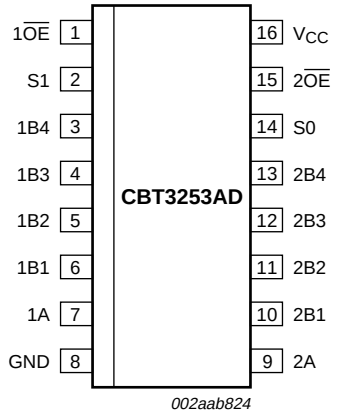


Fig 2. Pin configuration for SO16

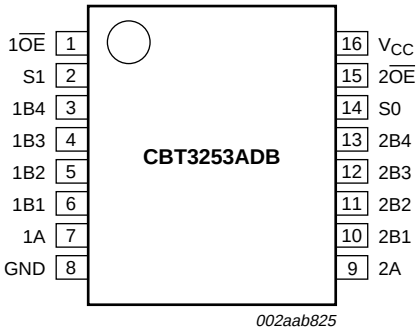


Fig 3. Pin configuration for SSOP16

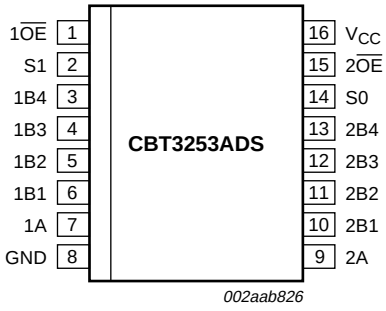


Fig 4. Pin configuration for SSOP16 (QSOP16)

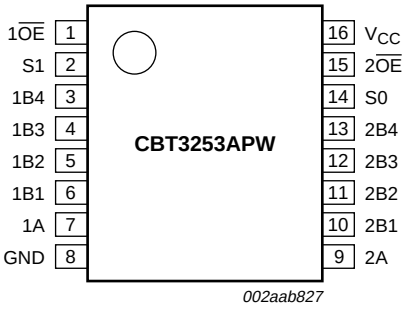


Fig 5. Pin configuration for TSSOP16

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{OE}$	1	output enable (active LOW)
S1	2	select-control input
1B4, 1B3, 1B2, 1B1	3, 4, 5, 6	B outputs[1]
1A	7	A input
GND	8	ground (0 V)
2A	9	A input
2B1, 2B2, 2B3, 2B4	10, 11, 12, 13	B outputs
S0	14	select-control input
$2\overline{OE}$	15	output enable (active LOW)
V_{CC}	16	positive supply voltage

[1] B outputs are inputs if A inputs are outputs.

6. Functional description

Refer to Figure 1 “Logic diagram of CBT3253A (positive logic)”

6.1 Function selection

Table 3. Function selection

H = HIGH state; L = LOW state; X = Don’t Care

Inputs				Function
$1\overline{OE}$	$2\overline{OE}$	S1	S0	
X	H	X	X	disconnect 1A and 2A
H	X	X	X	disconnect 1A and 2A
L	L	L	L	1A to 1B1 and 2A to 2B1
L	L	L	H	1A to 1B2 and 2A to 2B2
L	L	H	L	1A to 1B3 and 2A to 2B3
L	L	H	H	1A to 1B4 and 2A to 2B4

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+7.0	V
V_I	input voltage		–0.5[1]	+7.0	V
I_{CCC}	continuous current through each V_{CC} or GND pin		-	128	mA
I_{IK}	input clamping current	$V_I < 0$ V	-	–50	mA
T_{stg}	storage temperature		–65	+150	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

8. Recommended operating conditions

Table 5. Operating conditions

All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_{IH}	HIGH-level input voltage		2	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
T_{amb}	ambient temperature	operating in free air	–40	-	+85	°C

9. Static characteristics

Table 6. Static characteristics

T_{amb} = −40 °C to +85 °C

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_I = −18 mA		-	-	−1.2	V
V_{pass}	pass voltage	V_I = V_{CC} = 5.5 V; I_O = −100 µA		3.4	3.6	3.9	V
I_{LI}	input leakage current	V_{CC} = 5 V; V_I = 5.5 V or GND		-	-	±1	µA
I_{CC}	quiescent supply current	V_{CC} = 5.5 V; I_O = 0 mA; V_I = V_{CC} or GND		-	-	3	µA
ΔI_{CC}	additional quiescent supply current (control inputs)	V_{CC} = 5.5 V; one input at 3.4 V; other inputs at V_{CC} or GND	[2]	-	-	2.5	mA
C_i	input capacitance (control pins)	V_I = 3 V or 0 V		-	4.5	-	pF
$C_{io(off)}$	off-state input/output capacitance	A port; V_O = 3 V or 0 V; $\overline{OE}$ = V_{CC}		-	11.4	-	pF
		B port; V_O = 3 V or 0 V; $\overline{OE}$ = V_{CC}		-	3.8	-	pF
$C_{io(on)}$	on-state input/output capacitance	A port and B port		-	18.6	-	pF
R_{on}	ON-state resistance[3]	V_{CC} = 4.5 V; V_I = 0 V; I_I = 64 mA		-	5	7	Ω
		V_{CC} = 4.5 V; V_I = 0 V; I_I = 30 mA		-	5	7	Ω
		V_{CC} = 4.5 V; V_I = 2.4 V; I_I = −15 mA		-	10	15	Ω

[1] All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C.

[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

[3] Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two (A or B) terminals.

10. Dynamic characteristics

Table 7. Dynamic characteristics

V_{CC} = +5.0 V ± 0.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PD}	propagation delay	from input (nA or nBn) to output (nBn or nA)	[1]	-	-	0.25	ns
		from input (Sn) to output (nA or nBn)		1.2	-	6.2	ns
t_{en}	enable time[2]	from input (Sn) to output (nA or nBn)		1.3	-	6.3	ns
		from input (n$\overline{OE}$) to output (nA or nBn)		1.4	-	6.4	ns
t_{dis}	disable time[3]	from input (Sn) to output (nA or nBn)		1.1	-	7.2	ns
		from input (n$\overline{OE}$) to output (nA or nBn)		1.0	-	7	ns

[1] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

[2] Output enable time to HIGH and LOW level.

[3] Output disable time from HIGH and LOW level.

10.1 AC waveforms

V_I = GND to 3.0 V.

t_{PLZ} and t_{PHZ} are the same as t_{dis}.

t_{PZL} and t_{PZH} are the same as t_{en}.

t_{PLH} and t_{PHL} are the same as t_{PD}.

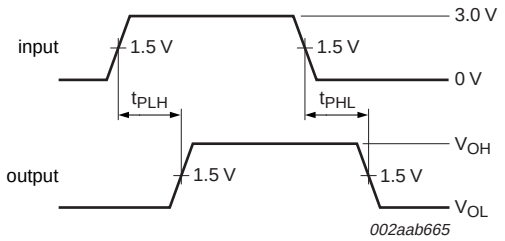
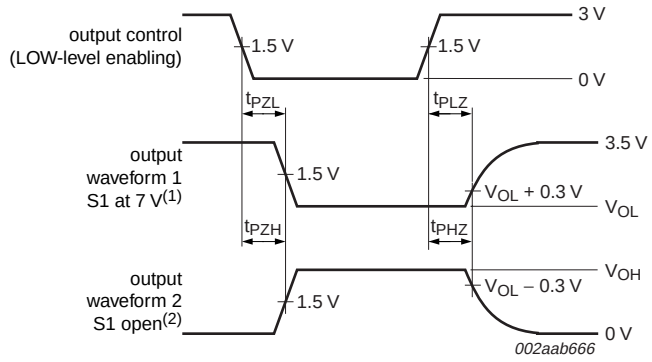


Fig 6. Input to output propagation delay

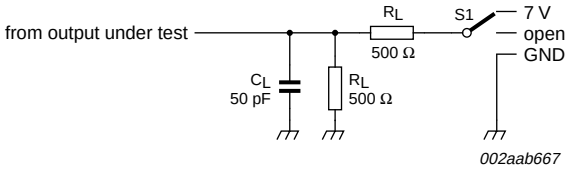


(1) Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control.

(2) Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.

Fig 7. 3-state output enable and disable times

11. Test information



Test data are given in Table 8.

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r ≤ 2.5 ns; t_f ≤ 2.5 ns.

The outputs are measured one at a time with one transition per measurement.

C_L = load capacitance includes jig and probe capacitance.

R_L = load resistance.

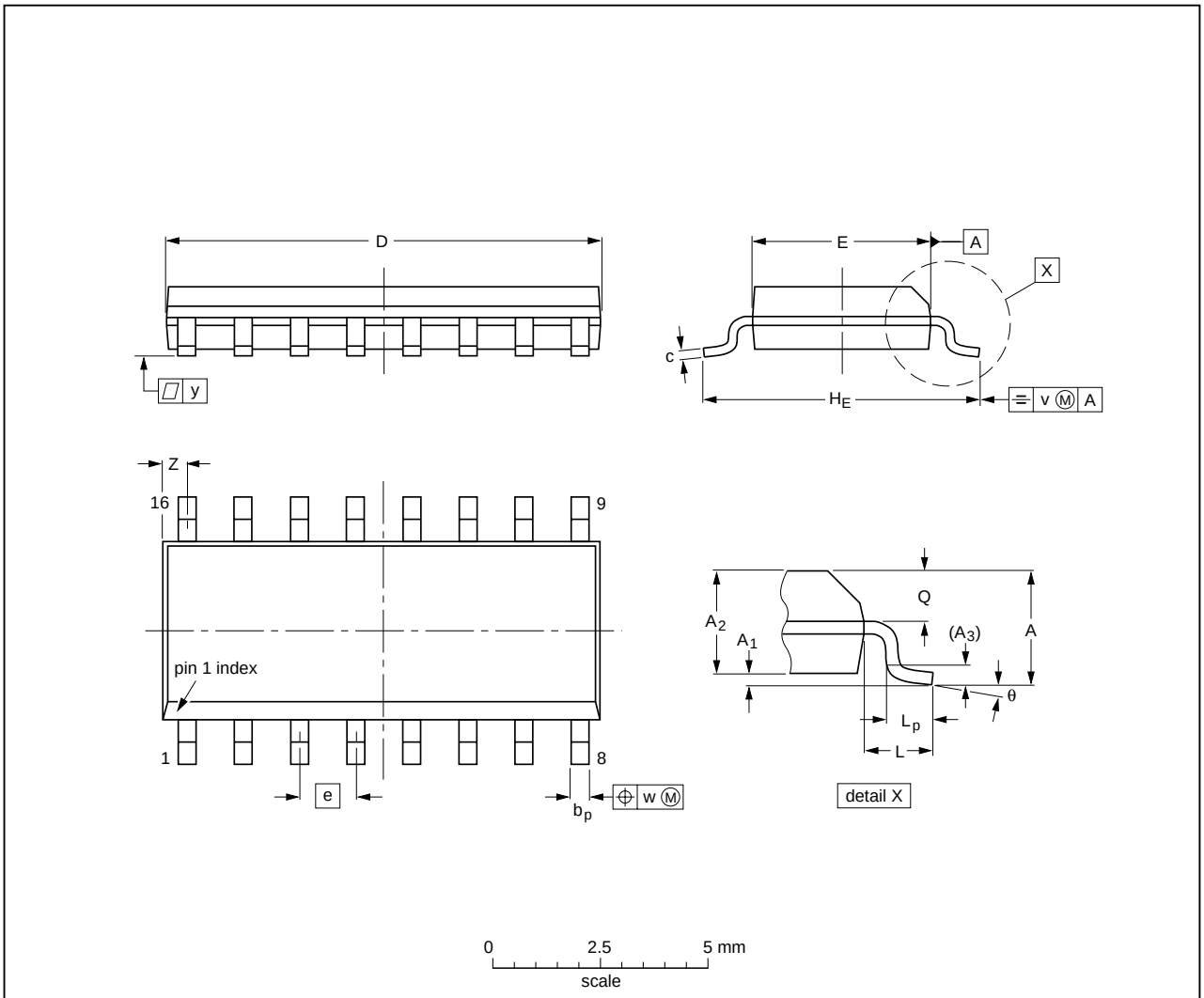
Fig 8. Test circuit

Table 8. Test data

Test	Load		Switch
	C_L	R_L	
t_{PD}	50 pF	500 Ω	open
t_{PLZ}, t_{PZL}	50 pF	500 Ω	7 V
t_{PHZ}, t_{PZH}	50 pF	500 Ω	open

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

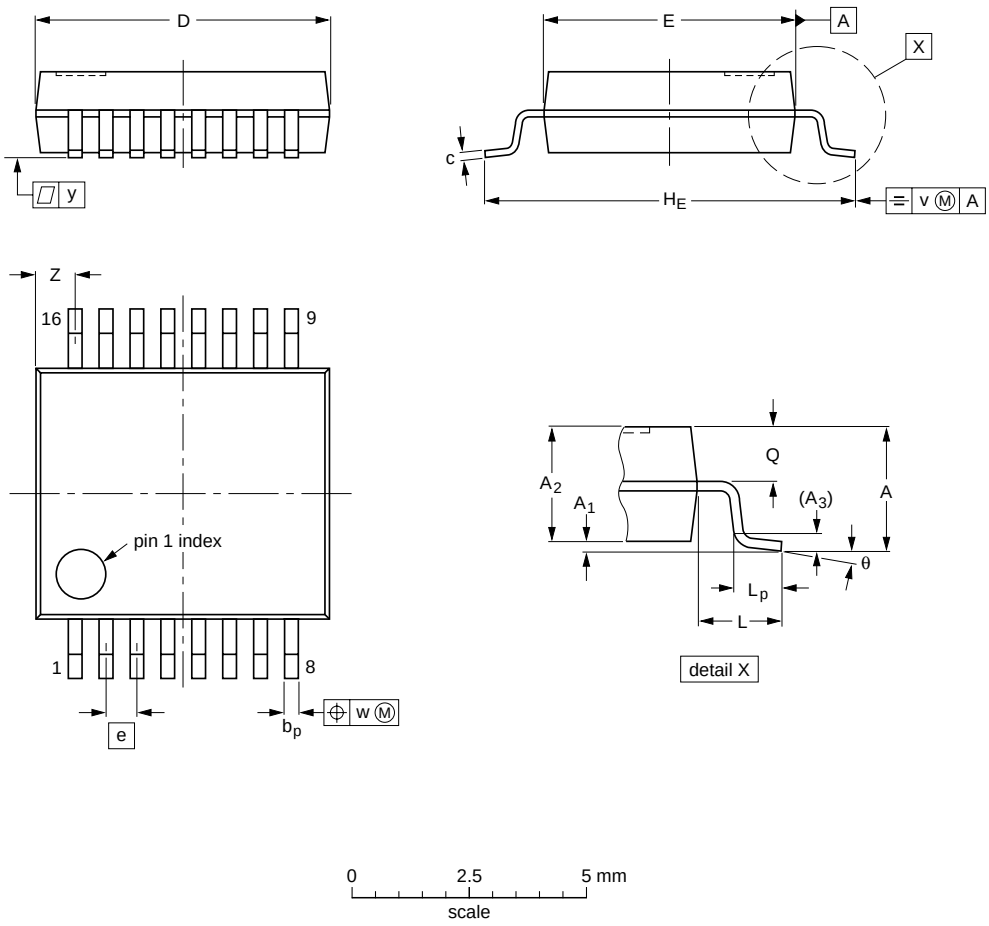
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

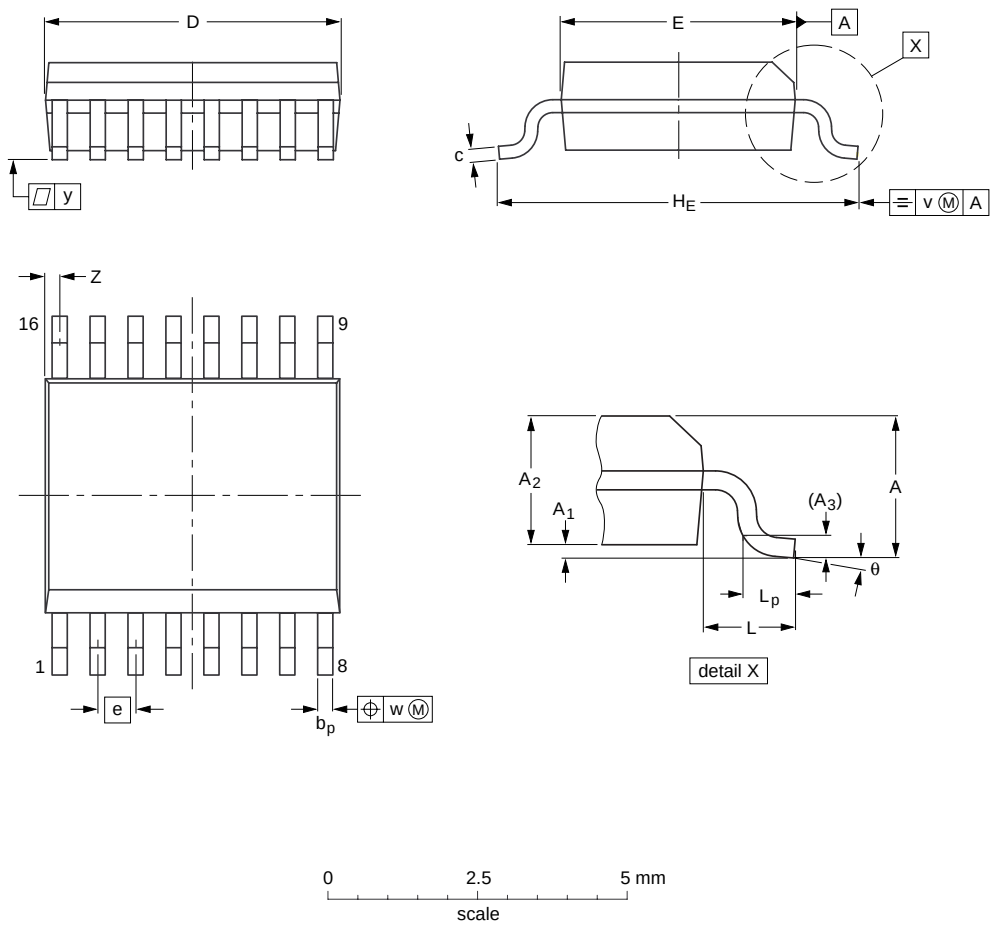
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT338-1 (SSOP16)

SSOP16: plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm **SOT519-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	v	w	y	Z (1)	θ
mm	1.73	0.25 0.10	1.55 1.40	0.25	0.31 0.20	0.25 0.18	5.0 4.8	4.0 3.8	0.635	6.2 5.8	1	0.89 0.41	0.2	0.18	0.09	0.18 0.05	8^o 0^o

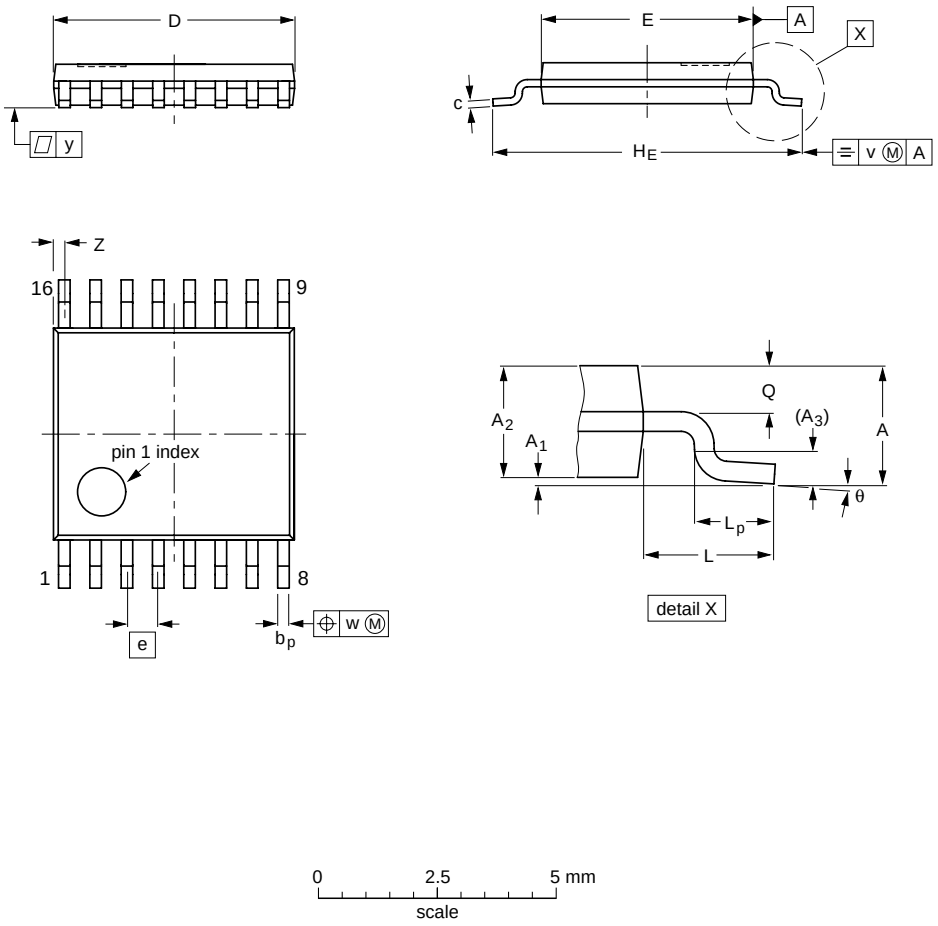
Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT519-1						~~99-05-04~~ 03-02-18

Fig 11. Package outline SOT519-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 12. Package outline SOT403-1 (TSSOP16)

13. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 13) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 9 and 10

Table 9. SnPb eutectic process (from J-STD-020C)

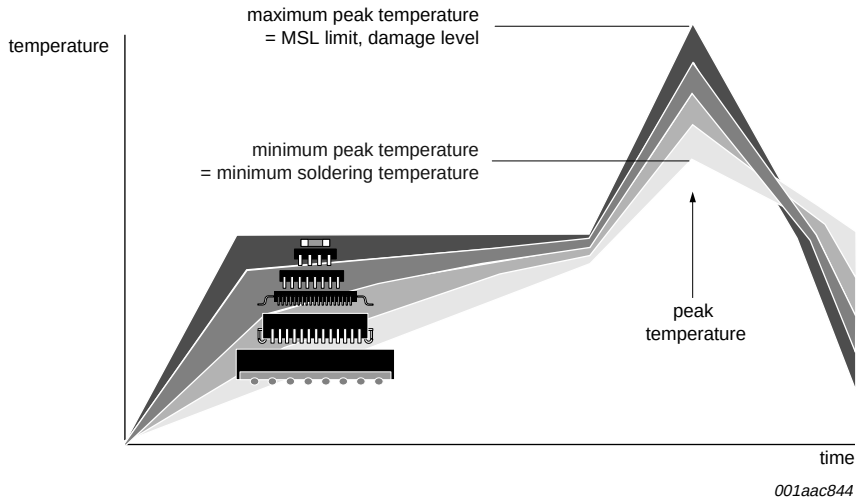
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 10. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 13.



MSL: Moisture Sensitivity Level

Fig 13. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
HBM	Human Body Model
MM	Machine Model
PRR	Pulse Rate Repetition
RC	Resistor-Capacitor network
TTL	Transistor-Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBT3253A_2	20070208	Product data sheet	-	CBT3253A_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 5 “Operating conditions”: – changed (V_{IH}) “HIGH-state input voltage” to “HIGH-level input voltage” – changed (V_{IL}) “LOW-state input voltage” to “LOW-level input voltage” • Table 6 “Static characteristics”: – $C_{io(off)}$, A port: changed Typ. value from 23.5 pF to 11.4 pF – $C_{io(off)}$, B port: changed Typ. value from 6.5 pF to 3.8 pF – added $C_{io(on)}$ specification			
CBT3253A_1 (9397 750 12919)	20051024	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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