45-W Dual-Output Isolated DC/DC Converter

SLTS225 APRIL 2004

Features

- Input Voltage: 36 V to 75 V
- Dual Output (15 V / 15 V) *(Independently Regulated!)*
- Separate Output Returns *(Accommodates ±15 V or +30 V)*
- Internal Power-Up Sequencing
- Flexible On/Off Control
- Output Current Limit
- Fixed Frequency Operation
- Over-Temperature Shutdown
- Under-Voltage Lockout
- 1500 VDC Isolation
- Space-Saving Solderable Case 1.2 sq. in. PCB Area (suffix N)
- Surface Mount Option
- Safety Approvals (Pending): UL 60950, cUL 60950

Description

The PT4711 Excalibur™ power module is a 45-watt rated DC/DC converter that produces two regulated output supply voltages from a standard (–48 V) telecom central office supply.

Both of the outputs from this module are truly independent. Each is separately regulated and has its own negative return. This allows the flexibility of configuring the output for up to three voltage options. This includes a complimentary dual ±15-V, or a single +30-V or –30-V output.

The PT4711 incorporates many features to simplify system integration. These include a flexible On/Off enable control, input under-voltage lock-out, and over-temperature protection. All outputs are short-circuit protected, and internally sequenced for simultaneous power-up and power-down.

The module is packaged in a space-saving solderable copper case, requires no heat sink, and can occupy as little as 1.2 in² of PCB area.

Ordering Information

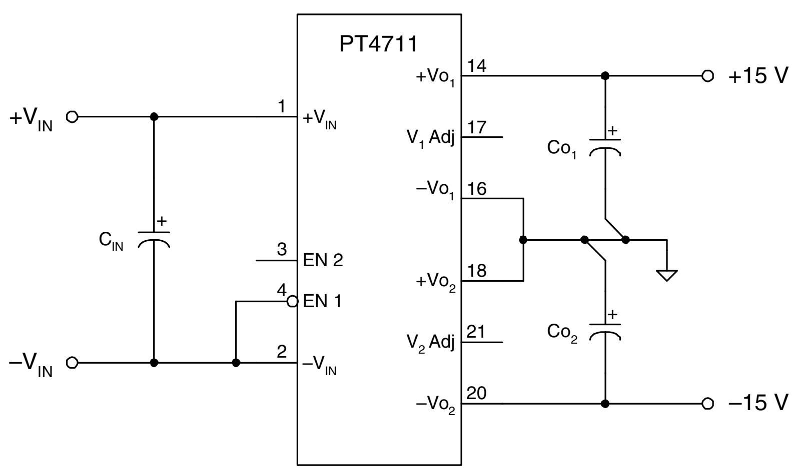
PT4711❑ = 15 V / 15 V

PT Series Suffix (PT1234x)

Case/Pin Configuration	Order Suffix	Package Code
Vertical	**N**	(ENM)
Horizontal	**A**	(ENN)
SMD	**C**	(ENP)

(Reference the applicable package code drawing for the dimensions and PC layout)

Typical Application



Co_1, Co_2:	Recommended 150 µF
Cin:	Optional 47 µF electrolytic
EN1 & EN2 pins:	See On/Off Enable Logic

Pin Configuration

Pin	Function
1	+Vin
2	–Vin
3	EN 2
4	EN 1
5	Do Not Connect
6	Do Not Connect
7	Do Not Connect
8	Pin Not Present
9	Pin Not Present
10	Pin Not Present
11	Pin Not Present
12	Pin Not Present
13	Pin Not Present
14	$+Vo_1$
15	Not Connected
16	$-Vo_1$
17	Vo_1 Adjust
18	$+Vo_2$
19	Not Connected
20	$-Vo_2$
21	Vo_2 Adjust

Note: Shaded functions indicates those pins that are at primary-side potential. All other pins are referenced to the secondary.

On/Off Enable Logic

Pin 3	Pin 4	Output Status
×	1	Off
1	0	On
0	×	Off

Notes:
Logic 1 =Open collector
Logic 0 = –Vin (pin 2) potential

For positive Enable function, connect pin 4 to pin 2 and use pin 3.

For negative Enable function, leave pin 3 open and use pin 4.

Pin Descriptions

+Vin: The positive input supply for the module with respect to $-V_{in}$. When powering the module from a –48-V telecom central office supply, this input is connected to the primary system ground.

–Vin: The negative input supply for the module, and the 0-VDC reference for the EN 1, and EN 2 inputs. When powering the module from a +48-V supply, this input is connected to the input source return.

EN 1: The negative logic input that activates the module output. This pin must be connected to $-V_{in}$ to enable the module's outputs. A high impedance disables the module's outputs.

EN 2: The positive logic input that activates the module output. If not used, this pin should be left open circuit. Connecting this input to $-V_{in}$ disables the module's outputs.

+Vo 1: This is the positive DC output voltage with respect to $-Vo_1$. The output voltage produced across $\pm Vo_1$ is electrically isolated from $\pm V_{in}$ and independently regulated from that produced at $\pm Vo_2$. If the $+Vo_1$ node is connected to the secondary ground, a negative output voltage will be produced at $-Vo_1$.

–Vo 1: The negative output supply voltage with respect to $+Vo_1$. If this node is connected to the secondary ground, a positive voltage is produced at $+Vo_1$.

+Vo 2: This is the positive DC output voltage with respect to $-Vo_2$. The output voltage produced across $\pm Vo_2$ is electrically isolated from $\pm V_{in}$ and independently regulated from that produced at $\pm Vo_1$. If $+Vo_2$ node is connected to the secondary ground, a negative output voltage will be produced at $-Vo_2$.

–Vo 2: The negative output supply voltage with respect to $+Vo_2$. If this node is connected to the secondary ground, a positive voltage is produced at $+Vo_2$.

±Vo1 Adjust: Using a single resistor, this pin allows the output voltage produced at $\pm Vo_1$ to be adjusted higher or lower by up to 10%. If not used this pin should be left open circuit.

±Vo2 Adjust: Using a single resistor, this pin allows the output voltage produced at $\pm Vo_2$ to be adjusted higher or lower by up to 10%. If not used this pin should be left open circuit.

PT4711 Electrical Specifications

(Unless otherwise stated, the operating conditions are:- T_a =25°C, V_{in} =48 V, and I_o =$I_o$max)

Characteristics	Symbols	Conditions	PT4711 Min	Typ	Max	Units
Output Current	Io_1, Io_2	Both outputs	0	—	1.5	A
Input Voltage Range	V_{in}	Continuous Surge (1 minute)	36 —	— —	75 80	V
Set-Point Voltage	Vo_1, Vo_2		14.55	15.0	15.45	V
Temperature Variation	ΔReg_{temp}	–40°C ≤T_a ≤+85°C, I_o =$I_o$min — Vo_1, Vo_2	—	±0.5	—	%V_o
Line Regulation	ΔReg_{line}	All outputs, Over V_{in} range	—	±0.05	±0.25	%V_o
Load Regulation	ΔReg_{load}	All outputs, 0≤I_o≤$I_o$max	—	±0.2	±0.5	%V_o
Cross Regulation	ΔReg_{cross}	Io_1 =Io_1max, 0 ≤ Io_2 ≤ Io_2max Io_2 =Io_2max, 0 ≤ Io_1 ≤ Io_1max	—	±10	—	mV
Total Output Voltage Variation	ΔV_o tot	Includes set-point, line, load, –40°C ≤T_a ≤+85°C — Vo_1 , Vo_2	14.25	—	15.75	V
Efficiency	η		—	86	—	%
V_o Ripple (pk-pk)	V_n	Measured from each output to COM, 0 to 20 MHz bandwidth — Vo_1, Vo_2	—	15	—	mV_{pp}
Transient Response	t_{tr} V_{os}	0.1 A/µs load step, 50% to 75% $I_o$max V_o over/undershoot	— —	100 2	— —	µSec %V_o
Output Adjust Range	Vo_x adj	Each V_o adjusted independently	—	±10	—	%V_o
Current Limit Threshold	Io_{LIM}	Shutdown, auto restart — Vo_1, Vo_2	—	2.5	—	A
Switching Frequency	f_s	Over V_{in} and I_o ranges	550	600	650	kHz
Under Voltage Lockout	V_{on} V_{off}	V_{in} increasing V_{in} decreasing	— —	34 32	— —	V
Enable Control (pins 3 & 4) High-Level Input Voltage Low-Level Input Voltage	 V_{IH} V_{IL}	Referenced to –V_{in} (pin 2)	 4 –0.2	 — —	 Open (1) 0.8 (1)	V
Low-Level Input Current	I_{IL}	Pin connected to –V_{in} (pin 2)	—	–0.16	—	mA
Standby Input Current	I_{in} standby	pins 3 & 4 open circuit	—	5	20	mA
Internal Input Capacitance	C_{int}		—	1	—	µF
External Output Capacitance	C_o	Each output to COM — Vo_1, Vo_2	0	—	500	µF
Primary/Secondary Isolation	V_{iso} C_{iso} R_{iso}		1500 — 10	— 2,200 —	— — —	V pF MΩ
Secondary Working Voltage	ΔV_{sec}	Between any two output pins	—	—	35 (2)	V
Operating Temperature Range	T_a	Over V_{in} Range	–40	—	85 (3)	°C
Solder Reflow Temperature	T_{reflow}	Surface temperature of module pins or case	—	—	215 (4)	°C
Storage Temperature	T_s	—	–40	—	125	°C
Mechanical Shock		Per Mil-STD-883D, Method 2002.3 1 msec, ½ Sine, mounted	—	500	—	G's
Mechanical Vibration		Mil-STD-883D, Method 2007.2 — Suffix A 20-2000 Hz — Suffix N, C	— —	15 (5) 20 (5)	— —	G's
Weight	—	Vertical/Horizontal	—	50	—	grams
Shutdown Temperature	OTP			115	125	°C
Flammability	—	Meets UL 94V-O				

Notes: (1) *The Enable inputs (pins 3 & 4) have internal pull-ups. Leaving pin 3 open-circuit and connecting pin 4 to –V_{in} allows the the converter to operate when input power is applied. The maximum open-circuit voltage is 5 V.*

(2) *The maximum voltage that may exist between any two output pins.*

(3) *See SOA curves or consult factory for appropriate derating.*

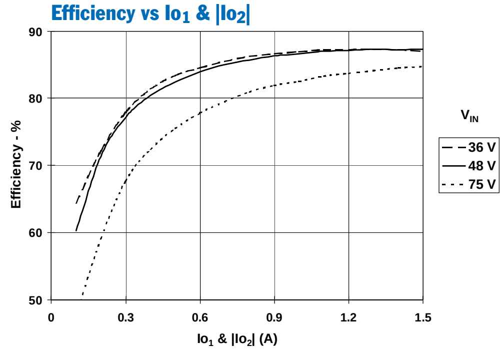
(4) *During solder reflow of SMD package version, do not elevate the module case, pins, or internal component temperatures above a peak of 215°C. For further guidance refer to the application note, "Reflow Soldering Requirements for Plug-in Power Surface Mount Products," (SLTA051).*

(5) *Only the case pins on through-hole pin configurations (N & A) must be soldered. For more information see the applicable package outline drawing.*

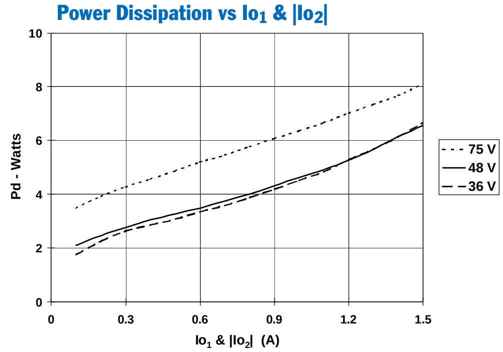
Performance Characteristics; V_{in} =48 V (See Note A)

(Refer to typical application for output configuration)

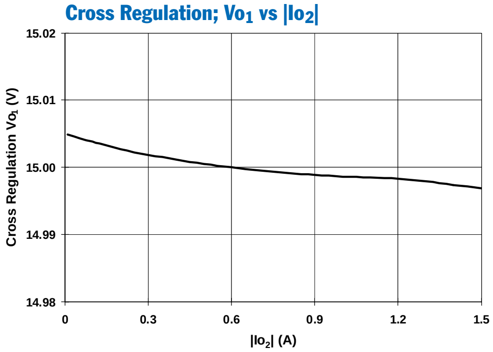
Efficiency vs Io_1 & $|Io_2|$



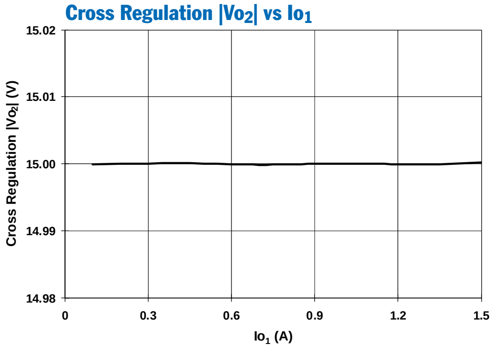
Power Dissipation vs Io_1 & $|Io_2|$



Cross Regulation; Vo_1 vs $|Io_2|$



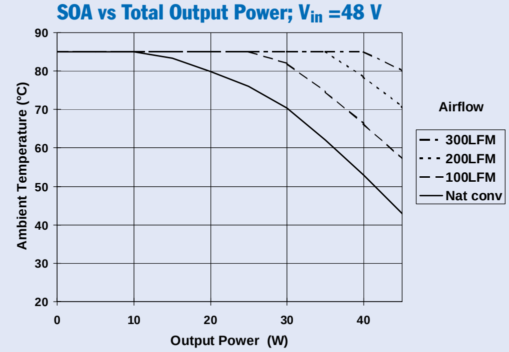
Cross Regulation $|Vo_2|$ vs Io_1



PT4711 Safe Operating Area (SOA) (See Note B)

(All outputs proportionally loaded from 0 to 100 % of full load)

SOA vs Total Output Power; V_{in} =48 V



Note A: *All Characteristic data in the above graphs has been developed from actual products tested at 25°C. This data is considered typical data for the ISR.*
Note B: *SOA curves represent operating conditions at which the internal components are at or below the manufacturer's maximum rated operating temperatures.*

Operating Features of the PT4711 Dual-Output DC/DC Converter

Over-Current Protection

Each of the two outputs from the PT4711 DC/DC converter incorporates protection against an output load fault. When a fault impedance is applied to one output, the module initially limits the output current of that output to approximately 150% of the maximum current rating. If the fault persists for more than 20 ms the converter shuts down, forcing the voltage at both regulated outputs to simultaneously fall to zero. Following shutdown the converter periodically attempts to recover by executing a soft-start power-up. The converter will contine in a cycle of successive shutdowns and restarts until the load fault is removed.

Over-Temperature Protection

The PT4711 DC/DC converter has an internal temperature sensor, which monitors the temperature of the module's internal components. If the sensed temperature exceeds a nominal 115°C, the converter will shut down. The converter will automatically restart when the sensed temperature returns to about 100°C.

Under-Voltage Lock-Out

The Under-Voltage Lock-Out (UVLO) circuit prevents operation of the converter whenever the input voltage to the module is insufficient to maintain output regulation. The UVLO has approximately 2 V of hysterisis. This is to prevent oscillation with a slowly changing input voltage. Below the UVLO threshold the module is off and the enable control inputs, EN1 and EN2 are inoperative.

Primary-Secondary Isolation

The PT4711 DC/DC converter incorporates electrical isolation between the input terminals (primary) and the output terminals (secondary). All converters are production tested to a withstand voltage of 1500 VDC. The isolation complies with UL/cUL 60950 and EN60950, and the requirements for operational isolation. This allows the converter to be configured for either a positive or negative input voltage source.

The regulation control circuitry for these modules is located on the secondary (output) side of the isolation barrier. Control signals are passed between the primary and secondary sides of the converter. The data sheet 'Pin Descriptions' and 'Pin-Out Information' provides guidance as to which reference (primary or secondary) that must be used for each of the external control pin.

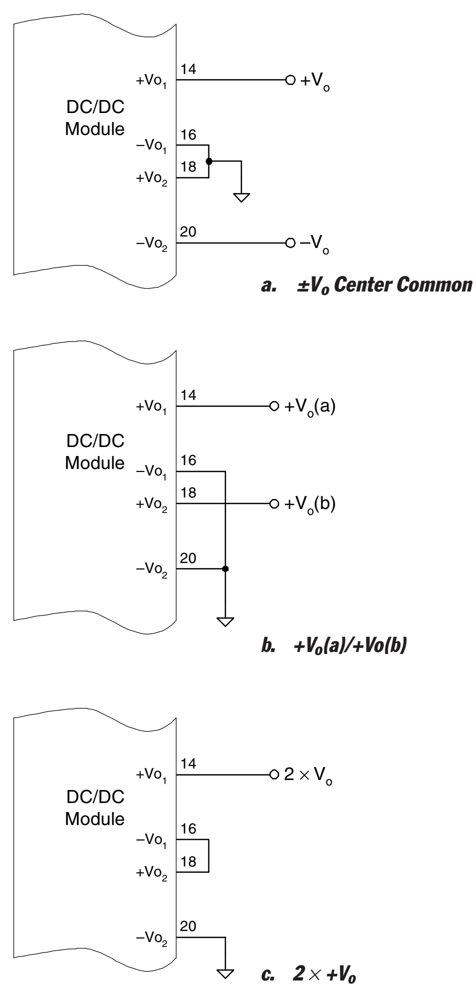
Input Current Limiting

The converter is not internally fused. For safety and overall system protection, the maximum input current to the converter must be limited. Active or passive current limiting can be used. Passive current limiting can be a fast acting fuse. A 125-V fuse, rated no more than 5 A, is recommended. Active current limiting can be implemented with a current limited "Hot-Swap" controller.

Output Voltage Configurations

Both outputs from the PT4711 DC/DC converter are independently regulated and isolated from each other. This allows flexibility to how the output voltages may be configured (up to the maximum allowed working voltage between the two outputs; see specification table). Figure 1-1 shows the most common ways that the outputs of the converter may be configured. They include $\pm V_O$ (Fig. 1-1a), $V_O(a)/V_O(b)$ (Fig. 1-1b), and $2 \times V_O$ (Fig. 1-1c).

Figure 1-1; PT4711 Output Voltage Configurations



a. $\pm V_o$ Center Common

b. $+V_o(a)/+Vo(b)$

c. $2 \times +V_o$

Using the On/Off Enable Controls on the PT4711 Dual-Output DC/DC Converter

The PT4711 is a dual-output DC/DC converter incorporates two output enable controls. EN1 (pin 4) is the *Negative Enable* input, and EN2 (pin 3) is the *Positive Enable* input. Both inputs are electrically referenced to $-V_{in}$ (pin 2) on the primary or input side of the converter. A pull-up resistor is not required, but may be added if desired. Voltages of up to 70 V can be safely applied to the either of the *Enable* pins.

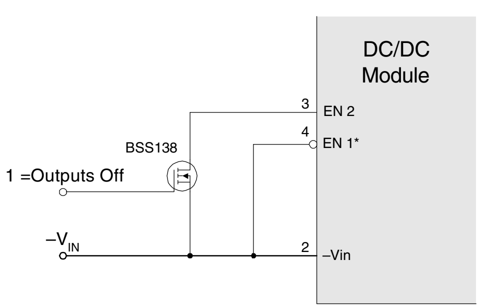
Automatic (UVLO) Power-Up

Connecting EN1 (pin 4) to $-V_{in}$ (pin 2) and leaving EN2 (pin 3) open-circuit configures the converter for automatic power up. (See data sheet "Typical Application"). The converter control circuitry incorporates an "Under Voltage Lockout" (UVLO) function, which disables the converter until the minimum specified input voltage is present at $\pm V_{in}$. (See data sheet Specifications). The UVLO circuitry ensures a clean transition during power-up and power-down, allowing the converter to tolerate a slow-rising input voltage. For most applications EN1 and EN2, can be configured for automatic power-up.

Positive Output Enable (Negative Inhibit)

To configure the converter for a positive enable function, connect EN1 (pin 4) to $-V_{in}$ (pin 2), and apply the system On/Off control signal to EN2 (pin 3). In this configuration, a low-level input voltage ($-V_{in}$ potential) applied to pin 3 disables the converter outputs. Figure 1 is an example of this configuration.

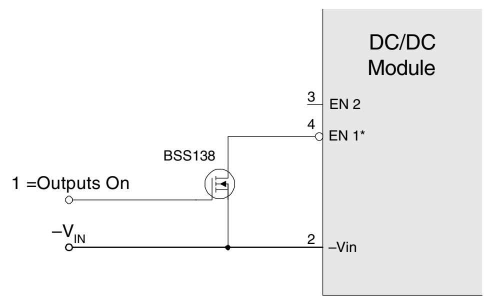
Figure 1; Positive Enable Configuration



Negative Output Enable (Positive Inhibit)

To configure the converter for a negative enable function, EN2 (pin 3) is left open circuit, and the system On/Off control signal is applied to EN1 (pin 4). A low-level input voltage ($-V_{in}$ potential) must then be applied to pin 4 in order to enable the outputs of the converter. An example of this configuration is detailed in Figure 2. *<u>Note</u>: The converter will only produce an output voltage if a valid input voltage is applied to* $\pm V_{in}$.

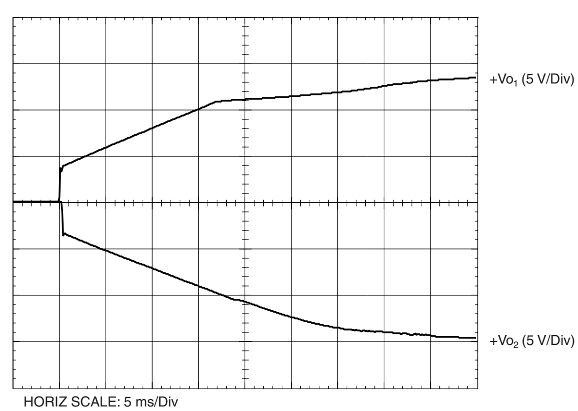
Figure 2; Negative Enable Configuration



On/Off Output Voltage Sequencing

Both outputs from the PT4711 converter are internally sequenced to power up in unison. Figure 3-3 shows the output waveforms after the module's output has been enabled. The converter produces a fully regulated output within 75 ms. The waveforms were measured with the output voltages configured per Figure 1-1a (for ±15-V output). A constant current load of 1.5 A was applied to both outputs, with an input source of 48 VDC.

Figure 3-3; PT4711 Power-up Sequence

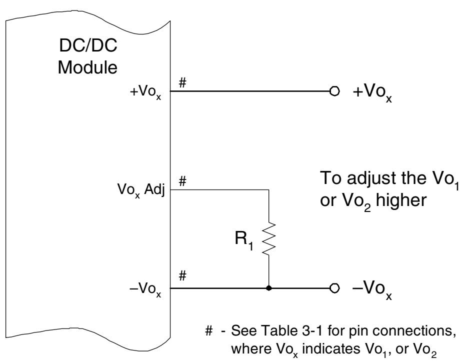


Adjusting the Output Voltages of the PT4711 Dual-Output DC/DC Converters

The PT4711 dual-output DC/DC converter produces two independently regulated output voltages. The magnitude of each output may be trimmed higher or lower than the nominal set-point by up to 10%. The adjustment method uses a single external resistor. [1] The value of the resistor determines the magnitude of adjustment, and the location of the resistor determines the direction of adjustment (increase or decrease). The resistor values can be calculated using a formula (see below). Alternatively the resistor value may be selected directly from the values given in Table 2-2. The placement of each resistor is as follows.

Adjust Up: To increase the magnitude of the output voltage, add a resistor R_1 between the appropriate *Vo_x Adj* ('Vo_1 Adj' or 'Vo_2 Adj') and the respective *-Vo_x* voltage rail. See Figure 2-1(a) and Table 2-1 for the resistor placement and pin connections.

Figure 2-1a



Notes:

1. Use only a single 1% (or better) tolerance resistor in either the R_1 or (R_2) location to adjust a specific output. Place the resistor as close to the ISR as possible.
2. Never connect capacitors to any of the 'Vo_x Adj' pins. Any capacitance added to these control pins will affect the stability of the respective regulated output.

Adjust Down: To decrease the magnitude of the output voltage, add a resistor (R_2), between the appropriate *Vo_x Adj* (Vo_1 Adj or Vo_2 Adj,) and the respective *+Vo_x* voltage rail. See Figure 2-1(b) and Table 2-1 for the resistor placement and pin connections.

Figure 2-1b

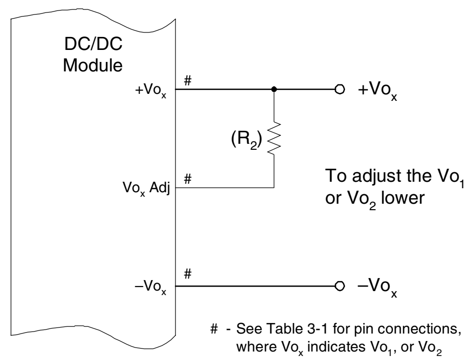


Table 2-1; Adjust Resistor Pin Connections

	To Adjust Up Connect R_1		To Adjust Down Connect (R_2)	
	from Vo_x Adj	to $-Vo_x$	from Vo_x Adj	to $+Vo_x$
Vo_1	17	16	17	14
Vo_2	21	20	21	18

Calculation of Resistor Adjust Values

The adjust resistor value may also be calculated using an equation. Note that the equation for R_1 [Adjust Up] is different to that for (R_2) [Adjust Down].

$$R_1 \text{ [Adjust Up]} = \frac{35.75}{(V_a - V_o)} - 20 \quad \text{k}\Omega$$

$$(R_2) \text{ [Adjust Down]} = \frac{14.3\,(V_a - 2.5)}{(V_o - V_a)} - 20 \quad \text{k}\Omega$$

Where: V_o = Original output voltage (Vo_x)
V_a = Adjusted output voltage (Va_x)

Table 2-2

ADJUSTMENT RESISTOR VALUES FOR Vo_1 & Vo_2

Adj. Resistor		R_1/(R_2)
% Adjust	V_a(req'd)	
–10%	13.50 V	(84.9) kΩ
– 9%	13.65 V	(98.1) kΩ
– 8%	13.80 V	(115) kΩ
– 7%	13.95 V	(136) kΩ
– 6%	14.10 V	(164) kΩ
– 5%	14.25 V	(204) kΩ
– 4%	14.40 V	(264) kΩ
– 3%	14.55 V	(363) kΩ
– 2%	14.70 V	(562) kΩ
– 1%	14.85 V	(1.16) MΩ
0%	15.00 V	
+ 1%	15.15 V	218 kΩ
+ 2%	15.30 V	99.2 kΩ
+ 3%	15.45 V	59.4 kΩ
+ 4%	15.60 V	39.6 kΩ
+ 5%	15.75 V	27.7 kΩ
+ 6%	15.90 V	19.7 kΩ
+ 7%	16.05 V	14.0 kΩ
+ 8%	16.20 V	9.8 kΩ
+ 9%	16.35 V	6.5 kΩ
+10%	16.50 V	3.8 kΩ

R_1 = Black, R_2 = (Blue)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
PT4711A	ACTIVE	SIP MODULE	ENN	21	8	TBD	Call TI	Level-1-215C-UNLIM
PT4711C	ACTIVE	SIP MODULE	ENP	21	8	TBD	Call TI	Level-3-215C-168HRS
PT4711N	ACTIVE	SIP MODULE	ENM	21	8	TBD	Call TI	Level-1-215C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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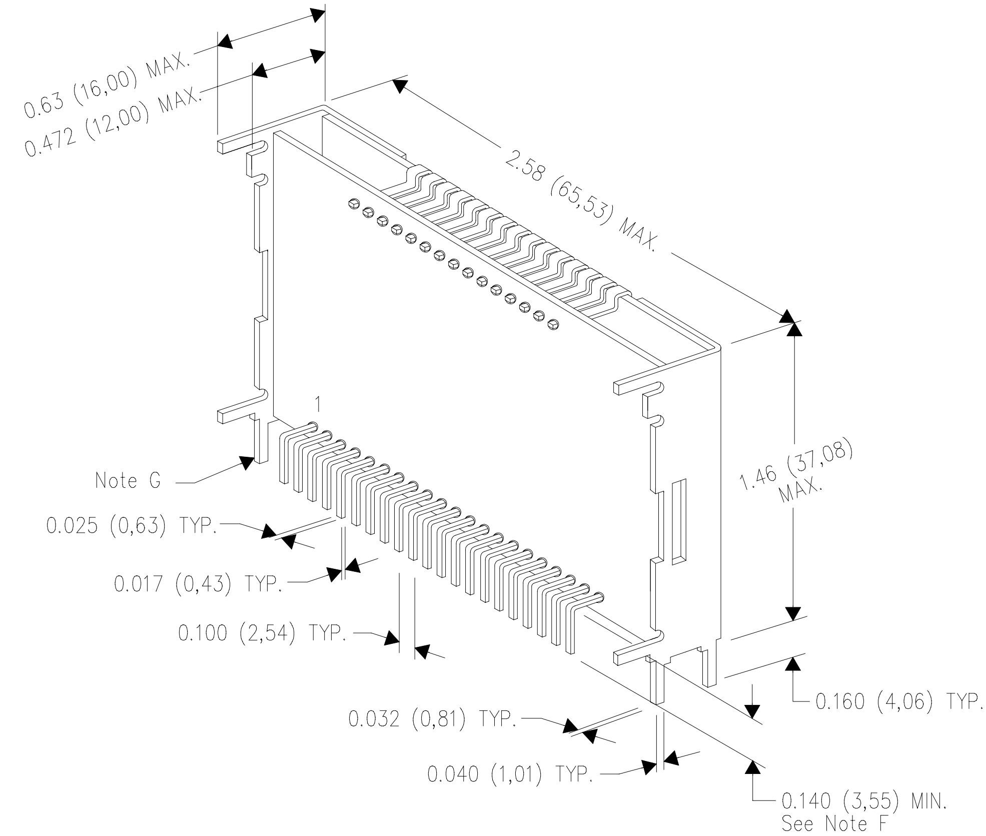
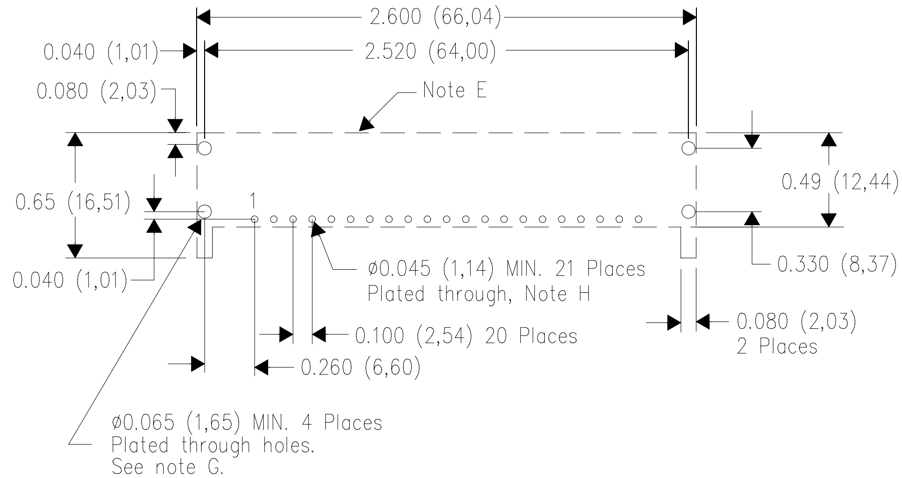
Suffix N





PC LAYOUT

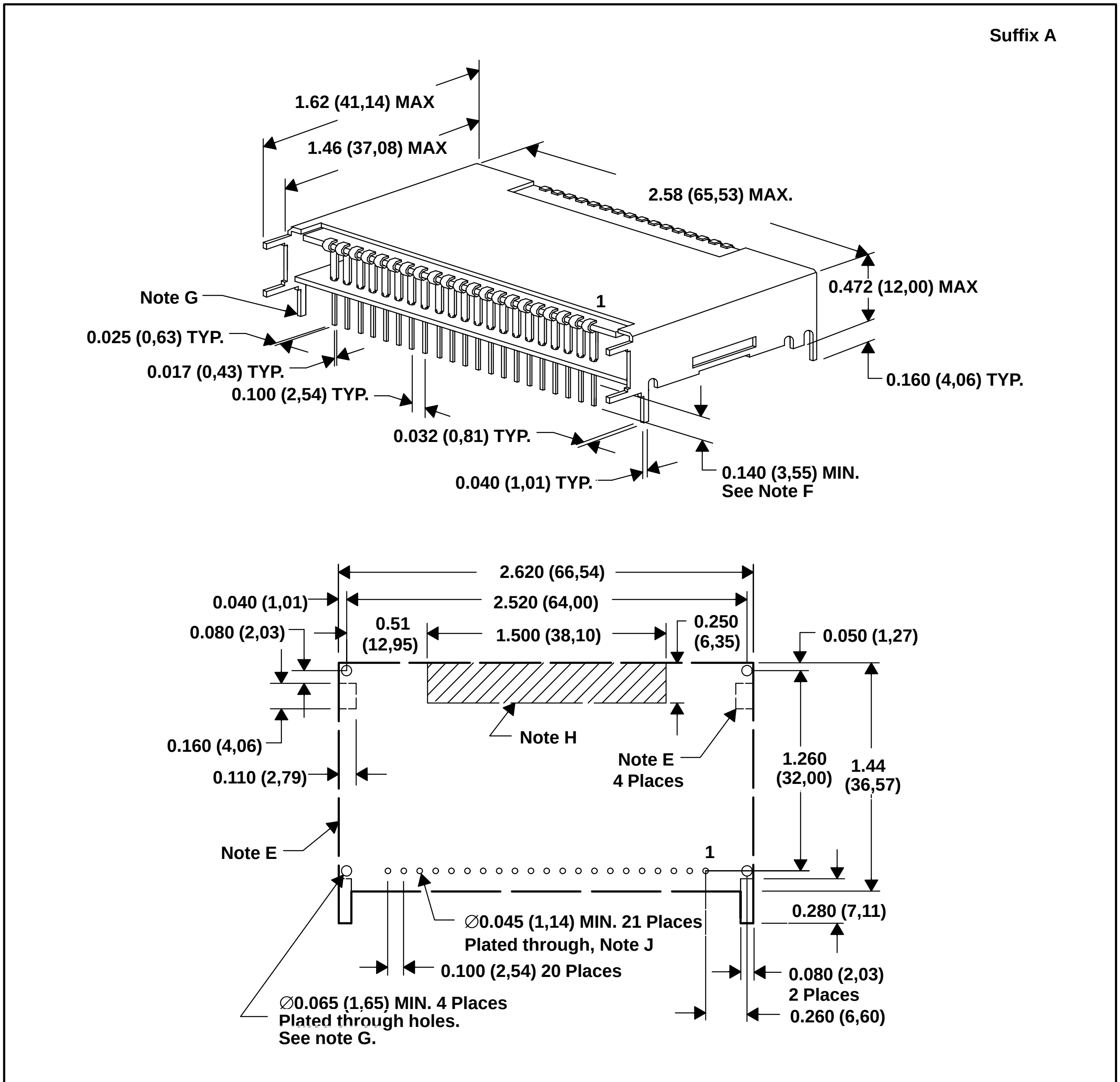
4203486/B 02/03

NOTES:

A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended mechanical keep out area.
F. Electrical pin length mounted on printed circuit board, from seating plane to pin end.
G. The case is electrically uncommitted. The recommended connection is to secondary ground.
H. Some pins may not be present, see product specifications.

SCALE	SIZE		REV	SHEET
1X	A	4203486	B	2/3

ENN (R–MSIP–T21) **METAL SINGLE–IN–LINE MODULE**

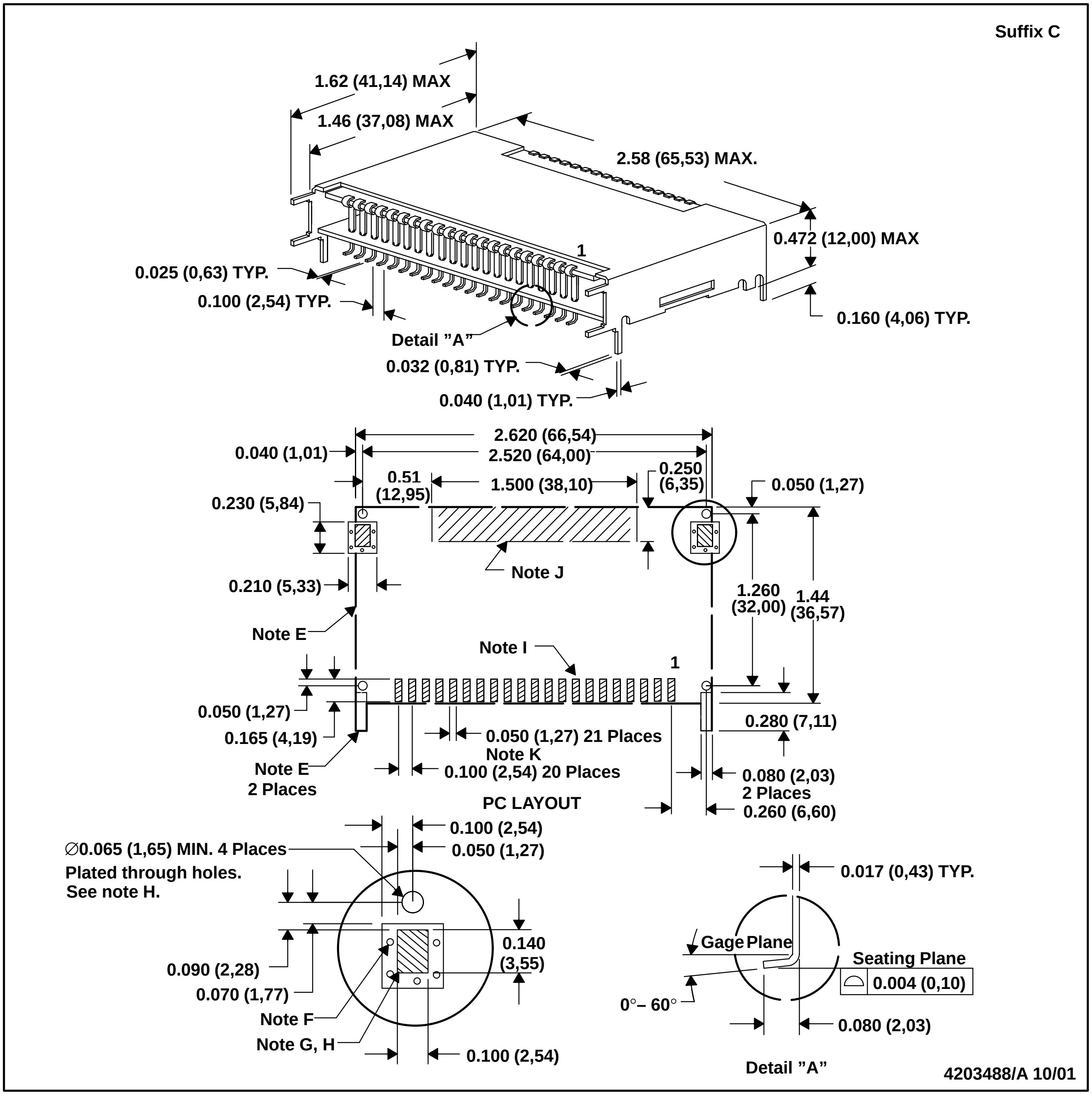


PC LAYOUT

4203487/A 10/01

NOTES:
- A. All linear dimensions are in inches (mm).
- B. This drawing is subject to change without notice.
- C. 2 place decimals are ±0.030 (±0,76mm).
- D. 3 place decimals are ±0.010 (±0,25mm).
- E. Recommended mechanical keep out area.
- F. Electrical pin length mounted on printed circuit board, from seating plane to pin end.
- G. The case is electrically uncommitted. The recommended connection is to secondary ground.
- H. No copper, power or signal traces in this area.
- J. Some pins may not be present, see product specifications.

ENP (R–MSIP–G21) METAL SINGLE–IN–LINE MODULE



NOTES:
- A. All linear dimensions are in inches (mm).
- B. This drawing is subject to change without notice.
- C. 2 place decimals are ±0.030 (±0,76mm).
- D. 3 place decimals are ±0.010 (±0,25mm).
- E. Recommended mechanical keep out area.
- F. Vias are recommended to improve copper adhesion.
- G. Solder mask openings to copper island for solder joints to mechanical pins.
- H. The case is electrically uncommitted. The recommended connection is to secondary ground.
- I. Power pin connections should utilize two or more vias per input, ground and output pin.
- J. No copper, power or signal traces in this area.
- K. Some pins may not be present, see product specifications.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

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Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265