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Fax: 886-2-29174598
URL: http://www.princeton.com.tw

2-Channel 300mW Class AB Power Amplifier **PT2308P**

DESCRIPTION

PT2308P is a 2 channel Class AB stereo speaker driver utilizing CMOS technology designed by AB push-pull, the original sound will be low distortion amplify and low consumption. The power of PT2308P will be reach 300mW on THD=10% and deliver 8Ω load.

FEATURES

- Wild operating temperature large
- Excellent Power Signal-to-Noise Repel Rate (PSRR)
- Low static state current consumption
- Output power (THD=10%)
  - Load is 16Ω/190mW
  - Load is 8Ω/300mW
- Low harmonics distortion (THD=0.03%)
- Large output amplitude

APPLICATIONS

- Walkman
- Portable audio
- HI-FI audio system
- CD-ROM

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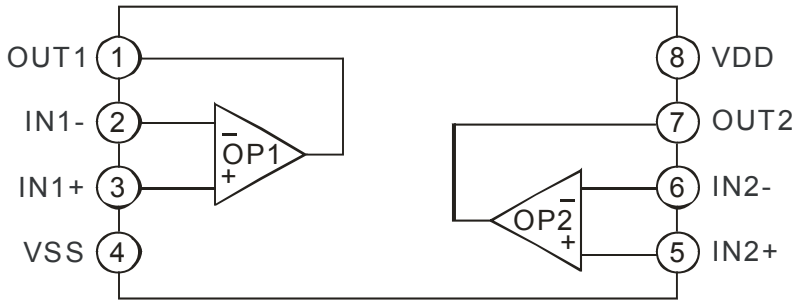
BLOCK DIAGRAM



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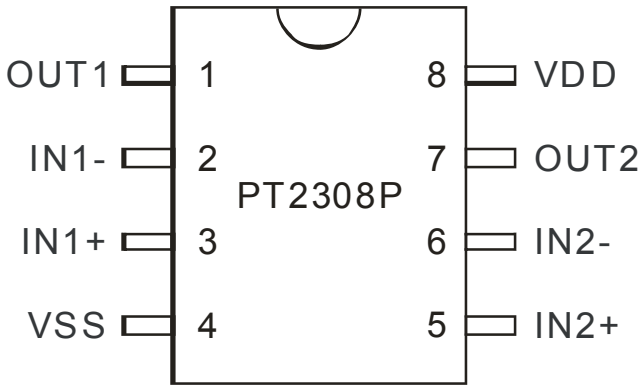
PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
OUT1	O	Output pin 1	1
IN1-	I	Inverting input pin 1	2
IN1+	I	Non-inverting input pin 1	3
VSS	-	Negative power supply	4
IN2+	I	Non-inverting input pin 2	5
IN2-	I	Inverting input pin 2	6
OUT2	O	Output pin 2	7
VDD	-	Positive power supply	8

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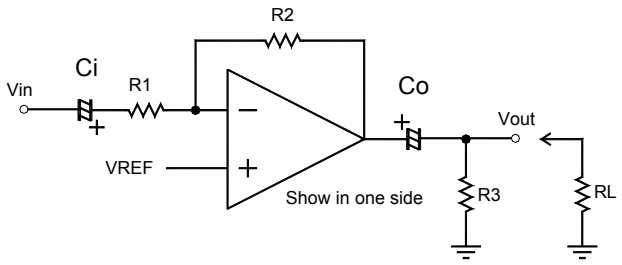
BASIC APPLICATION DESCRIPTION

PT2308P is a low power amplifier which operates with a 5V input voltage, it can be used to drive regular earphones or low power speakers with a load resistance of 8ohm or higher. The operation mechanics is much like the typical OPAMP. (The picture below shows the basic application circuit of PT2308P as an inverted amplifier).



PT2308P Typical Application Circuit

1. Gain Settings
   The inverted amplifier's amplification is equal to the ratio between R2 and R1 (Av= -(R2÷R1)). Please take note that the maximum supply voltage for the PT2308P is 5V, voltage gain setting should depend on the input level amplitude; too much voltage gain may increase the chance of causing clipping at the output.

2. VREF
   Because the PT2308P operates with a single power source, to ensure the best output performance, the suggested value for VREF is 1/2 VDD.

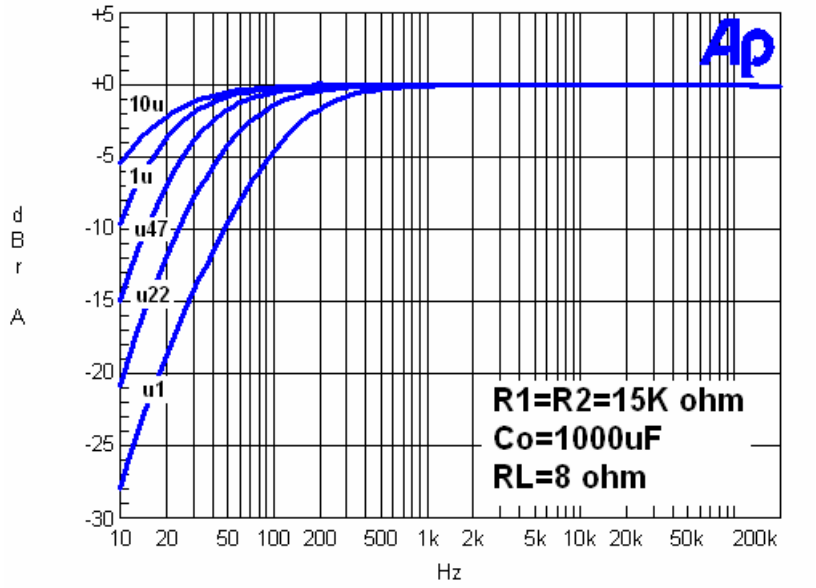
3. Input Coupling Capacitor Ci

In typical applications, this input coupling capacitor transfers signals between the input and PT2308P, it allows block DC bias of the PT2308P flowing into input signal, and thus the user must be aware of the voltage tolerance and the polarity of this Cap.

Referring to the diagram above, Ci and R1 forms a 1st order high-pass filter; the lower-cutoff frequency is determined by the equation:

$$f_{c(highpass)}=1/2\pi R1Ci$$

The diagram below shows the frequency response when: Ci=10μF/1μF/0.47μF/0.22μF/0.1μF

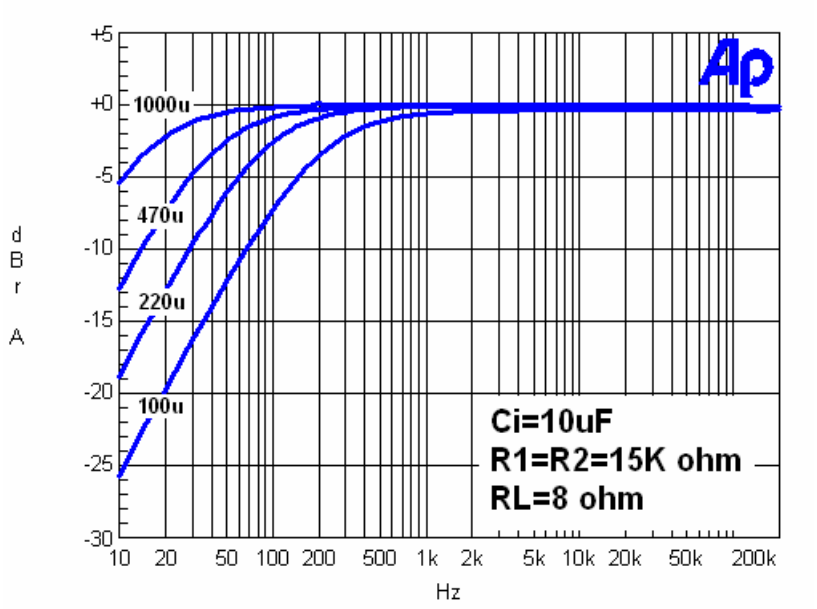


4. Output Coupling Capacitor Co

Single power single-ended (SE) configuration generates a DC bias at the output of the amplifier; a coupling capacitor must be placed at the output to block the DC bias from being sent to the load and connect a RL at the signal output terminal. The low cut-off frequency may be needs to adjust to correspond to different load (speaker or earphone) specifications. Similar to the input coupling capacitor, the output coupling capacitor and impedance of the load form a 1st order high-pass filter, the low cut-off frequency is determined by the equation:

$$f_{c(highpass)}=1/2\pi R_L Co$$

The diagram below shows the frequency response when: Co=1000μF/470μF/220μF/100μF.



5. Discharging Resistor (R3)

When the PT2308 is powered ON, the output coupling capacitor Co will start charging. When there is no load connected at Vout, there will be a DC voltage present. At this time, if a load is suddenly connected (usually earphone or speaker for general applications), the charged Co will then discharge through Vout to the load, causing a very loud popping sound, thus, it is recommended to connect a R3 to regulate the discharge of Co.

The time it takes to discharge is T=CoR3.

The recommended resistance value for R3 is between 1KΩ ~ 10KΩ, to prevent loading effect from the amplifier. If the load (ex. Speaker) is permanently connected then R3 can be neglected.

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ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	8	V
Operating temperature	Topr	-40~+85	℃
Storage temperature	Tstg	-65~+150	℃

ELECTRONICAL CHARACTERISTICS

(Unless otherwise specified, V_{DD}=5V, V_{SS}=0V, Ta=25℃, fin=1KHz, RL=8Ω)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		2.7	5	5.5	V
Supply current	I_{DD}	No Load	-	3	4	mA
Input offset voltage	$V_{I(OS)}$		-	5	50	mV
Total harmonic distortion	THD+N	PO=200mW, RL=8Ω, F=1KHZ	-	0.04	0.1	%
		PO=120mW, RL=16Ω, F=1KHZ	-	0.03	0.06	%
Maximum Output Power	PO	THD=0.2%, f=1KHz, RL=8Ω	200	250	-	mW
		THD=0.2%, f=1KHz, RL=16Ω	100	130	-	mW
		THD=10%, f=1KHz, RL=8Ω	250	300	-	mW
		THD=10%, f=1KHz, RL=16Ω	160	190	-	mW
Output noise	VN		-	20	50	μV
VDD=3V						
Supply current	I_{DD}	No Load	-	2	3	mA
Input offset voltage	$V_{I(OS)}$		-	5	50	mV
Total harmonic distortion	THD+N	PO=50mW, RL=8Ω, F=1KHZ	-	0.02	0.05	%
		PO=40mW, RL=16Ω, F=1KHZ	-	0.02	0.05	%
Maximum output power	PO	THD=0.2%, f=1KHz, RL=8Ω	60	80	-	mW
		THD=0.2%, f=1KHz, RL=16Ω	40	50	-	mW
		THD=10%, f=1KHz, RL=8Ω	70	100	-	mW
		THD=10%, f=1KHz, RL=16Ω	55	70	-	mW
Output noise	VN		-	20	50	μV

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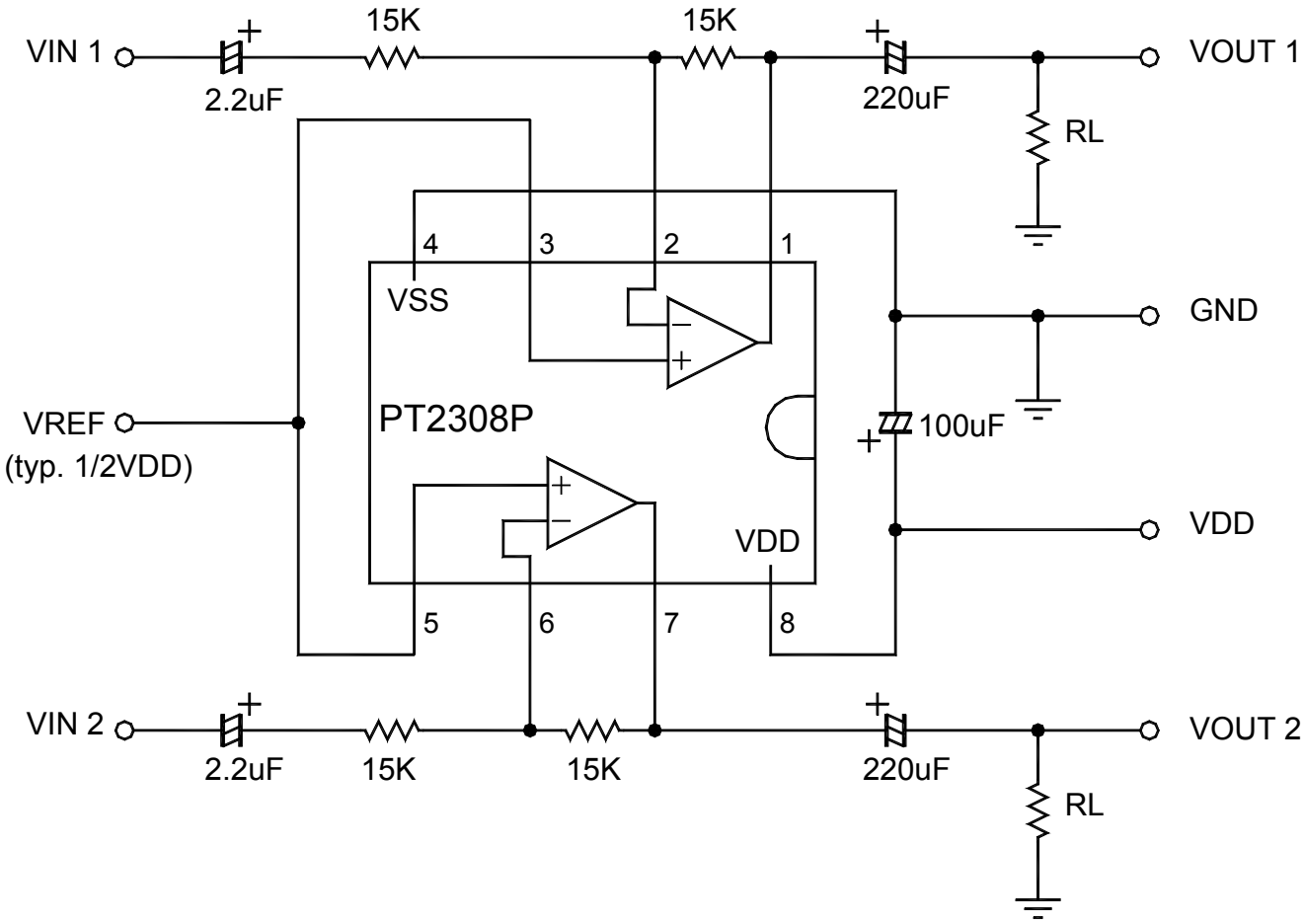
APPLICATION CIRCUIT



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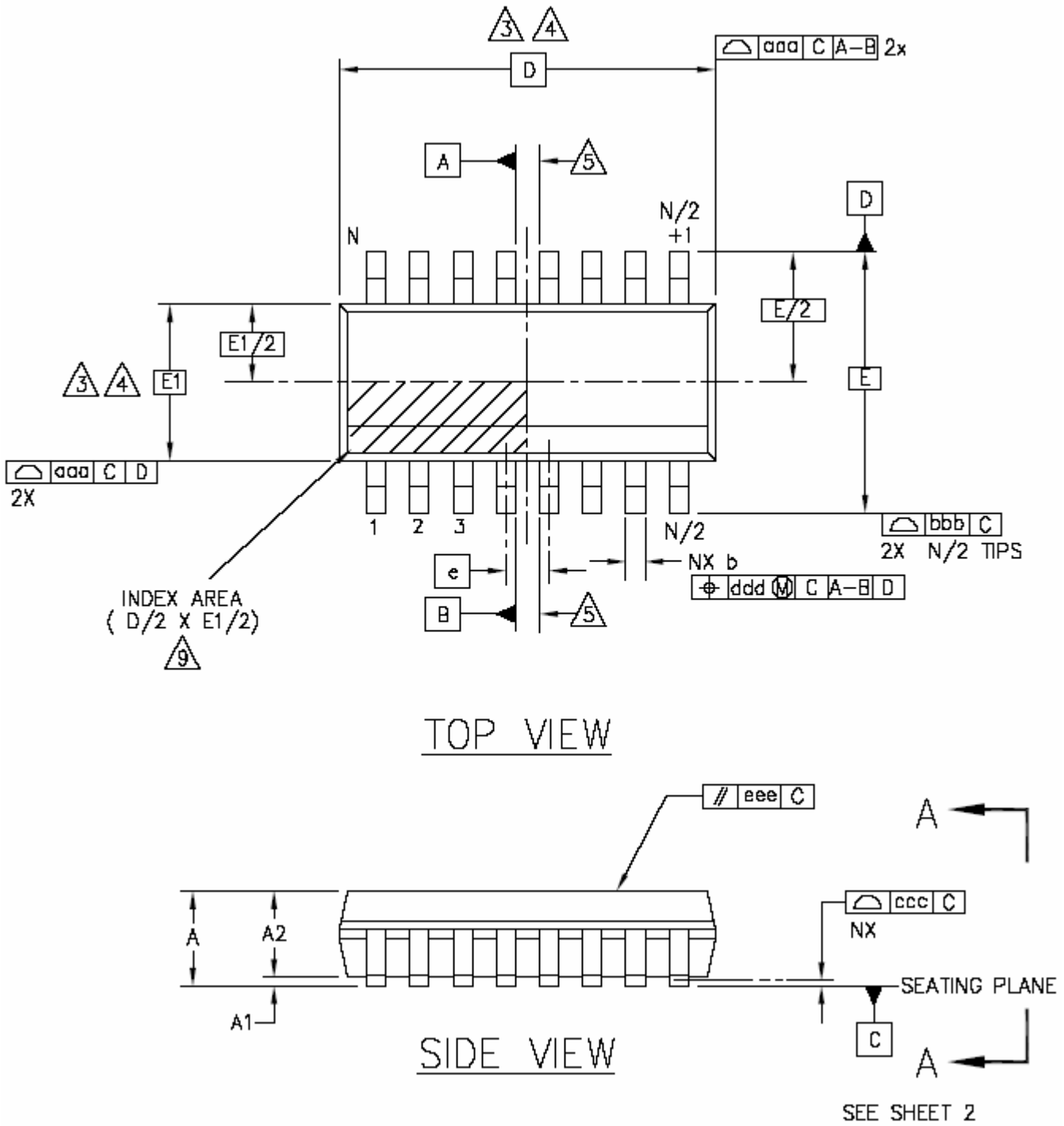
ORDER INFORMATION

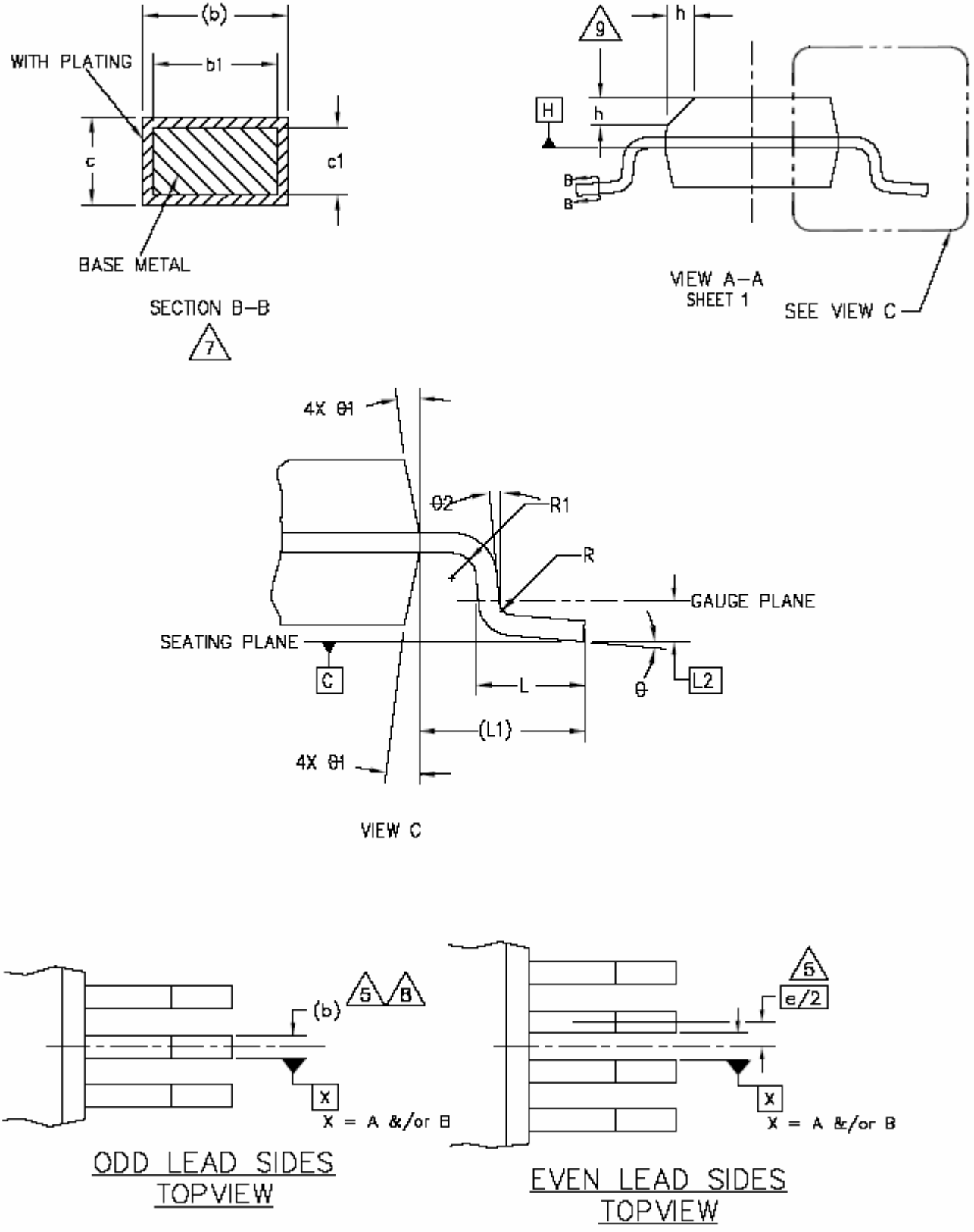
Valid Part Number	Package Type	Top Code
PT2308P-S	8 Pins, SOP, 150mil	PT2308P-S
PT2308P-S (L)	8 Pins, SOP, 150mil	PT2308P-S

Notes:
1. (L), (C) or (S) = Lead Free.
2. The Lead Free mark is put in front of the date code.

PACKAGE INFORMATION

8PINS, SOP, 150MIL




(b)
WITH PLATING
b1
c
c1
BASE METAL
SECTION B–B
7
g
h
H
h
B
B
VIEW A–A
SHEET 1
SEE VIEW C
4X θ1
θ2
R1
R
GAUGE PLANE
SEATING PLANE
C
L
θ
L2
(L1)
4X θ1
VIEW C
5
B
(b)
X
X = A &/or B
ODD LEAD SIDES
TOPVIEW
5
e/2
X
X = A &/or B
EVEN LEAD SIDES
TOPVIEW

Symbol	Min.	Typ.	Max.
A	1.35	-	1.75
A1	0.10	-	0.25
A2	1.25	-	1.65
b	0.31	-	0.51
b1	0.28	-	0.48
c	0.17	-	0.25
c1	0.17	-	0.23
D	4.90 BSC.		
E	6.00 BSC.		
E1	3.90 BSC.		
e	1.27 BSC.		
L	0.40	-	1.27
L1	1.04 REF.		
L2	0.25 BSC.		
R	0.07	-	-
R1	0.07		-
h	0.25	-	0.50
θ	0°	-	8°
θ1	5°	-	15°
θ2	0°	-	-

Notes:
1. Dimensioning and tolerancing per ANSI Y 14.5M-1994
2. Controlling Dimension: MILLIMETERS.
3. Dimension D does not include mold flash protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm (0.006 in) per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side. D and E1 dimensions are determined at datum H.
4. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
5. Datums A & B to be determined at datum H.
6. N is the number of terminal positions. (N=8)
7. The dimensions apply to the flat section of the lead between 0.10 to 0.25mm from the lead tip.
8. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of the “b” dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.
9. This chamfer feature is optional. If it is not present, then a pin 1 identifier must be located within the index area indicated.
10. Refer to JEDEC MS-012, Variation AA.
    JEDEC is the registered trademark of JEDEC SOLID STATE TECHNOLOGY ASSOCIATION.