



STP100NF04 STB100NF04

N-channel 40V - 0.0043Ω - 120A - TO-220 - D²PAK
STripFET™ II Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D	P _w
STP100NF04	40V	< 0.0046Ω	120A	300W
STB100NF04	40V	< 0.0046Ω	120A	300W

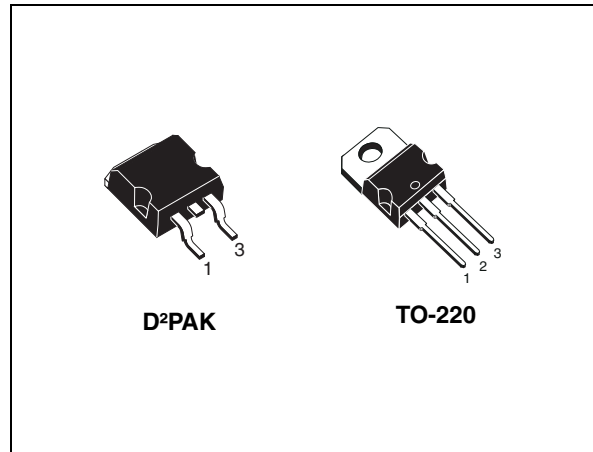
- Standard threshold drive
- 100% avalanche tested

Description

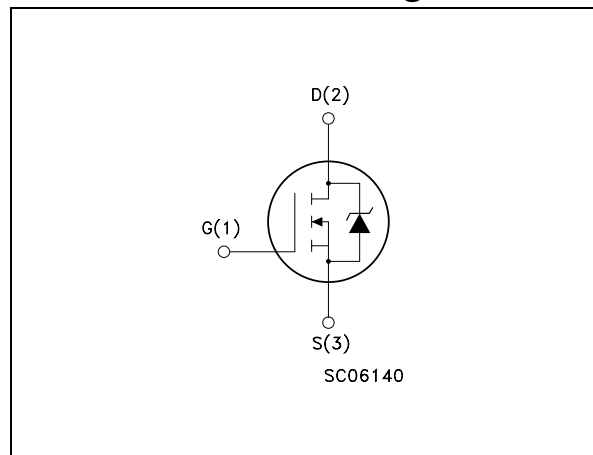
This Power MOSFET is the latest development of STMicroelectronics unique “Single Feature Size™” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Applications

- Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STB100NF04	B100NF04	D ² PAK	Tape & Reel
STP100NF04	P100NF04	TO-220	Tube

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage ($V_{GS}=0$)	40	V
V_{GS}	Gate-source Voltage	± 20	V
$I_D^{(1)}$	Drain-current (continuous) at $T_c=25^\circ\text{C}$	120	A
$I_D^{(1)}$	Drain-current (continuous) at $T_c=100^\circ\text{C}$	120	A
$I_{DM}^{(2)}$	Drain-current (pulsed)	480	A
P_{TOT}	Total dissipation at $T_c=25^\circ\text{C}$	300	W
	Derating factor	2	W/ $^\circ\text{C}$
$dv/dt^{(3)}$	Peak Diode Recovery voltage slope	6	V/ns
$E_{AS}^{(4)}$	Single Pulse Avalanche Energy	1.2	J
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 175	$^\circ\text{C}$

1. Current limited by package
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 120\text{A}$, $di/dt \leq 300\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{jmax}$
4. Starting $T_j=25^\circ\text{C}$, $I_D=60\text{A}$, $V_{DD}=30\text{V}$

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal Resistance Junction-case Max	0.5	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}$	Thermal Resistance Junction-pcb Max	(see Figure 13)	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal Resistance Junction-ambient (Free Air) Max	62.5	$^\circ\text{C}/\text{W}$
T_l	Maximum Lead Temperature For Soldering Purpose	300	$^\circ\text{C}$

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 3. On/off

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0$	40			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS}=0$)	$V_{DS}=\text{Max Rating}$ $V_{DS}=\text{Max Rating}$ $T_c=125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS}=0$)	$V_{GS}=\pm 20\text{V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS}=10\text{V}$, $I_D=50\text{A}$		0.0043	0.0046	Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
gfs	Forward Transconductance	$V_{DS}=15\text{V}$, $I_D=50\text{A}$		150		S
C_{iss}	Input Capacitance	$V_{DS}=25\text{V}$, $f=1\text{MHz}$, $V_{GS}=0$		5100		pF
C_{oss}	Output Capacitance			1300		pF
C_{rss}	Reverse Transfer Capacitance			160		pF
Q_g	Total Gate Charge	$V_{DD}=32\text{V}$, $I_D=120\text{A}$ $V_{GS}=10\text{V}$		110	150	nC
Q_{gs}	Gate-Source Charge			35		nC
Q_{gd}	Gate-Drain Charge			70		nC
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=20\text{V}$, $I_D=60\text{A}$ $R_G=4.7\Omega$, $V_{GS}=10\text{V}$ (see Figure 21)		35		ns
t_r	Rise time			220		ns
$t_{d(off)}$	Turn-off delay Time			80		ns
t_f	Fall Time			50		ns

Table 5. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				120	A
$I_{SDM}^{(1)}$	Source-drain Current (pulsed)				480	A
$V_{SD}^{(2)}$	Forward on Voltage	$I_{SD}=120A, V_{GS}=0$			1.3	V
t_{rr}	Reverse Recovery Time	$I_{SD}=120A, V_{DD}=20V,$ $di/dt=100A/\mu s, T_J=150^{\circ}C$		75		ns
Q_{rr}	Reverse Recovery Charge			185		nC
I_{RRM}	Reverse recovery Current			5		A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration=300 μ s, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Power Derating vs. Tc

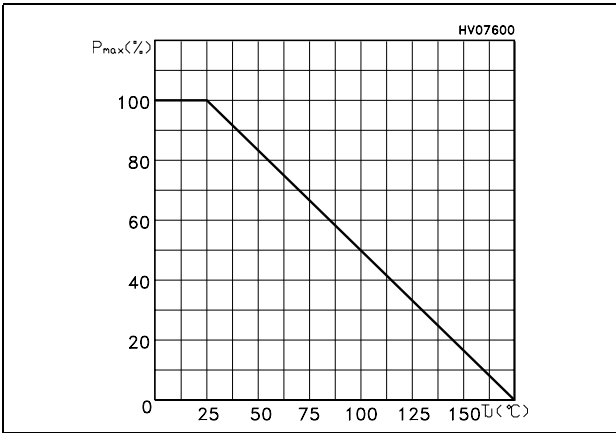


Figure 2. Max Id Current vs. Tc

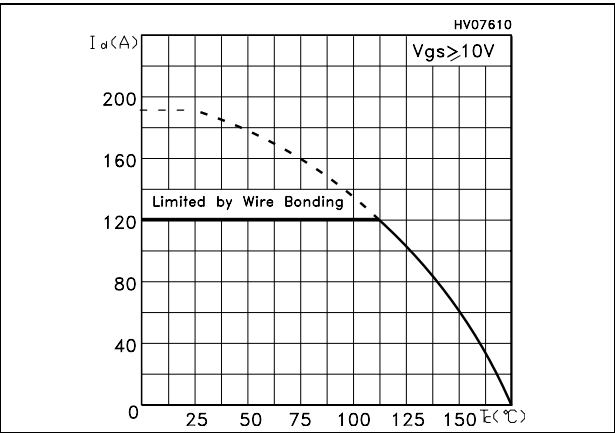


Figure 3. Output Characteristics

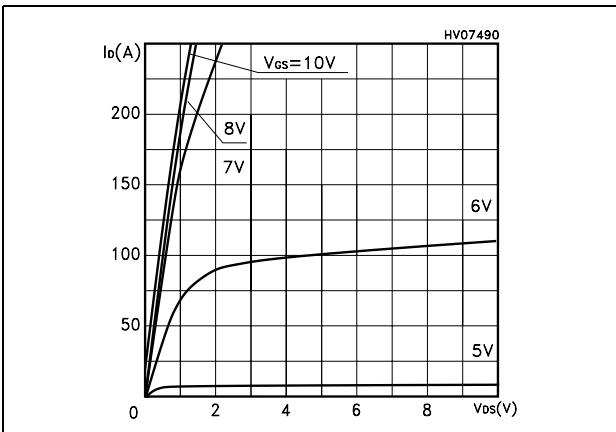


Figure 4. Transfer Characteristics

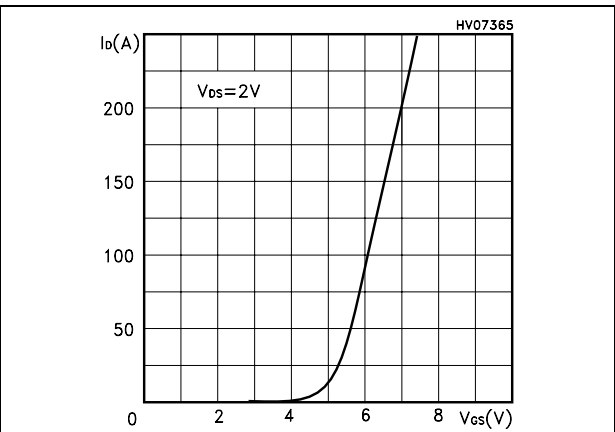


Figure 5. Transconductance

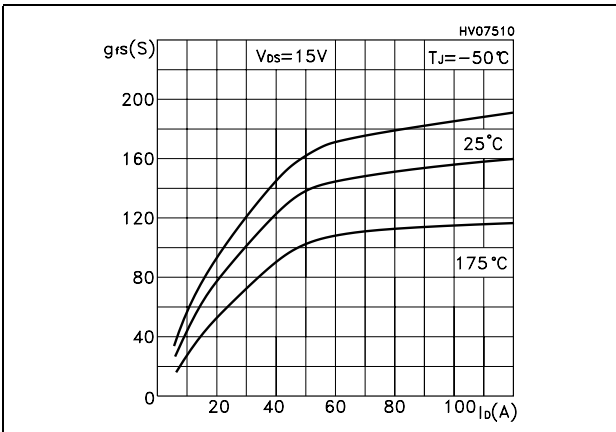


Figure 6. Static Drain-source on Resistance

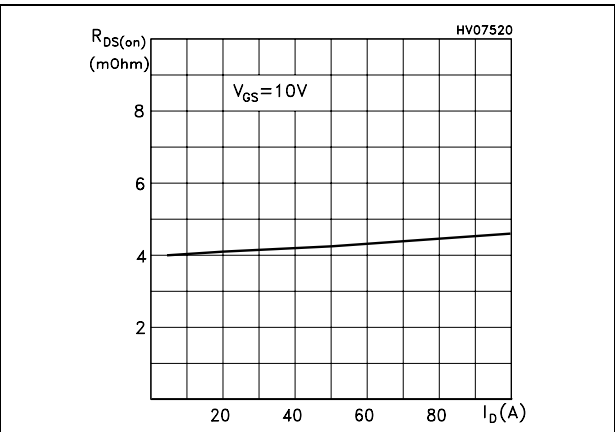


Figure 7. Gate Charge vs. Gate-source Voltage

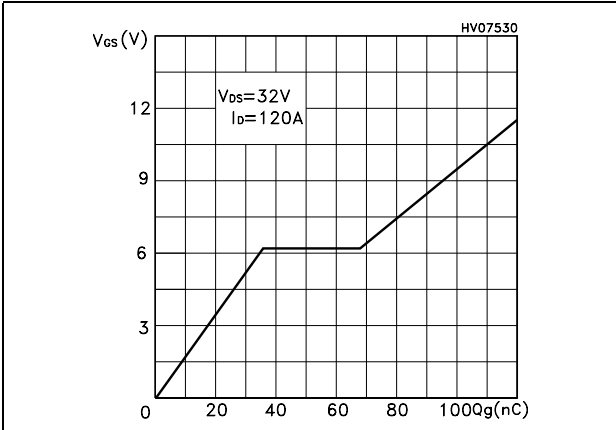


Figure 8. Capacitance Variations

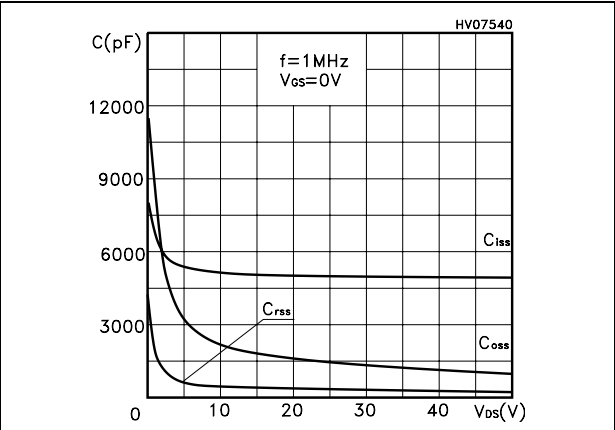


Figure 9. Normalized Gate Threshold Voltage vs. Temperature

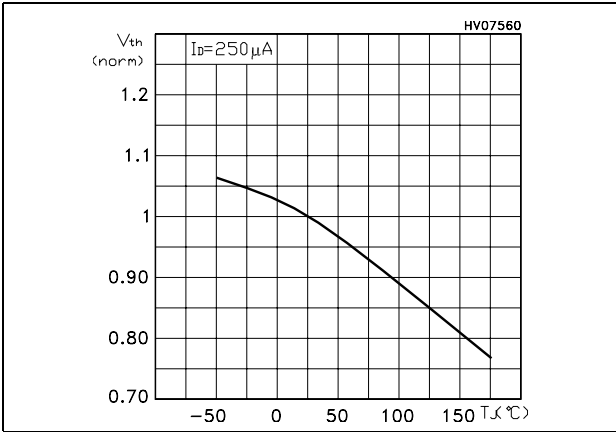


Figure 10. Normalized on Resistance vs. Temperature

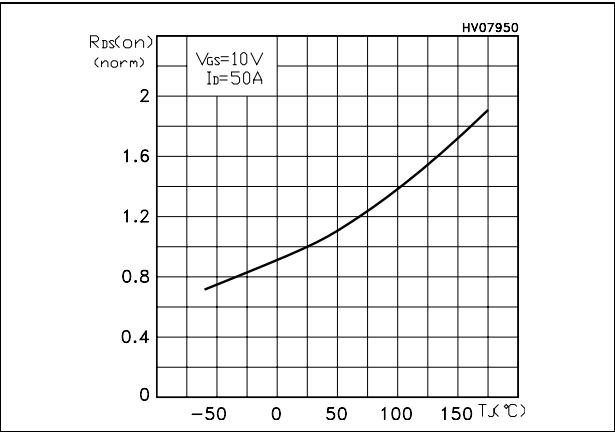


Figure 11. Source-Drain Diode Forward Characteristics

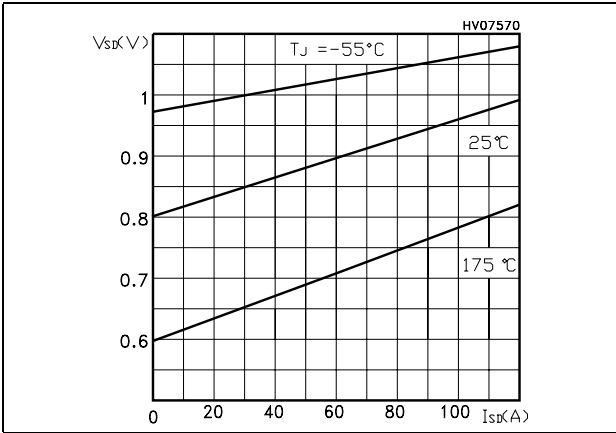


Figure 12. Normalized BVdss vs. Temperature

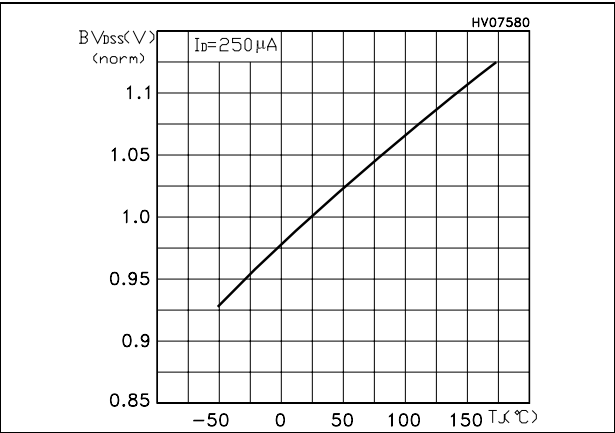


Figure 13. Thermal Resistance Rthj-pcb vs. PCB Copper Area

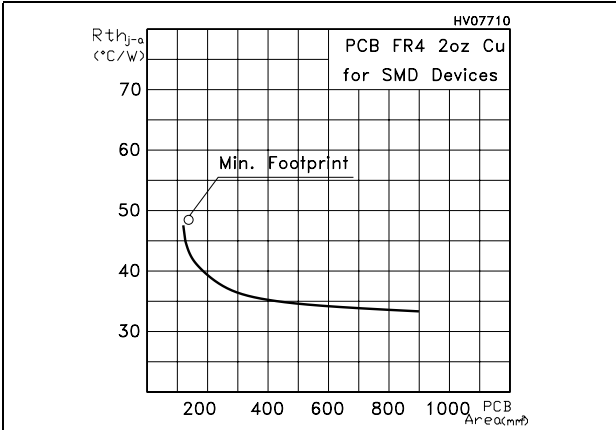


Figure 14. Thermal Impedance

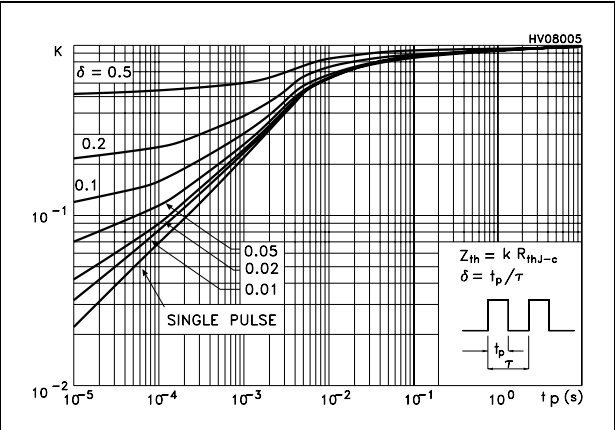


Figure 15. Max Power Dissipation vs. PCB Copper Area

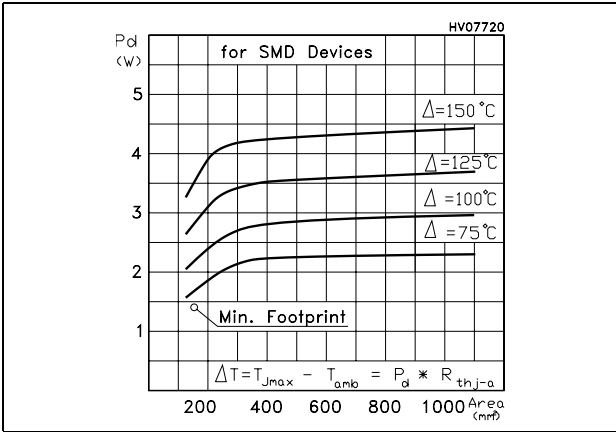


Figure 16. Safe Operating Area

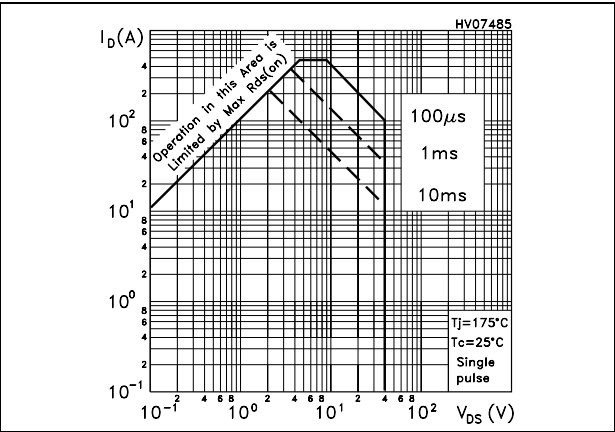
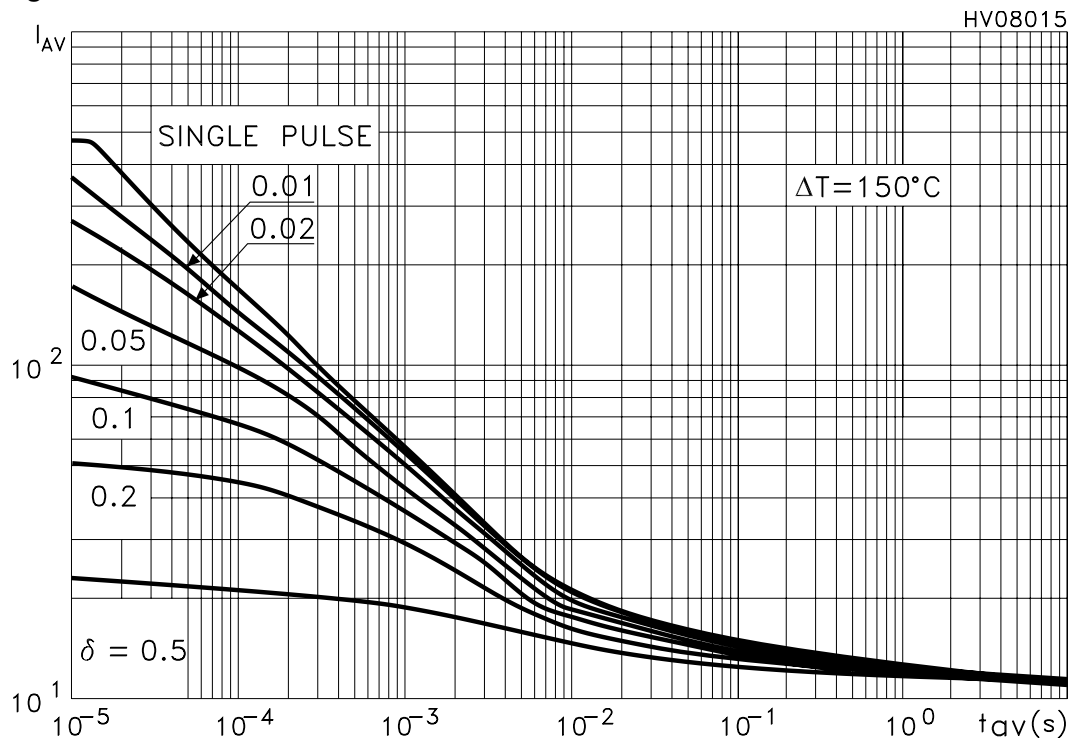


Figure 17. Allowable I_{AV} vs. Time in Avalanche

The previous curve give the safe operating area for unclamped inductive loads, single pulse or repetitive, under the following conditions:

$$P_{D(AVE)} = 0.5 \cdot (1.3 \cdot BV_{DSS} \cdot I_{AV})$$

$$E_{AS(AR)} = P_{D(AVE)} \cdot t_{AV}$$

Where:

I_{AV} is the Allowable Current in Avalanche

$P_{D(AVE)}$ is the Average Power Dissipation in Avalanche (Single Pulse)

t_{AV} is the Time in Avalanche

To de rate above 25°C, at fixed I_{AV} , the following equation must be applied:

$$I_{AV} = 2 \cdot (T_{jmax} - T_{CASE}) / (1.3 \cdot BV_{DSS} \cdot Z_{th})$$

Where:

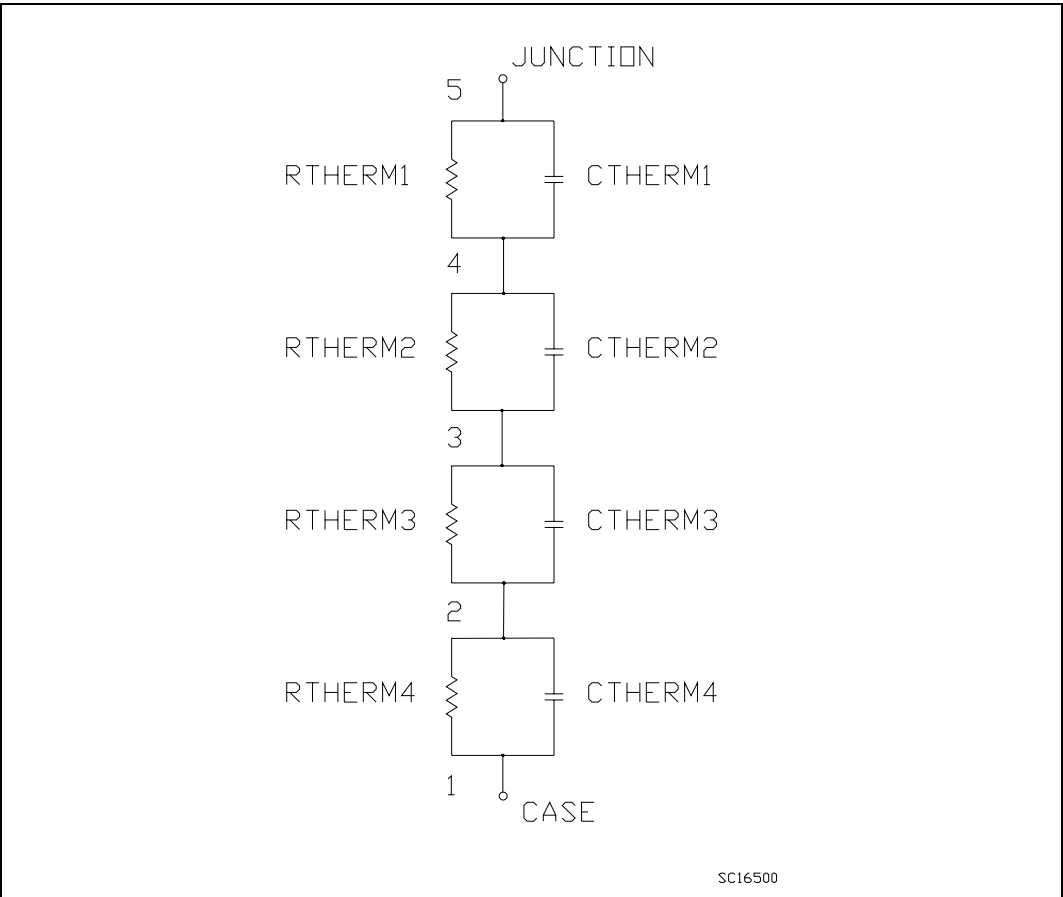
$Z_{th} = K \cdot R_{th}$ is the value coming from Normalized Thermal Response at fixed pulse width equal to T_{AV}

2.2 Spice thermal model

Table 6. Spice parameter

Parameter	Node	Value
CTHERM1	5 - 4	0.011
CTHERM1	4 - 3	0.0012
CTHERM3	3 - 2	0.05
CTHERM4	2 - 1	0.1
R THERM1	5 - 4	0.09
R THERM2	4 - 3	0.02
R THERM3	3 - 2	0.11
R THERM4	2 - 1	0.17

Figure 18. Spice model schematic



3 Test circuit

Figure 19. Unclamped inductive load test circuit

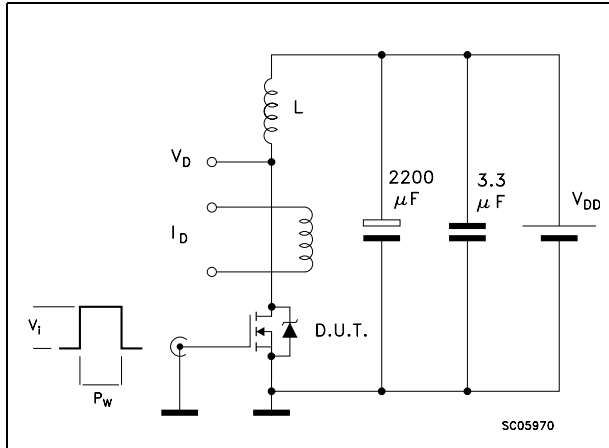


Figure 20. Unclamped inductive waveform

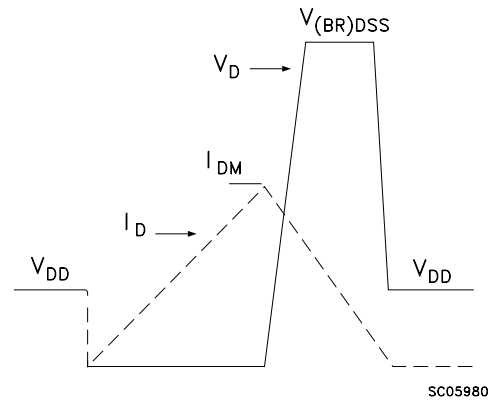


Figure 21. Switching times test circuit for resistive load

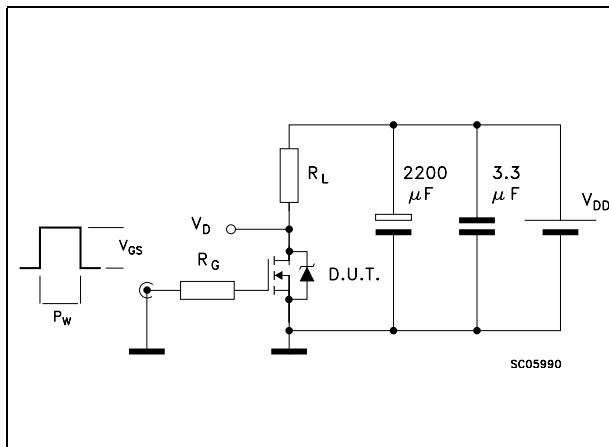


Figure 22. Gate charge test circuit

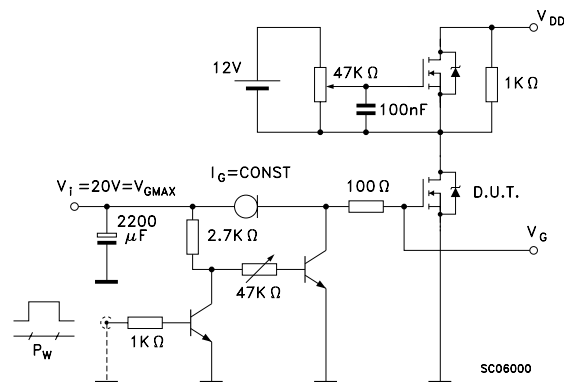


Figure 23. Test circuit for inductive load switching

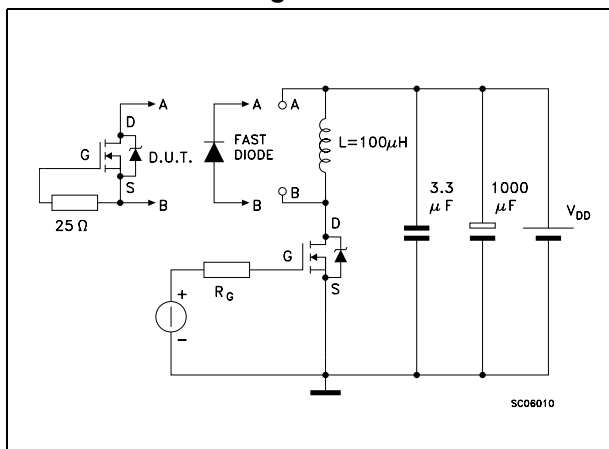
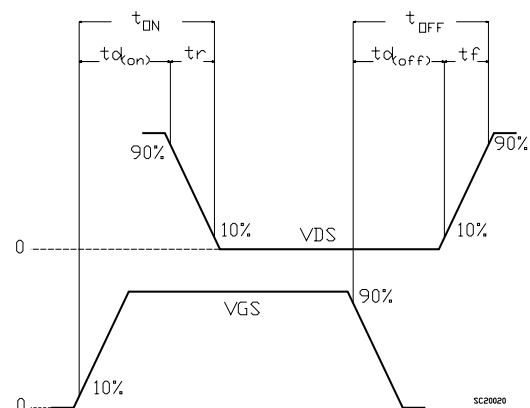


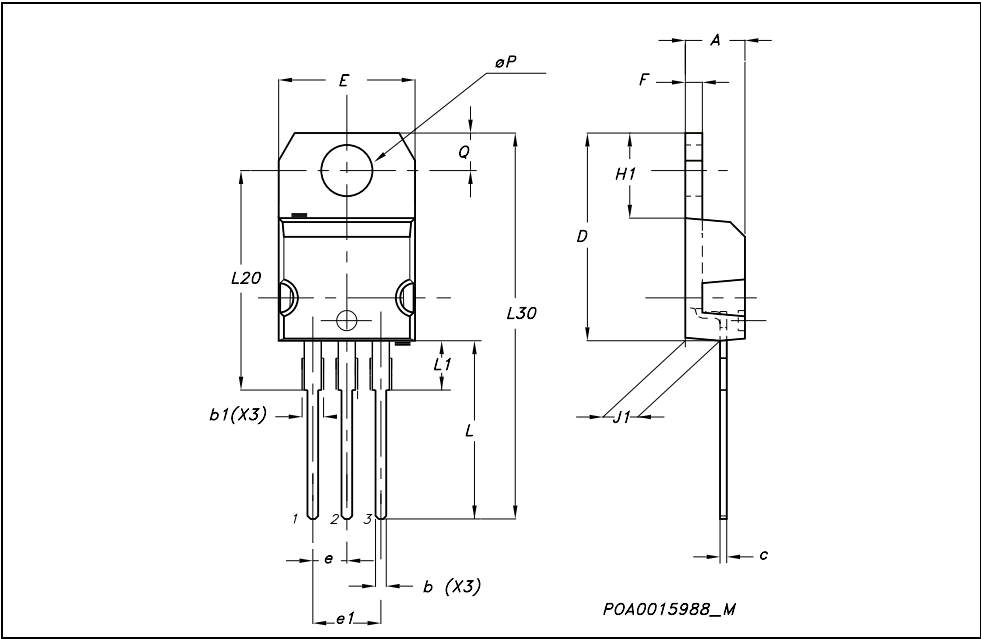
Figure 24. Switching time waveform



4 **Package mechanical data**

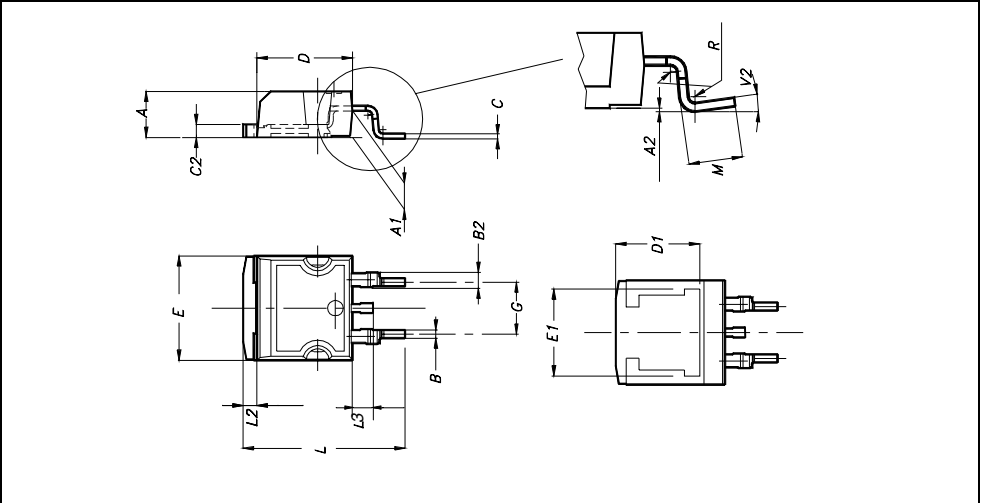
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-220 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			

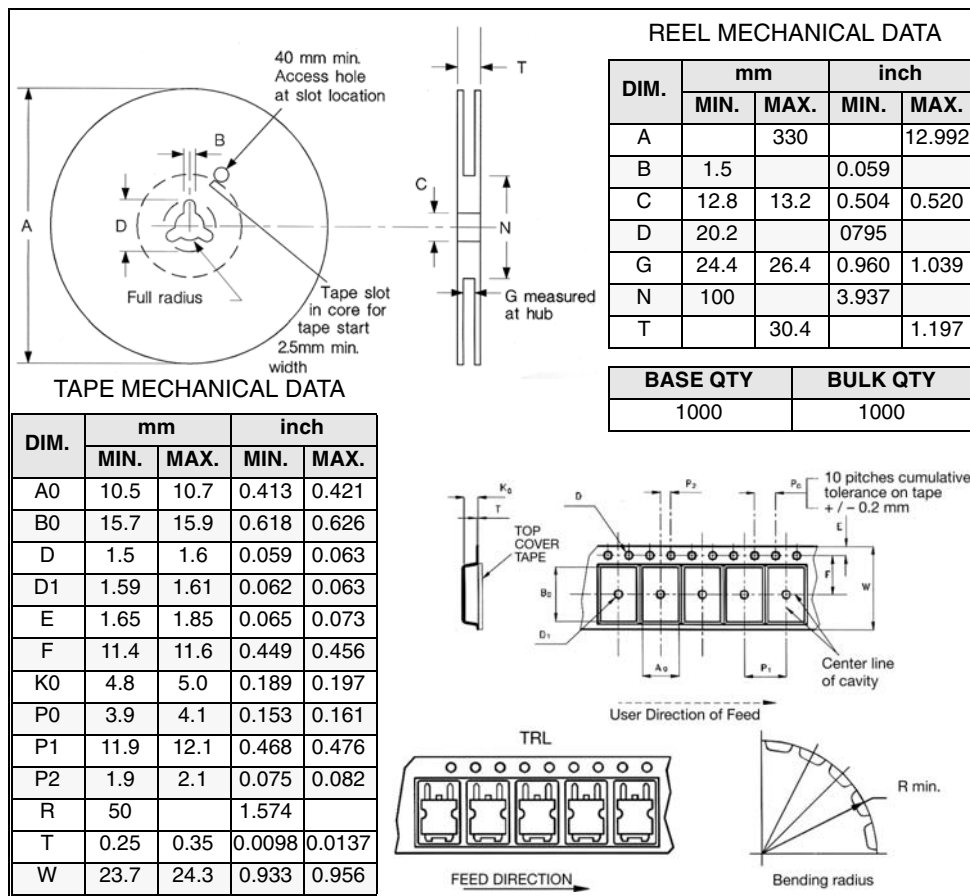


5 Packaging mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



* on sales type

6 Revision history

Table 7. Revision history

Date	Revision	Changes
23-Mar-2005	2	New template
01-Mar-2006	3	Removed I ² PAK and inserted D ² PAK.
04-Sep-2006	4	New template, no content change
20-Feb-2007	5	Typo mistake on page 1

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