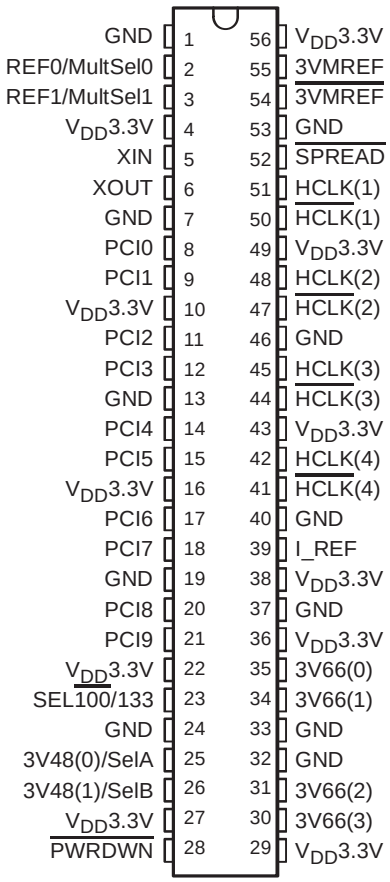
CDC930
133-MHz DIFFERENTIAL CLOCK SYNTHESIZER/DRIVER FOR PC MOTHERBOARDS WITH 3-STATE OUTPUTS

SCAS641 – JULY 2000

- **Generates Clocks for Pentium® 4 Microprocessors**
- **Uses a 14.318 MHz Crystal Input to Generate Multiple Output Frequencies**
- **Includes Spread Spectrum Clocking (SSC), 0.6% Downspread for Reduced EMI With Theoretical EMI Damping of 7 dB†**
- **Power Management Control Terminals**
- **Low Output Skew and Jitter for Clock Distribution**
- **Operates From Single 3.3-V Supply**
- **Consumes Less Than 30-mA Power-Down Current**
- **Generates the Following Clocks:**
  - **4 HCLK (Host) (Different Pairs– 100/133 MHz)**
  - **1 3VMREF Pair (3.3 V, 180° Shifted 50/66 MHz)**
  - **10 PCI (3.3 V, 33.3 MHz)**
  - **2 REF (3.3 V, 14.318 MHz)**
  - **4 3V66 MHz (3.3 V, 66 MHz)**
  - **2 3V48 MHz (3.3 V, 48 MHz)**
- **Packaged in 56-Pin SSOP Package**

DL PACKAGE
(TOP VIEW)



description

The CDC930 is a differential clock synthesizer/ driver that generates HCLK/HCLK, 3VMREF/ 3VMREF, PCI, 3V66, 3V48, REF system clock signals to support a computer system with a Pentium® 4 microprocessor and a Direct Rambus™ memory subsystem.

All output frequencies are generated from a 14.318-MHz crystal input. A reference clock input can be provided at the XIN input instead of a crystal. Two phase-locked loops (PLLs) are used to generate the host frequencies and the 48-MHz clock frequencies. On-chip loop filters and internal feedback eliminate the need for external components. The host, PCI clock and 48-MHz clock outputs provide low-skew/low-jitter clock signals for reliable clock operation. All outputs have 3-state capability, which can be selected using control inputs SEL133, SelA and SelB.

The outputs are either differential host clock or 3.3-V single-ended CMOS buffers. When PWRDWN is set to high, the device operates in normal mode. When PWRDWN is set low, the device transitions to a power-down mode in which HCLK is driven at $2\times I_{REF}$, HCLK is not driven, and all others are set low.

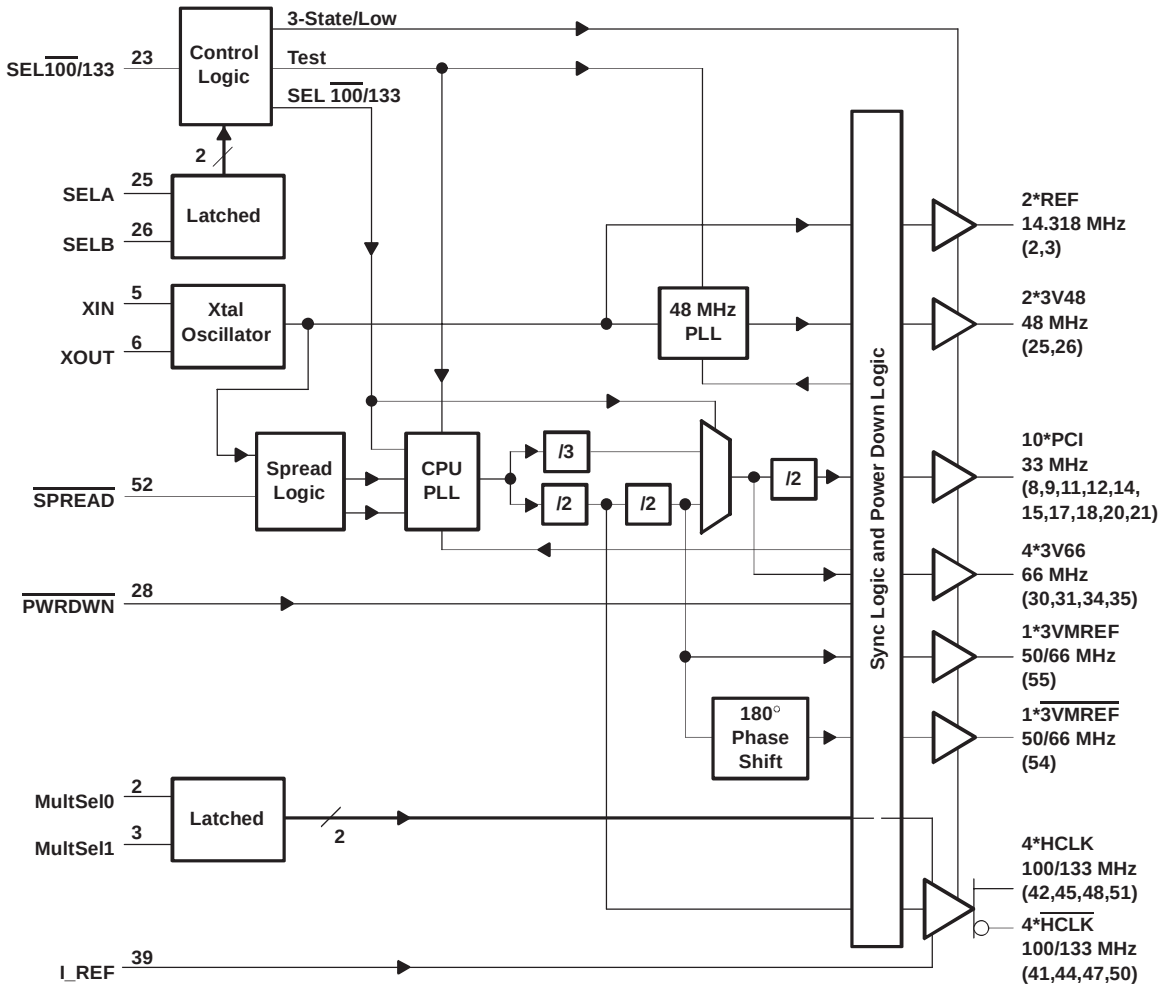
†This is system design dependant.
Intel and Pentium® 4 are trademarks of Intel Corporation.
Rambus is a trademark of Rambus Corporation.

description (continued)

The HOST bus operates at 100 MHz or 133 MHz. The MREF bus operates at 50 MHz or 66 MHz. Output frequency selection is accomplished with corresponding setting for SEL100/133 control input. The PCI bus frequency is fixed to 33 MHz.

Since the CDC930 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power up as well as changes to SEL inputs. With use of external reference clock, this signal must be fixed-frequency and fixed-phase prior stabilization time starts.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
3V48(0)/SelA	25	I/O	Dual function 3.3 V, Type 3, 48-MHz clock output that latches the state of SelA during power up
3V48(1)/SelB	26	I/O	Dual function 3.3 V, Type 3, 48-MHz clock output that latches the state of SelB during power up
3V66[0–3]	30, 31, 34, 35	O	3.3 V, Type 5, 66-MHz clock outputs
3VMREF	55	O	3.3 V, Type 5, 50/66-MHz memory clock output
$\overline{3VMREF}$	54	O	3.3 V, Type 5, 50/66-MHz memory clock output (180° out of phase with 3VMREF)
GND	1, 7, 13, 19, 24, 32, 33, 37, 40, 46, 53		Ground for core and HCLK/$\overline{HCLK}$, 3VMREF/$\overline{3VMREF}$, 3V48, 3V66 and PCI outputs
HCLK[1–4]	42, 45, 48, 51	O	Type X1, host clock outputs
$\overline{HCLK}$[1–4]	41, 44, 47, 50	O	Type X1, host complementary clock outputs
I_REF	39	Special	Current reference pin for the host clock pairs. I_REF uses a fixed precision resistor tied to ground to establish the appropriate current.
PCI[0–9]	8, 9, 11, 12, 14, 15, 17, 18, 20, 21	O	3.3 V, Type 5, 33-MHz PCI clock outputs
$\overline{PWRDWN}$	28	I	Power down for complete device with HOST at 2×I_{REF}, $\overline{HCLK}$ not driven and all other outputs forced low.
REF0/MultSel0	2	I/O	Dual function 3.3 V, Type 3, 14.318-MHz reference clock output. The state of MultSel0 is latched during power up. MultSel0 configures the I_{OH} amplitude (and thus the V_{OH} swing amplitude) of the HCLK pair outputs.
REF1/MultSel1	3	I/O	Dual function 3.3 V, Type 3, 14.318-MHz reference clock output. The state of MultSel1 is latched during power up. MultSel1 configures the I_{OH} amplitude (and thus the V_{OH} swing amplitude) of the HCLK pair outputs.
SEL$\overline{100}$/133	23	I	Active low LVTTL level logic select. SEL100/133 is used for enabling 100/133 MHz. Low=100 MHz, high=133 MHz
$\overline{SPREAD}$	52	I	LVTTL level logic select. $\overline{SPREAD}$ pin enables/disables the spread spectrum for the HCLK/$\overline{HCLK}$, 3VMREF/$\overline{3VMREF}$, 3V66 and PCI outputs.
V_{DD}3.3V	4, 10, 16, 22, 27, 29, 36, 38, 43, 49, 56	I	3.3-V power for core and the HCLK/$\overline{HCLK}$, 3VMREF/$\overline{3VMREF}$, 3V48, 3V66, and PCI outputs.
XIN	5	I	Crystal input – 14.318 MHz
XOUT	6	O	Crystal output – 14.318 MHz

Function Tables

SELECT FUNCTIONS

INPUTS			OUTPUTS						FUNCTION
SEL100/133	SelA	SelB	HOST, HCLK	3VMREF, 3VMREF	PCI	3V66	3V48	REF	
0	0	0	100 MHz	50 MHz	33 MHz	66 MHz	48 MHz	14.318 MHz	Active 100 MHz
0	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	All outputs 3-stated
1	0	0	133 MHz	66 MHz	33 MHz	66 MHz	48 MHz	14.318 MHz	Active 133 MHz
1	1	1	TCLK/2	TCLK/4	TCLK/8	TCLK/4	TCLK/2	TCLK	Test Mode

ENABLE FUNCTION

INPUT	OUTPUTS						
SEL100/133	HCLK	HCLK	3VMREF, 3VMREF	PCI	3V66	3V48	REF
0	$2\times I_{REF}$	Not driven	L	L	L	L	L
1	On	On	On	On	On	On	On

SPREAD SPECTRUM FUNCTION

INPUT		OUTPUTS
SPREAD	0	Spread spectrum clocking active, –0.6% at HCLK/HCLK, 3VMREF/3VMREF, 3V66, PCI
	1	Spread spectrum clocking nonactive

OUTPUT BUFFER SPECIFICATIONS

BUFFER NAME	V_{DD} RANGE (V)	IMPEDANCE (Ω)	BUFFER TYPE
3V48, REF	3.135 – 3.465	20–60	TYPE 3
PCI, 3V66	3.135 – 3.465	12–65	TYPE 5
3VMREF/3VMREF	3.135 – 3.465	12–55	TYPE 5
HCLK/HCLK			TYPE X1

OUTPUT BUFFER SPECIFICATIONS

INPUTS		BOARD TARGET TRACE/TERM Z	REFERENCE R, $I_{REF} = VDD/3\times R_r$)	OUTPUT CURRENT	V_{OH} AT Z IREF = 2.32 mA
MultSel0	MultSel1				
0	**0**	**60 Ω**	**R_r = 475 1%, I_{REF} = 2.32 mA**	**$I_{OH} = 5\times I_{REF}$**	**0.71 V at 60 Ω**
0	0	50 Ω	R_r = 475 1%, I_{REF} = 2.32 mA	$I_{OH} = 5\times I_{REF}$	0.59 V at 50 Ω
0	1	60 Ω	R_r = 475 1%, I_{REF} = 2.32 mA	$I_{OH} = 6\times I_{REF}$	0.85 V at 60 Ω
0	**1**	**50 Ω**	**R_r = 475 1%, I_{REF} = 2.32 mA**	**$I_{OH} = 6\times I_{REF}$**	**0.71 V at 50 Ω**
1	0	60 Ω	R_r = 475 1%, I_{REF} = 2.32 mA	$I_{OH} = 4\times I_{REF}$	0.56 V at 60 Ω
1	0	50 Ω	R_r = 475 1%, I_{REF} = 2.32 mA	$I_{OH} = 4\times I_{REF}$	0.47 V at 50 Ω
1	1	60 Ω	R_r = 475 1%, I_{REF} = 2.32 mA	$I_{OH} = 7\times I_{REF}$	0.99 V at 60 Ω
1	1	50 Ω	R_r = 475 1%, I_{REF} = 2.32 mA	$I_{OH} = 7\times I_{REF}$	0.82 V at 50 Ω

NOTE: The entries in **boldface** are the primary system configurations of interest. The outputs should be optimized for these configurations

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{DD} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{DD} + 0.5 V
Voltage range applied to any output in the high-impedance state or power-off state,
V_O (see Note 1) . . . . . –0.5 V to V_{DD} + 0.5 V
Current into any output in the low state, I_O . . . . . 2 × rated I_{OL}
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
(V_I < V_{DD}) . . . . . 18 mA
Output clamp current , I_{OK} (V_O < 0) . . . . . –50 mA
(V_O < V_{DD}) . . . . . 50 mA
Package thermal impedance, θ_{JA} (see Note 2) . . . . . 74°C/W
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3) . . . . . 1.3 W
Operating free-air temperature range, T_A . . . . . 0°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for the through-hole packages, which use a trace length of zero. The absolute maximum power dissipation allowed at T_A = 55°C (in still air) is 1.3 W.
3. The maximum package power dissipation is calculated using a junction temperature of 1505C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DL	1558.6 mW	12.468 mW/°C	997.5 mW	810.52 mW

‡ This is the inverse of the traditional junction-to-case thermal resistance ($R_{\theta JA}$) and uses a board-mounted device at 74°C/W.

recommended operating conditions (see Note 2)

		MIN	NOM†	MAX	UNIT
Supply voltage, V_{DD}		3.135		3.465	V
High-level input voltage, V_{IH}		2		V_{DD} + 0.3 V	V
Low-level input voltage, V_{IL}		GND – 0.3 V		0.8	V
Input voltage, V_I		0		V_{DD}	V
High-level output current, I_{OH}	HCLK/$\overline{\text{HCLK}}$			–20	mA
	3VMREF/$\overline{\text{3VMREF}}$			–15	
	48MHz, REFx			–16	
	PCIx, 3V66x			–15	
Low-level output current, I_{OL}	HCLK/$\overline{\text{HCLK}}$			5	µA
	3VMREF/$\overline{\text{3VMREF}}$			10	mA
	48MHz, REFx			10	
	PCIx, 3V66x			10	
Reference frequency, $f_{(XIN)}$‡	Test mode		14		MHz
Crystal frequency, $f_{(XTAL)}$§	Normal mode	13.8	14.318	14.8	MHz
Operating free-air temperature, T_A		0		85	°C

† All nominal values are measured at their respective nominal V_{DD} values.
‡ Reference frequency is a test clock driven on the XIN input during the device test mode and normal mode. In test mode, XIN can be driven externally up to $f_{(XIN)}$ = 16 MHz. If XIN is driven externally, XOUT is floating.
§ This is a series fundamental crystal with f_O = 14.31818 MHz.
NOTES: 4. Unused inputs must be held high or low to prevent them from floating.
5. V_{IH}, V_{IL}: All input levels referenced to V_{DD} = 3.30 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		V_{DD} = 3.135 V,	I_I = –18 mA			–1.2	V
R_I	Input resistance	XIN-XOUT	V_{DD} = 3.465 V,	$V_I = V_{DD}$ –0.5 V		100		kΩ
I_{IH}	High-level input current	XOUT	V_{DD} = 3.135 V,	$V_I = V_{DD}$ –0.5 V			50	mA
		MultSel0, MultSel1, SelA, SelB	V_{DD} = 3.465 V,	$V_I = V_{DD}$			10	µA
		$\overline{SEL100}$/133 $\overline{SPREAD}$, PWRDWN	V_{DD} = 3.465 V,	$V_I = V_{DD}$			5	µA
I_{IL}	Low-level input current	XOUT	V_{DD} = 3.135 V,	V_O = 0 V			–5	mA
		MultSel0, MultSel1, SelA, SelB,	V_{DD} = 3.465 V,	V_I = GND			–10	µA
		$\overline{SEL100}$/133 $\overline{SPREAD}$, $\overline{PWRDWN}$	V_{DD} = 3.465 V,	V_I = GND			–5	µA
		I_REF	V_{DD} = 3.465 V,	R_r = 221			–5.5	mA
I_{OZ}	High-impedance-state output current		V_{DD} = 3.465 V	SELA, $\overline{SELB}$ = H, $\overline{SEL100}$/133 H → L, $V_O = V_{DD}$ or GND, $\overline{PWRDWN}$ = H			±10	µA
$I_{DD(Z)}$	High-impedance-state supply current		V_{DD} = 3.465 V	SELA, $\overline{SELB}$ = H, $\overline{SEL100}$/133 H → L, $\overline{PWRDWN}$ = H			40	mA
$I_{DD(PD)}$	$\overline{PWRDWN}$ state supply current		V_{DD} = 3.465 V,	$\overline{PWRDWN}$ = L			30	mA
I_{DD}	Dynamic supply current		V_{DD} = 3.465 V	$\overline{PWRDWN}$ = H, HCLK = 133 MHz, SSC = ON/OFF, C_L = MAX, R_{ref} = 475 Ω, $I_{OUT} = 6 \times I_{ref}$			250	mA
C_I	Input capacitance‡		V_{DD} = 3.3 V,	$V_I = V_{DD}$ or GND	2		5	pF
$C_{(XTAL)}$	Crystal terminal capacitance		V_{DD} = 3.3 V,	V_I = 0.3 V		18		pF

† All typical values are measured at their respective nominal V_{DD} values.
‡ These parameters are ensured by design and lab characterization, not 100% production tested.
Control SELx, $\overline{PWRDWN}$, $\overline{SPREAD}$ threshold levels during FUNC w/c level tests.
C_L = MAX = 5 pF, R_S = 33.2 Ω, R_p = 49.9 Ω at HCLK/$\overline{HCLK}$ (Type X1)
C_L = MAX = 20 pF, R_L = 500 Ω at 48 MHz, REF (Type 3) $\overline{\text{REF}}$
C_L = MAX = 30 pF, R_L = 500 Ω at PCIx, 3V66, 3VMREF, $\overline{3VMREF}$ (Type 5)

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

HCLK/$\overline{\text{HCLK}}$ (Type X1)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
I_{OH}	High-level output current	I_{ref} = 2.32 mA × 4	V_{DD} = 3.135 V	V_{OH} at Z = 50 Ω	–8.1			mA
			V_{DD} = 3.465 V				–10.5	
		I_{ref} = 2.32 mA × 5	V_{DD} = 3.135 V		–10.1			mA
			V_{DD} = 3.465 V				–13.1	
		I_{ref} = 2.32 mA × 6	V_{DD} = 3.135 V		–12.1			mA
			V_{DD} = 3.465 V				–15.7	
		I_{ref} = 2.32 mA × 7	V_{DD} = 3.135 V		–14.1			mA
			V_{DD} = 3.465 V				–18.4	
C_O	Output capacitance‡	V_O = V_{DD} or GND				3.5		pF

† All typical values are measured at their respective nominal V_{DD} values.
‡ These parameters are ensured by design and lab characterization, not 100% production tested.

48MHz, REFx (Type 3), C_L = 20 pF, R_L = 500 Ω

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{DD} = min to max,	I_{OH} = –1 mA	VDD – 0.1 V			V
		V_{DD} = 3.135 V,	I_{OH} = –14 mA	2.4			
V_{OL}	Low-level output voltage	V_{DD} = min to max,	I_{OL} = 1 mA			0.1	V
		V_{DD} = 3.135 V,	I_{OL} = 9 mA			0.4	
I_{OH}	High-level output current	V_{DD} = 3.135 V,	V_O = 1 V	–29			mA
		V_{DD} = 3.3 V,	V_O = 1.65 V		–41		
		V_{DD} = 3.465 V,	V_O = 3.135 V			–23	
I_{OL}	Low-level output current	V_{DD} = 3.135 V,	V_O = 1.95 V	29			mA
		V_{DD} = 3.3 V,	V_O = 1.65 V		53		
		V_{DD} = 3.465 V,	V_O = 0.4 V			27	
C_O	Output capacitance‡	V_{DD} = 3.3 V,	V_O = V_{DD} or GND	2		5	pF

† All typical values are measured at their respective nominal V_{DD} values.
‡ These parameters are ensured by design and lab characterization, not 100% production tested.

PCIx, 3V66x, MREF/$\overline{\text{MREF}}$ (Type 5), C_L = 20 pF, R_L = 500 Ω

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{DD} = min to max,	I_{OH} = –1 mA	VDD – 0.1 V			V
		V_{DD} = 3.135 V,	I_{OH} = –18 mA	2.4			
V_{OL}	Low-level output voltage	V_{DD} = min to max,	I_{OL} = 1 mA			0.1	V
		V_{DD} = 3.135 V,	I_{OL} = 12 mA			0.4	
I_{OH}	High-level output current	V_{DD} = 3.135 V,	V_O = 1 V	–33			mA
		V_{DD} = 3.3 V,	V_O = 1.65 V		–53		
		V_{DD} = 3.465 V,	V_O = 3.135 V			–33	
I_{OL}	Low-level output current	V_{DD} = 3.135 V,	V_O = 1.95 V	30			mA
		V_{DD} = 3.3 V,	V_O = 1.65 V		70		
		V_{DD} = 3.465 V,	V_O = 0.4 V			38	
C_O	Output capacitance‡	V_{DD} = 3.3 V,	V_O = V_{DD} or GND	2		5	pF

† All typical values are measured at their respective nominal V_{DD} values.
‡ These parameters are ensured by design and lab characterization, not 100% production tested.

switching characteristics, V_{DD} = MIN to MAX, T_A = 0°C to 85°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
v_{over}	Overshoot‡			HCLK/HCLK 0.7 V amplitude			V_{OH}+200	mV
v_{under}	Undershoot‡						V_{OL}–200	
v_{over}	Overshoot‡			Other clocks, C_L = Worst case	GND–0.7			V
v_{under}	Undershoot‡						V_{DD}+0.7	
t_{PZL}	Output enable time to low level	SEL100/133	HCLK/HCLK	$f_{(HCL)}$ = 100 or 133 MHz, SELA, SELB = H, SEL100/133 L → H, R_{ref} = 475 Ω			100	ns
t_{PZH}	Output enable time to high level						100	ns
t_{PHZ}	Output disable time from high level			$f_{(HCL)}$ = 100 or 133 MHz, SELA, SELB = H, SEL100/133 H → L, R_{ref} = 475 Ω			10	ns
t_{PLZ}	Output disable time from low level						10	ns
t_{PZL}	Output enable time to low level	SEL100/133	REF, 3V48 3VMREF, 3VMREF, 3V66, PCI	$f_{(HCL)}$ = 100 or 133 MHz, SELA, SELB = H, SEL100/133 L → H, R_{ref} = 475 Ω			10	ns
t_{PZH}	Output enable time to high level						10	ns
t_{PHZ}	Output disable time from high level			$f_{(HCL)}$ = 100 or 133 MHz, SELA, SELB = H, SEL100/133 H → L, R_{ref} = 475 Ω			10	ns
t_{PLZ}	Output disable time from low level						10	ns
t_{stab}	Stabilization time†			After power up			3	ms

† Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. In order for phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present a XIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics tables are not applicable. Stabilization time is defined as the time from when V_{DD} achieves its nominal operating level until the output frequency is stable and operating within specification.

‡ These parameters are ensured by design and lab characterization, not 100% production tested.

HCLK/HCLK (Type X1) C_L = 2 pF, R_L > 500 kΩ

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_c	HCLK clock period†			$f_{(HCLK)}$ = 100 MHz	10		10.2	ns
				$f_{(HCLK)}$ = 133 MHz	7.5		7.65	
$t_{jit(cc)}$	Cycle to cycle jitter			$f_{(HCLK}$ = 100 or 133 MHz			200	ps
t_{dc}	Duty cycle			$f_{(HCLK)}$ = 100 or 133 MHz crossing point	45%		55%	
$t_{sk(o)}$	HCLK bus skew	HCLKx	HCLKx	$f_{(HCLK)}$ = 100 or 133 MHz crossing point			150	ps
t_w	Pulse duration width			$f_{(HCLK}$ = 100 MHz	4.41			ns
				$f_{(HCLK}$ = 133 MHz	3.29			
t_r	Rise time‡	0.7 V amplitude		V_O = 0.14 V to 0.56 V	175		700	ps
t_f	Fall time‡			V_O = 0.14 V to 0.56 V	175		700	ps
t_r, t_f	Rise and fall time matching‡			2 × (t_r – t_f)/(t_r + t_f)			20%	
v_{cross}	Cross point voltages‡	0.7 V amplitude		$f_{(HCLK)}$ = 100 or 133 MHz HCLK and HCLK	40% VOH		55% VOH	V

† The average over any 1–μs period of time is greater than the minimum specified period.

‡ These parameters are ensured by design and lab characterization, not 100% production tested.

switching characteristics, V_{DD} = 3.135 V to 3.465 V, T_A = 0°C to 85°C (continued)

3VMREF/$\overline{3VMREF}$ (Type 5) C_L = 30 pF, R_L = 500 Ω

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_c	3VMREF/3VMREF clock period†			$f_{(3VMREF/\overline{3VMREF})}$ = 50 MHz	20		20.4	ns
				$f_{(3VMREF/\overline{3VMREF})}$ = 66 MHz	15		15.3	ns
$t_{jit(cc)}$	Cycle to cycle jitter			$f_{(3VMREF/\overline{3VMREF})}$ = 66 MHz, $f_{(HCLK)}$ = 100 or 133 MHz, V_{DD} = 3.3 V, Measured at 1.5 V			250	ps
t_{dc}	Duty cycle			$f_{(3VMREF/\overline{3VMREF})}$ = 66 MHz	45%		55%	
$t_{sk(o)}$	3VMREF/$\overline{3VMREF}$ output skew	3VMREF/ $\overline{3VMREF}$	3VMREF/ $\overline{3VMREF}$	$f_{(3VMREF/\overline{3VMREF})}$ = 66 MHz, $f_{(HCLK)}$ = 100 or 133 MHz, V_{DD} = 3.3 V, Measured at 1.5 V			250	ps
$t_{(off)}$	3VMREF/$\overline{3VMREF}$ clock to PCI offset	3VMREF/ $\overline{3VMREF}$	PCIx	$f_{(3VMREF/\overline{3VMREF})}$ = 66 MHz, Measured points at 1.5 V, Measured at rising edges			3	ns
t_r	Rise time			V_O = 0.4 V to 2.4 V	0.5		2	ns
t_f	Fall time			V_O = 0.4 V to 2.4 V	0.5		2	ns

† The average over any 1–μs period of time is greater than the minimum specified period.

3V66 (Type 5, No SSC), C_L = 30 pF, R_L = 500 Ω

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_c	3V66 clock period†			$f_{(3V66)}$= 66 MHz		15.03		ns
$t_{jit(cc)}$	Cycle to cycle jitter			$f_{(3V66)}$ = 66 MHz, $f_{(HCLK)}$ = 100 or 133 MHz, V_{DD} = 3.3 V, Measured at 1.5 V			300	ps
t_{dc}	Duty cycle			$f_{(3V66)}$ = 66 MHz	45%		55%	
$t_{sk(o)}$	3V66 output skew	3V66x	3V66x	$f_{(3V66)}$ = 66 MHz, $f_{(HCLK)}$ = 100 or 133 MHz, V_{DD} = 3.3 V, Measured at 1.5 V			250	ps
$t_{(off)}$	3V66 clock to PCI	3V66x	PCIx	$f_{(3V66)}$ = 66 MHz, Measured points at 1.5 V, Measured at rising edges	1.5		3.5	ns
t_r	Rise time			V_O = 0.4 V to 2.4 V	0.5		2	ns
t_f	Fall time			V_O = 0.4 V to 2.4 V	0.5		2	ns

† The average over any 1–μs period of time is greater than the minimum specified period.

PCI (Type 5), C_L = 30 pF, R_L = 500 Ω

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_c	PCI clock period†			$f_{(PCI)}$= 33.3 MHz		30.06		ns
$t_{jit(cc)}$	Cycle to cycle jitter			$f_{(HCLK)}$ = 100 or 133 MHz			500	ps
t_{dc}	Duty cycle			$f_{(PCI)}$ = 33.3 MHz	45%		55%	
$t_{sk(o)}$	PCI output skew	PCIx	PCIx	$f_{(PCI)}$ = 33.3 MHz			500	ps
t_r	Rise time			V_O = 0.4 V to 2.4 V	0.5		2	ns
t_f	Fall time			V_O = 0.4 V to 2.4 V	0.5		2	ns

† The average over any 1–μs period of time is greater than the minimum specified period.

switching characteristics, V_{DD} = 3.135 V to 3.465 V, T_A = 0°C to 85°C (continued)

3V48 (Type 3), C_L = 20 pF, R_L = 500 Ω

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_c	3V48 clock period†			$f_{(3V48)}$= 48 MHz		15.03		ns
$t_{jit(cc)}$	Cycle to cycle jitter			$f_{(3V48)}$ = 48 MHz, $f_{(HCLK)}$ = 100 or 133 MHz, V_{DD} = 3.3 V, Measured at 1.5 V			350	ps
t_{dc}	Duty cycle			$f_{(3V48)}$ = 48 MHz	45%		55%	
$t_{sk(o)}$	3V48 output skew	3V48x	3V48x	$f_{(3V48)}$ = 48 MHz, $f_{(HCLK)}$ = 100 or 133 MHz, V_{DD} = 3.3 V, Measured at 1.5 V			250	ps
$t_{(off)}$	3V48 clock to PCI	3V48x	PCIx	$f_{(3V48)}$ = 48 MHz, Measured points at 1.5 V, Measured at rising edges	1.5		3.5	ns
t_r	Rise time			V_O = 0.4 V to 2.4 V	1		4	ns
t_f	Fall time			V_O = 0.4 V to 2.4 V	1		4	ns

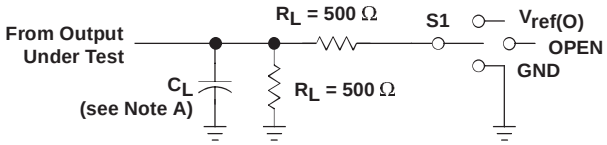
† The average over any 1–µs period of time is greater than the minimum specified period.

REF (Type 3), C_L = 20 pF, R_L = 500 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_c	REF clock period†	$f_{(REF)}$= 14.318 MHz		69.84		ns
$t_{jit(cc)}$	Cycle to cycle jitter	$f_{(HCLK)}$ = 100 or 133 MHz			1	ps
t_{dc}	Duty cycle	$f_{(REF)}$ = 14.318 MHz	52%		62%	
t_r	Rise time	V_O = 0.4 V to 2.4 V	1		4	ns
t_f	Fall time	V_O = 0.4 V to 2.4 V	1		4	ns

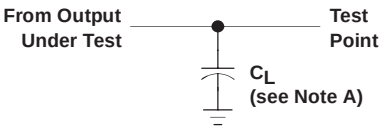
† The average over any 1–µs period of time is greater than the minimum specified period.

PARAMETER MEASUREMENT INFORMATION

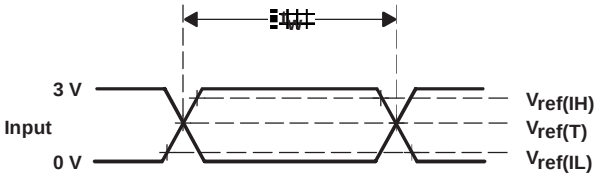


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$V_{ref(OFF)}$
t_{PHZ}/t_{PZH}	GND

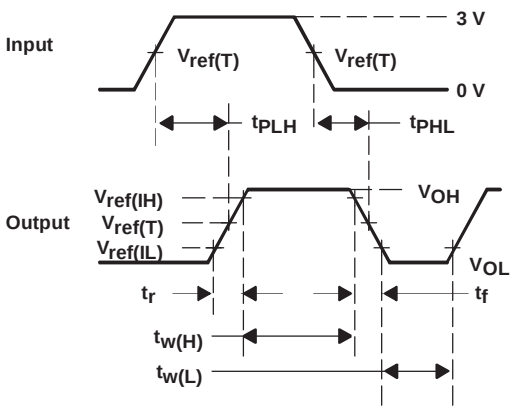
LOAD CIRCUIT of single-ended outputs for t_{pd} and t_{sk}



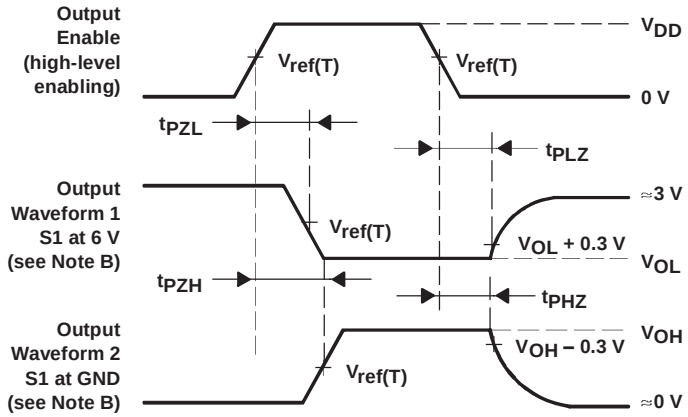
LOAD CIRCUIT of single-ended outputs for t_r and t_f



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



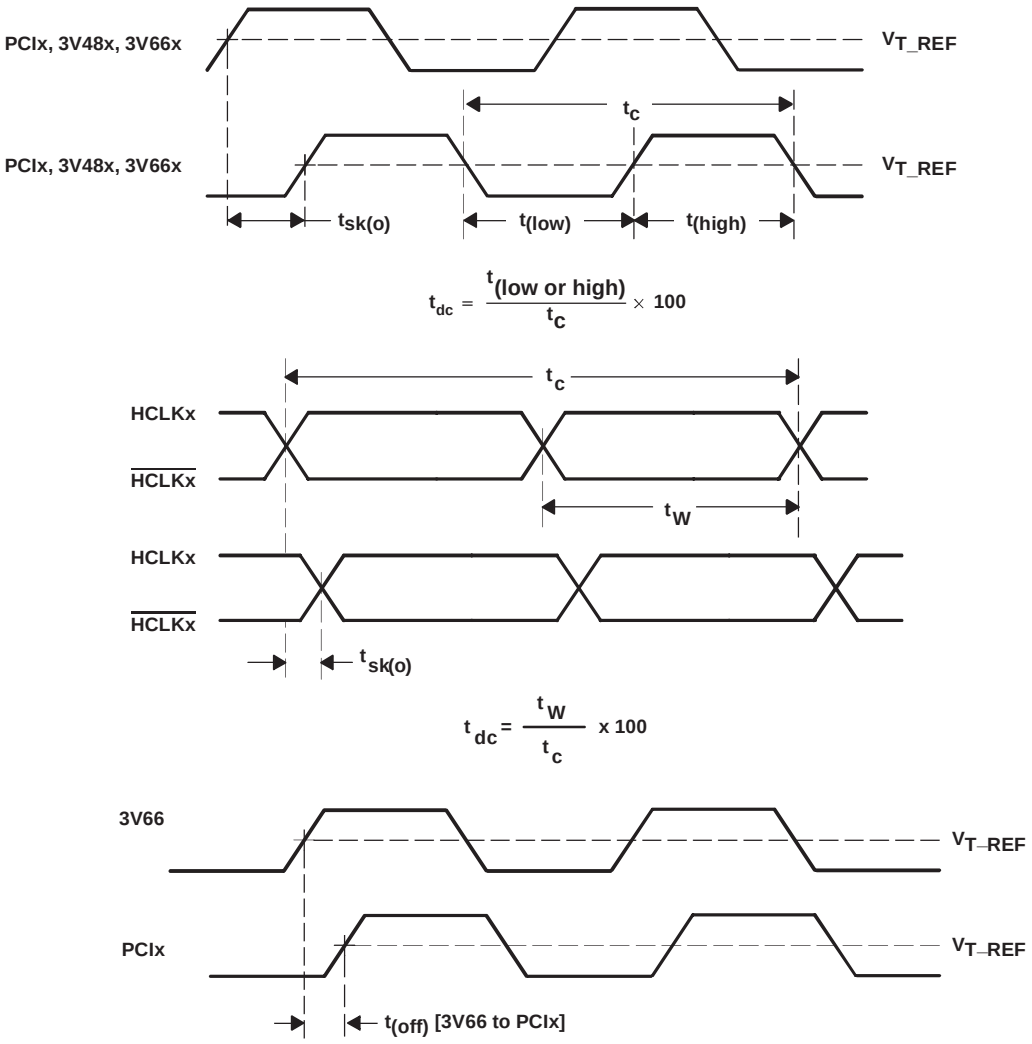
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance. C_L = 2 pF (HCLK, $\overline{HCLK}$), C_L = 20 pF (48MHZ, REF), C_L = 30 pF (PCIx, 3VMREF, 3V66).
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 14.318 MHz, Z_O = 50 Ω, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

PARAMETER		3.3-V INTERFACE	2.5-V INTERFACE	UNIT
$V_{ref(IH)}$	High-level reference voltage	2.4	2	V
$V_{ref(IL)}$	Low-level reference voltage	0.4	0.4	V
$V_{ref(T)}$	Input threshold reference voltage	1.5	1.25	V
$V_{ref(OFF)}$	Off-state reference voltage	6	4.6	V

Figure 1. Load Circuit and Voltage Waveforms

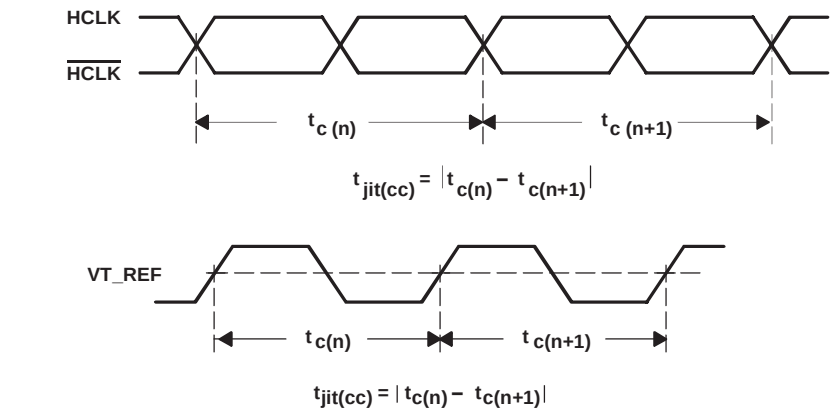
PARAMETER MEASUREMENT INFORMATION



PARAMETER		3.3-V INTERFACE	UNIT
V_{T_REF}	Input threshold reference voltage	1.5	V

Figure 2. Waveforms for Calculation of Output Skew, Duty Cycle, and Offset

PARAMETER MEASUREMENT INFORMATION



PARAMETER		3.3-V INTERFACE	UNIT
V_{T_REF}	Input threshold reference voltage	1.5	V

Figure 3. Waveforms for Calculation of Cycle-Cycle Jitter

PARAMETER MEASUREMENT INFORMATION

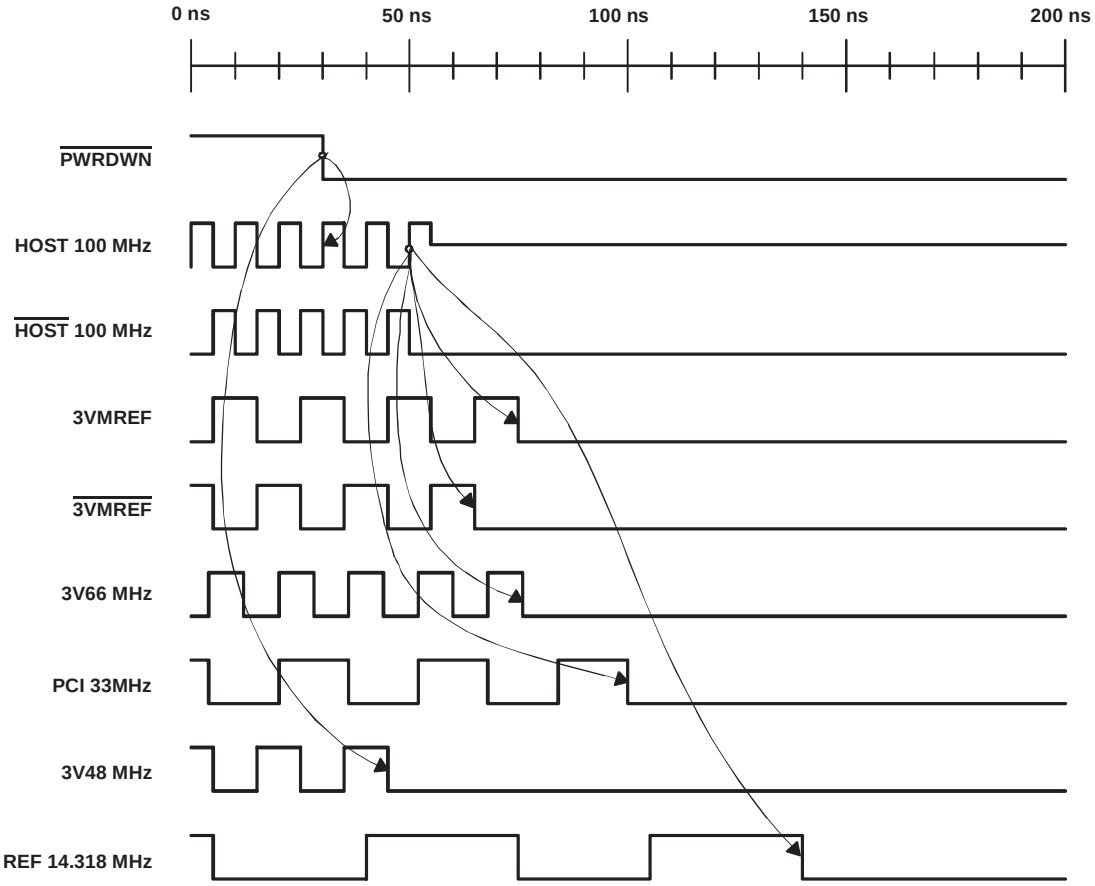
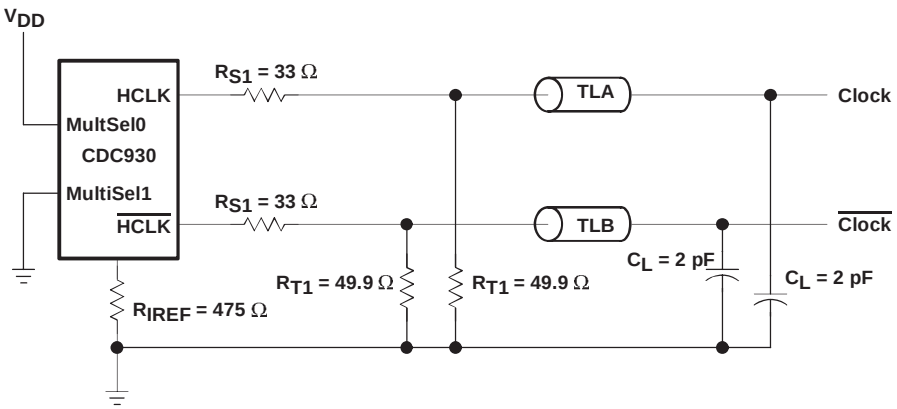


Figure 4. Power DOWN Timing



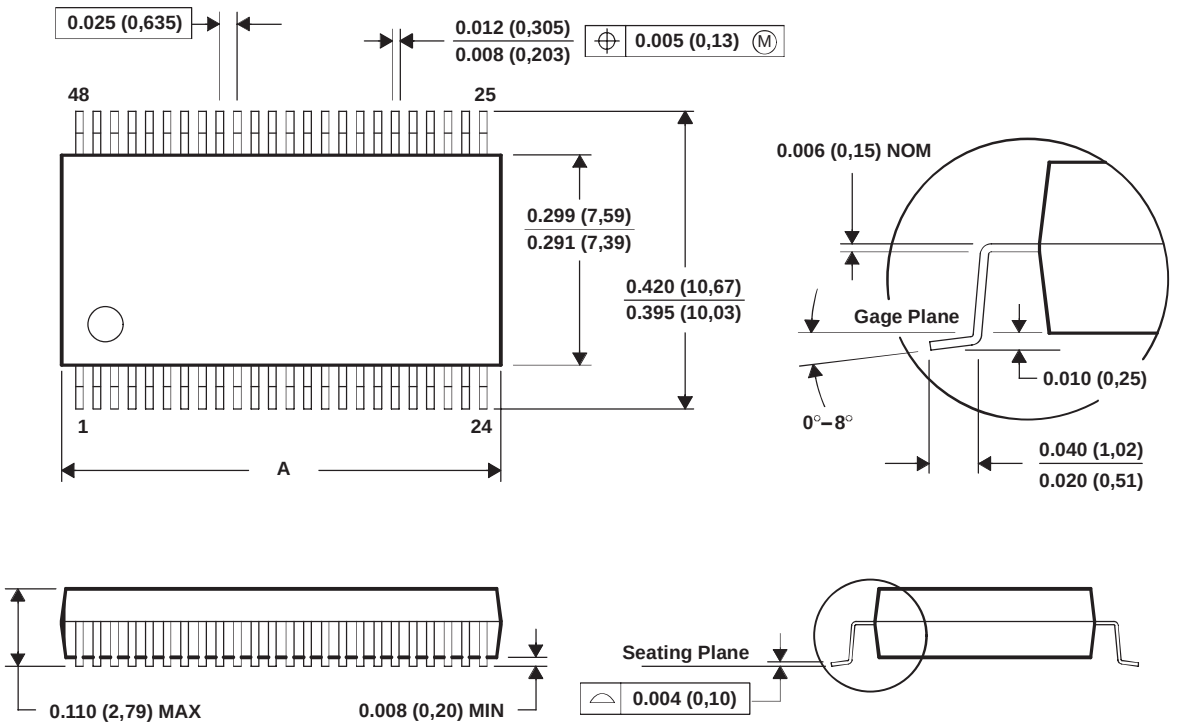
NOTE A: $Z_{(TLA)} = Z_{(TLB)} = 50\ \Omega$, $L_{(TLA)} = L_{(TLB)} = 3.5$", C_L represents probe and jig capacitance.

Figure 5. Load Circuit for 0.7 V Amplitude HCLK/HCLK Bus

MECHANICAL DATA

DL (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48-PIN SHOWN



DIM \ PINS **	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048/D 08/97

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.