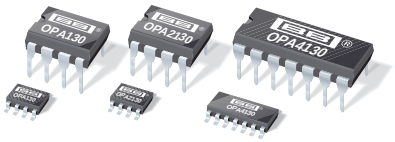
Burr-Brown Products
from Texas Instruments



OPA130
OPA2130
OPA4130

SBOS053A – MAY 1998 – REVISED MARCH 2006

Low Power, Precision FET-INPUT OPERATIONAL AMPLIFIERS

FEATURES

- **LOW QUIESCENT CURRENT: 530μA/amp**
- **LOW OFFSET VOLTAGE: 1mV max**
- **HIGH OPEN-LOOP GAIN: 120dB min**
- **HIGH CMRR: 90dB min**
- **FET INPUT: I_B = 20pA max**
- **EXCELLENT BANDWIDTH: 1MHz**
- **WIDE SUPPLY RANGE: ±2.25 to ±18V**
- **SINGLE, DUAL, AND QUAD VERSIONS**

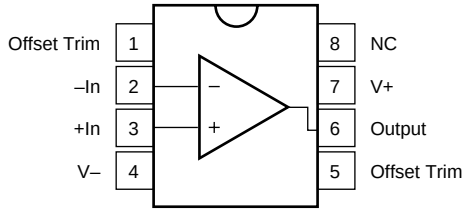
DESCRIPTION

The OPA130 series of FET-input op amps combine precision dc performance with low quiescent current. Single, dual, and quad versions have identical specifications for maximum design flexibility. They are ideal for general-purpose, portable, and battery operated applications, especially with high source impedance.

OPA130 op amps are easy to use and free from phase inversion and overload problems often found in common FET-input op amps. Input cascode circuitry provides excellent common-mode rejection and maintains low input bias current over its wide input voltage range. OPA130 series op amps are stable in unity gain and provide excellent dynamic behavior over a wide range of load conditions, including high load capacitance. Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

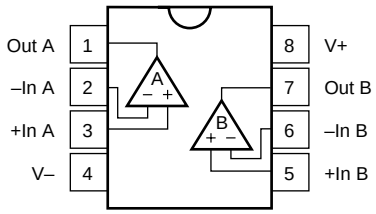
Single and dual versions are available in DIP-8 and SO-8 surface-mount packages. Quad is available in DIP-14 and SO-14 surface-mount packages. All are specified for –40°C to +85°C operation.

OPA130



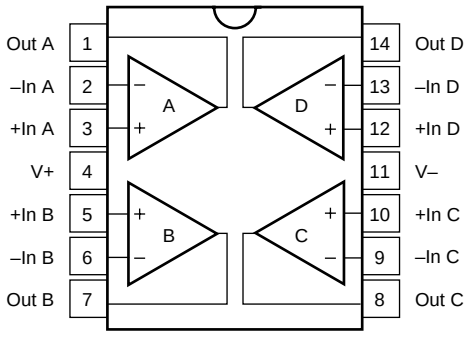
DIP-8, SO-8

OPA2130



DIP-8, SO-8

OPA4130



DIP-14, SO-14

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage, V+ to V–	36V
Input Voltage	(V–) –0.7V to (V+) +0.7V
Output Short-Circuit[2]	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	150°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Short-circuit to ground, one amplifier per package.

PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_S = ±15V, and R_L = 10kΩ, unless otherwise noted.

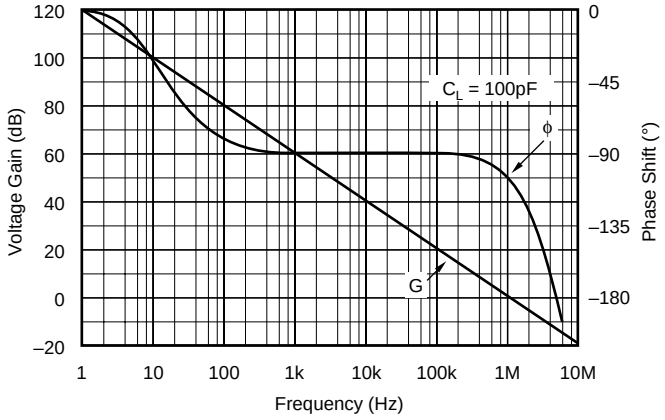
PARAMETER	CONDITION	OPA130PA, UA OPA2130PA, UA OPA4130PA, UA MIN	TYP	MAX	UNITS
OFFSET VOLTAGE					
Input Offset Voltage			±0.2	±1	mV
vs Temperature[1]	Operating Temperature Range		±2	±10	µV/°C
vs Power Supply	V_S = ±2.25V to ±18V		2	20	µV/V
Channel Separation (dual and quad)			0.3		µV/V
INPUT BIAS CURRENT[2]					
Input Bias Current	V_{CM} = 0V		+5	±20	pA
vs Temperature			See Typical Characteristics		
Input Offset Current	V_{CM} = 0V		±2	±20	pA
NOISE					
Input Voltage Noise					
Noise Density, f = 10Hz			30		nV/√Hz
f = 100Hz			18		nV/√Hz
f = 1kHz			16		nV/√Hz
f = 10kHz			16		nV/√Hz
Current Noise Density, f = 1kHz			4		fA/√Hz
INPUT VOLTAGE RANGE					
Common-Mode Voltage Range, Positive		(V+)–2	(V+)–1.5		V
Negative		(V–)+2	(V–)+1.2		V
Common-Mode Rejection	V_{CM} = –13V to +13V	90	105		dB
INPUT IMPEDANCE					
Differential			10^{13} || 1		Ω || pF
Common-Mode	V_{CM} = –13V to +13V		10^{13} || 3		Ω || pF
OPEN-LOOP GAIN					
Open-loop Voltage Gain	V_O = –13.8V to +13V	120	135		dB
	R_L = 2kΩ, V_O = –13V to +12V	120	135		dB
FREQUENCY RESPONSE					
Gain-Bandwidth Product			1		MHz
Slew Rate			2		V/µs
Settling Time: 0.1%	G = 1, 10V Step, C_L = 100pF		5.5		µs
0.01%	G = 1, 10V Step, C_L = 100pF		7		µs
Overload Recovery Time	G = 1, V_{IN} = ±15V		2		µs
Total Harmonic Distortion + Noise	1kHz, G = 1, V_O = 3.5Vrms		0.0003		%
OUTPUT					
Voltage Output, Positive		(V+)–2	(V+)–1.5		V
Negative		(V–)+1.2	(V–)+1		V
Positive	R_L = 2kΩ	(V+)–3	(V+)–2.5		V
Negative	R_L = 2kΩ	(V–)+2	(V–)+1.5		V
Short-Circuit Current			±18		mA
Capacitive Load Drive (Stable Operation)			10		nF
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±2.25		±18	V
Quiescent Current (per amplifier)	I_O = 0		±530	±650	µA
TEMPERATURE RANGE					
Operating Range		–40		+85	°C
Storage		–40		+125	°C
Thermal Resistance, θ_{JA}					
DIP-8			100		°C/W
SO-8 Surface-Mount			150		°C/W
DIP-14			80		°C/W
SO-14 Surface-Mount			110		°C/W

NOTES: (1) Ensured by wafer test. (2) High-speed test at T_J = 25°C.

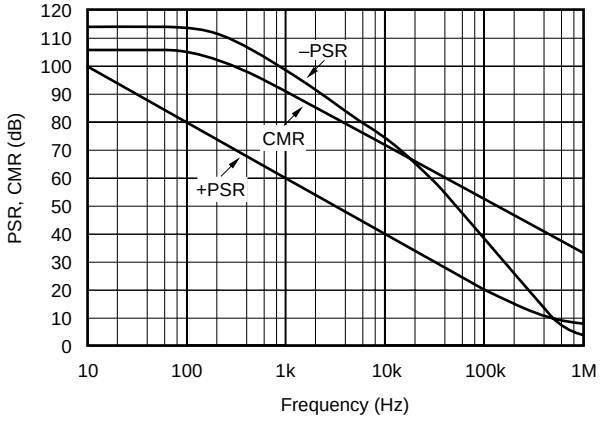
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = ±15V, and R_L = 10kΩ, unless otherwise noted.

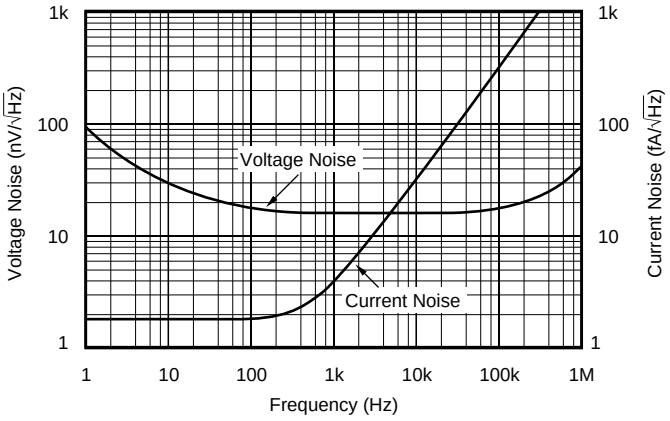
OPEN-LOOP GAIN/PHASE vs FREQUENCY



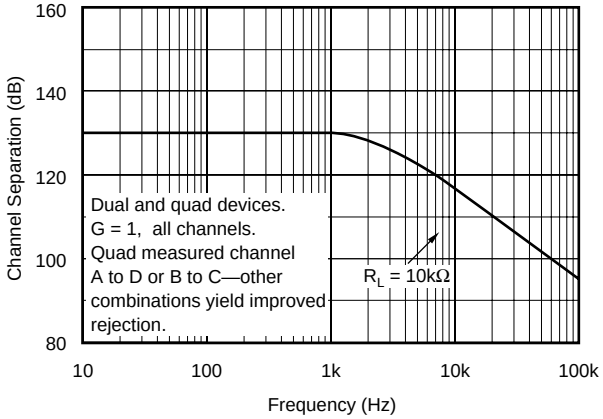
POWER SUPPLY AND COMMON-MODE REJECTION vs FREQUENCY



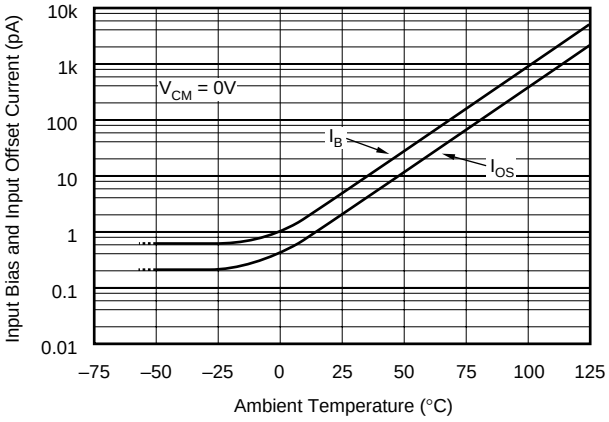
INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



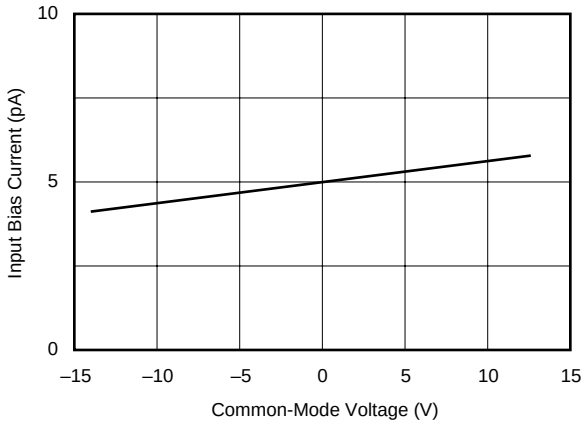
CHANNEL SEPARATION vs FREQUENCY



INPUT BIAS AND INPUT OFFSET CURRENT vs TEMPERATURE



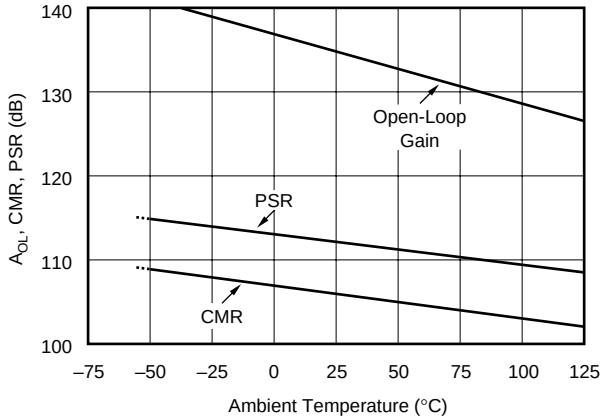
INPUT BIAS CURRENT vs INPUT COMMON-MODE VOLTAGE



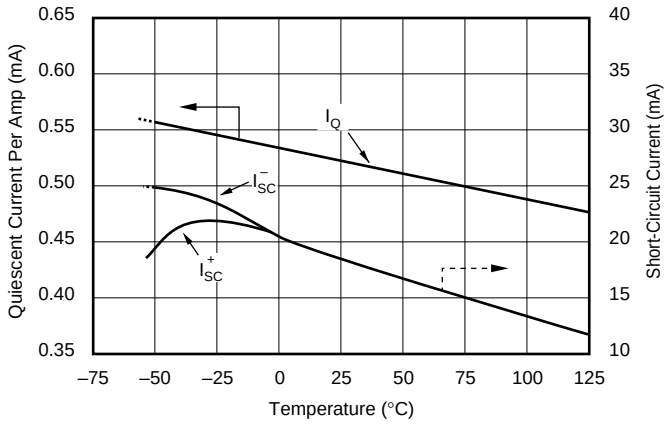
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = ±15V, and R_L = 10kΩ, unless otherwise noted.

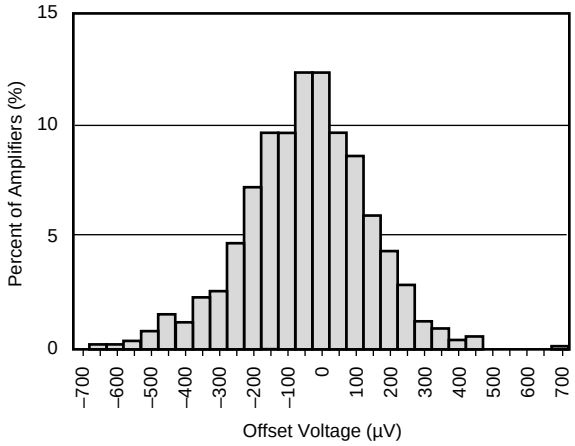
A_{OL}, CMR, PSR vs TEMPERATURE



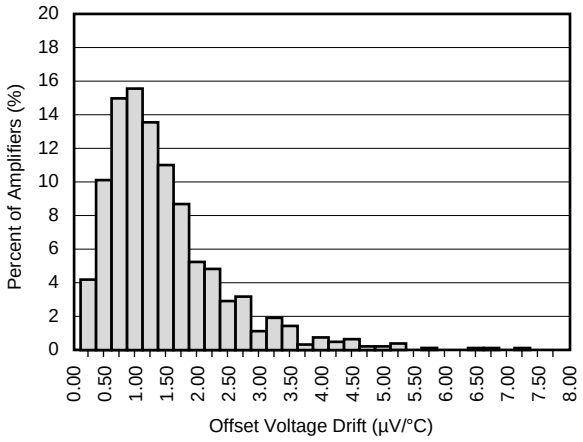
QUIESCENT CURRENT AND SHORT-CIRCUIT CURRENT vs TEMPERATURE



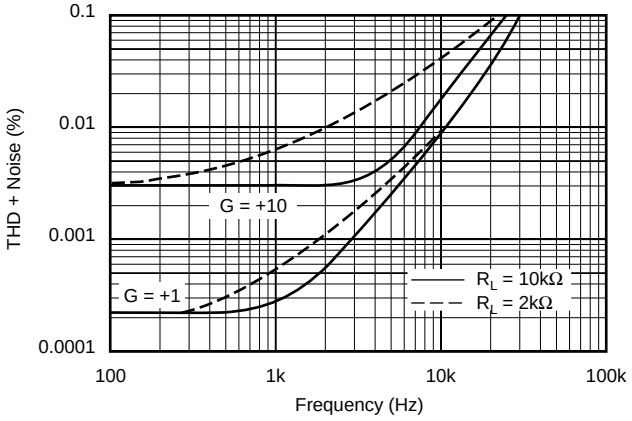
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



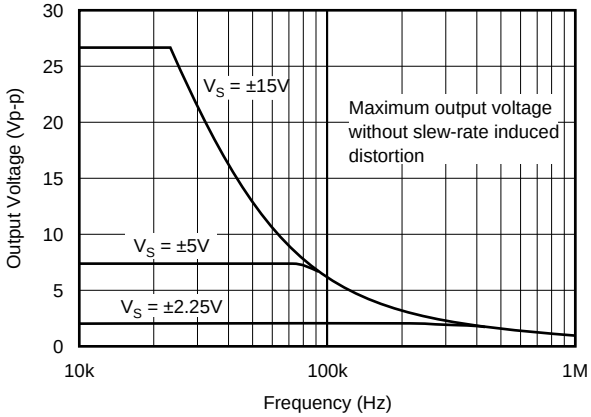
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



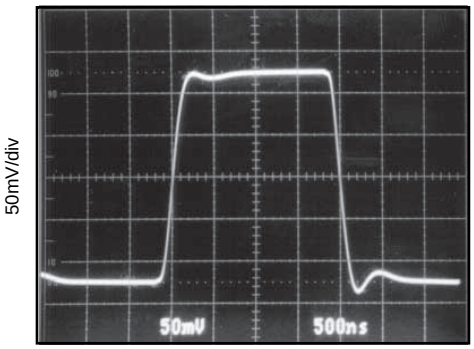
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



TYPICAL CHARACTERISTICS (Cont.)

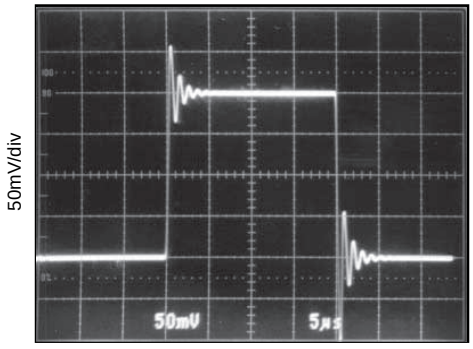
At T_A = +25°C, V_S = ±15V, and R_L = 10kΩ, unless otherwise noted.

SMALL-SIGNAL STEP RESPONSE
G =1, C_L = 100pF



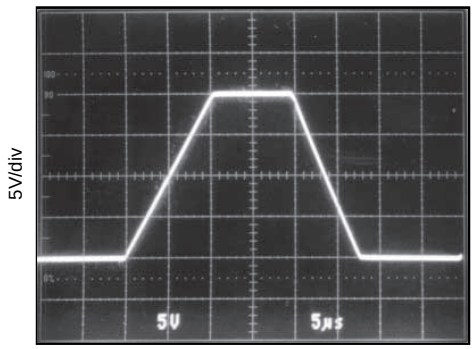
500ns/div

SMALL-SIGNAL STEP RESPONSE
G = 1, C_L = 1000pF



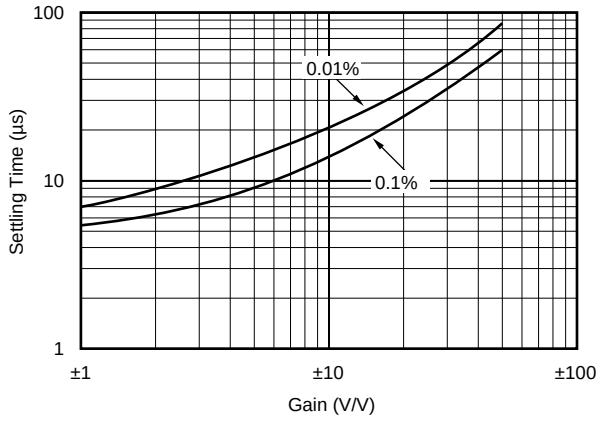
5µs/div

LARGE-SIGNAL STEP RESPONSE
G = 1, C_L = 100pF

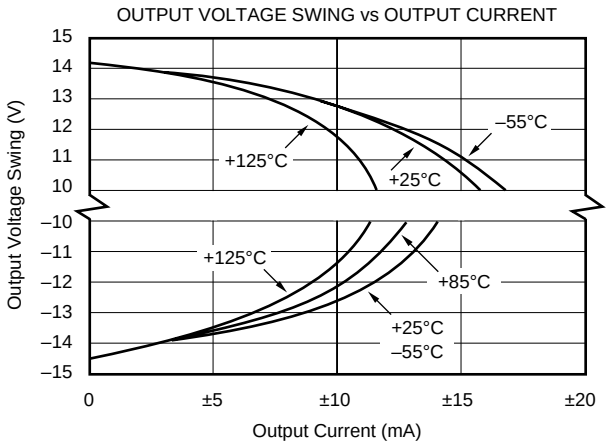


5µs/div

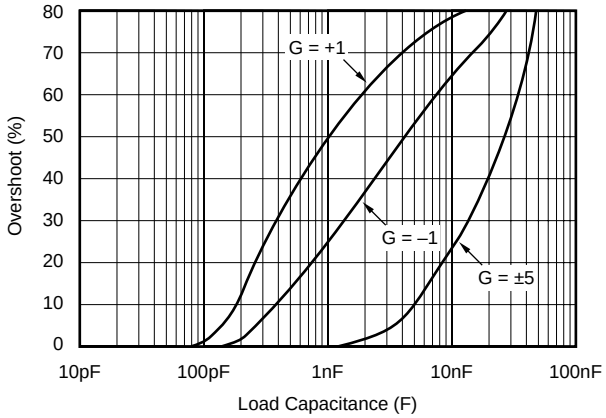
SETTLING TIME vs GAIN



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



SMALL-SIGNAL OVERSHOOT
vs LOAD CAPACITANCE



APPLICATIONS INFORMATION

OPA130 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. Power supply pins should be bypassed with 10nF ceramic capacitors or larger.

OPA130 op amps are free from unexpected output phase-reversal common with FET op amps. Many FET-input op amps exhibit phase-reversal of the output when the input common-mode voltage range is exceeded. This can occur in voltage-follower circuits, causing serious problems in control loop applications. OPA130 series op amps are free from this undesirable behavior. All circuitry is completely independent in dual and quad versions, assuring normal behavior when one amplifier in a package is overdriven or short-circuited.

OPERATING VOLTAGE

OPA130 series op amps operate with power supplies from ±2.25V to ±18V with excellent performance. Although specifications are production tested with ±15V supplies, most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the typical performance curves.

OFFSET VOLTAGE TRIM

Offset voltage of OPA130 series amplifiers is laser trimmed and usually requires no user adjustment. The OPA130 (single op amp version) provides offset voltage trim connections on pins 1 and 5. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 1. This adjustment should be used only to null the offset of the op amp, not to adjust system offset or offset produced by the signal source. Nulling offset that is not produced by the amplifier will change the offset voltage drift behavior of the op amp.

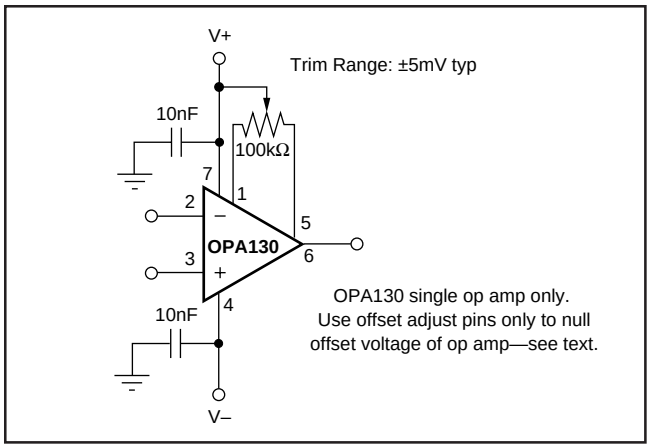


FIGURE 1. OPA130 Offset Voltage Trim Circuit.

INPUT BIAS CURRENT

The input bias current is approximately 5pA at room temperature and increases with temperature as shown in the Typical Characteristic curve *Input Bias Current vs Temperature*.

Input stage cascode circuitry assures that the input bias current remains virtually unchanged throughout the full input common-mode range of the OPA130. See the Typical Characteristic curve *Input Bias Current vs Common-Mode Voltage*.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
OPA130PA	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
OPA130UA	ACTIVE	SOIC	D	8	100	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA130UA/2K5	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA130UA/2K5E4	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA130UAE4	ACTIVE	SOIC	D	8	100	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA2130PA	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
OPA2130UA	ACTIVE	SOIC	D	8	100	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA2130UA/2K5	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA2130UA/2K5E4	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA2130UAE4	ACTIVE	SOIC	D	8	100	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA4130PA	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
OPA4130UA	ACTIVE	SOIC	D	14	58	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA4130UA/2K5	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA4130UA/2K5E4	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA4130UAE4	ACTIVE	SOIC	D	14	58	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

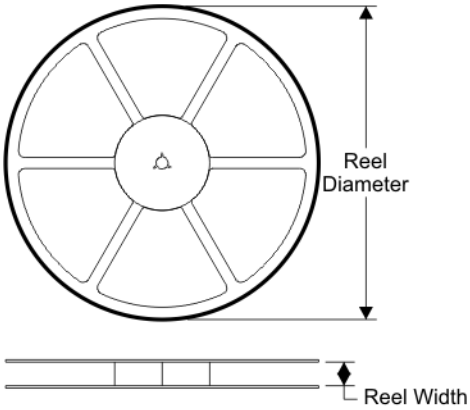
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

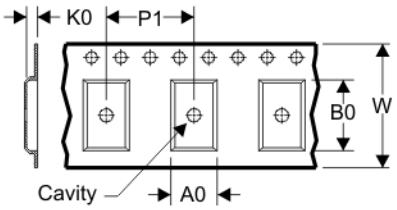
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL BOX INFORMATION

REEL DIMENSIONS

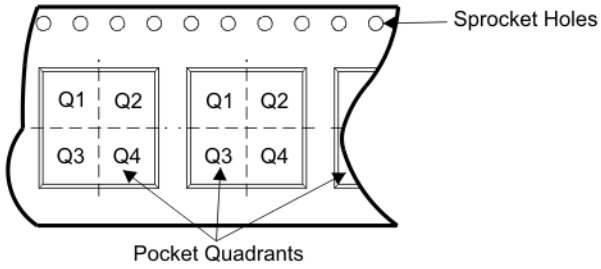


TAPE DIMENSIONS



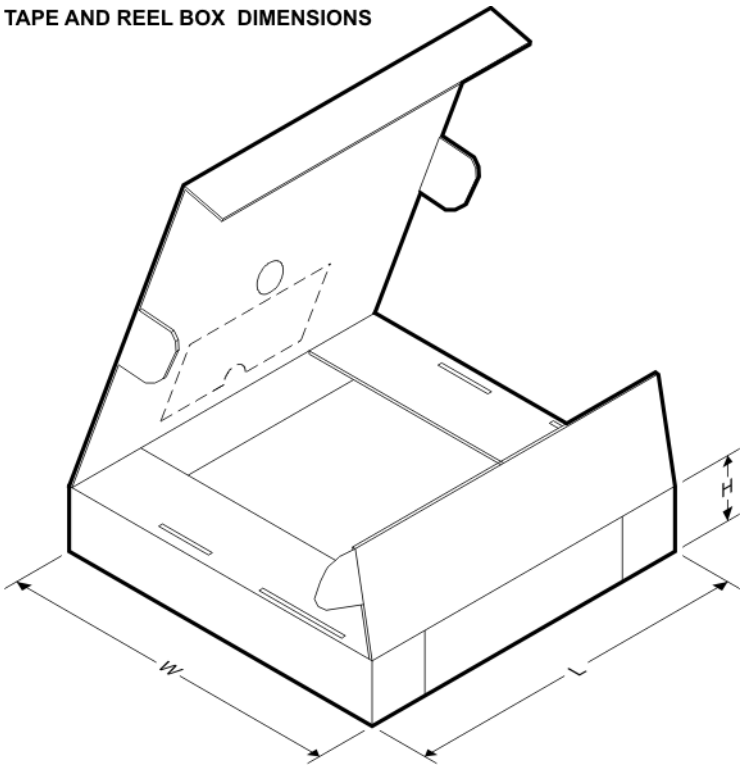
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA130UA/2K5	D	8	SITE 41	330	12	6.9	5.4	2.0	8	12	Q1
OPA2130UA/2K5	D	8	SITE 41	330	12	6.9	5.4	2.0	8	12	Q1
OPA4130UA/2K5	D	14	SITE 41	330	16	6.5	9.5	2.1	8	16	Q1

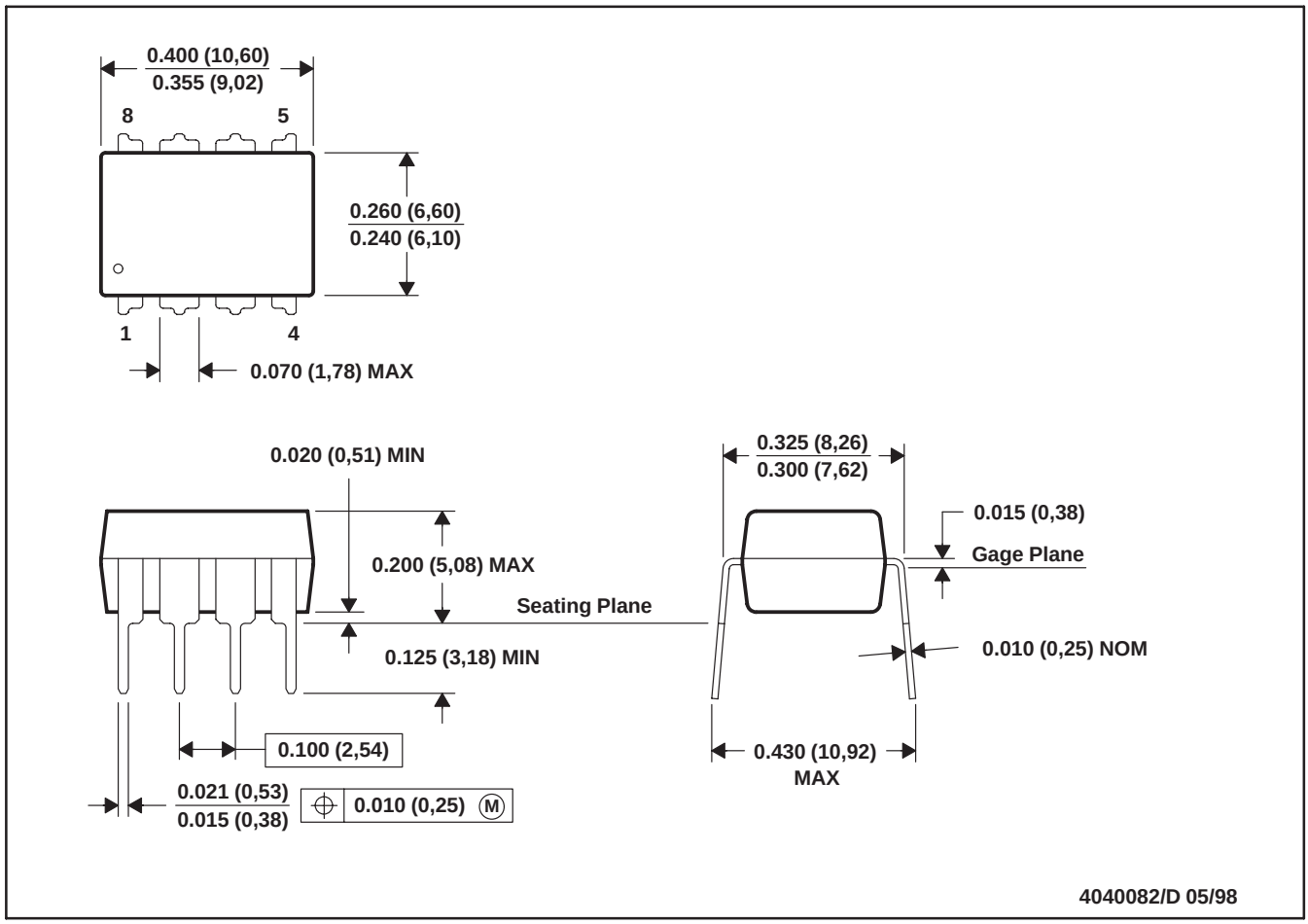
TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
OPA130UA/2K5	D	8	SITE 41	346.0	346.0	29.0
OPA2130UA/2K5	D	8	SITE 41	346.0	346.0	29.0
OPA4130UA/2K5	D	14	SITE 41	346.0	346.0	33.0

MPDI001A – JANUARY 1995 – REVISED JUNE 1999

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**



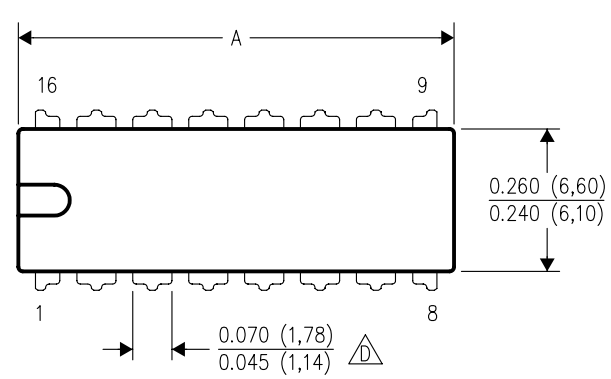
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

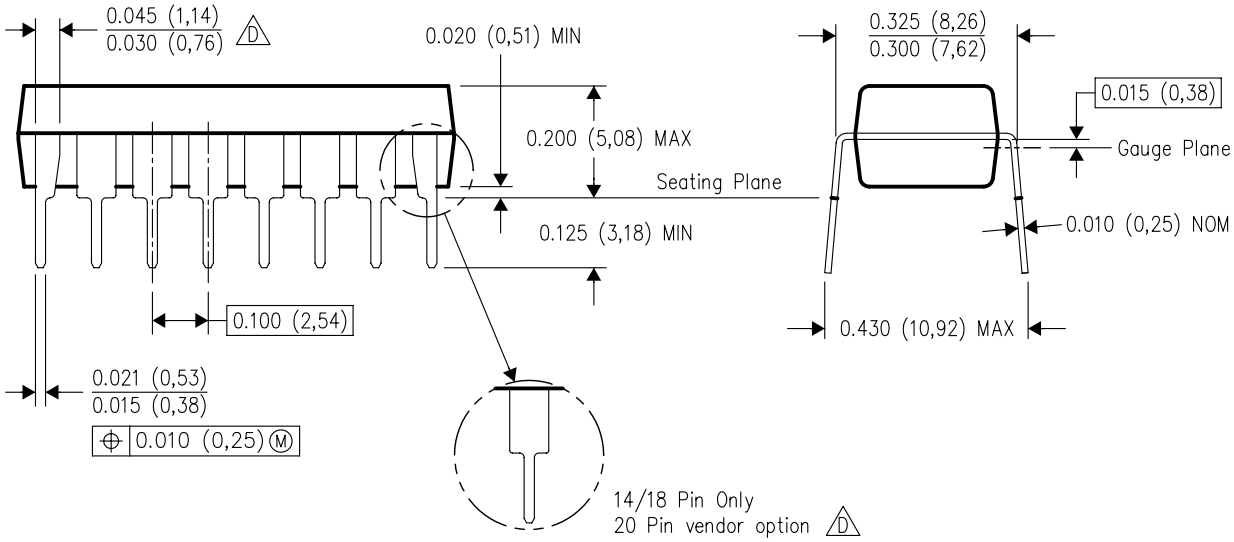
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



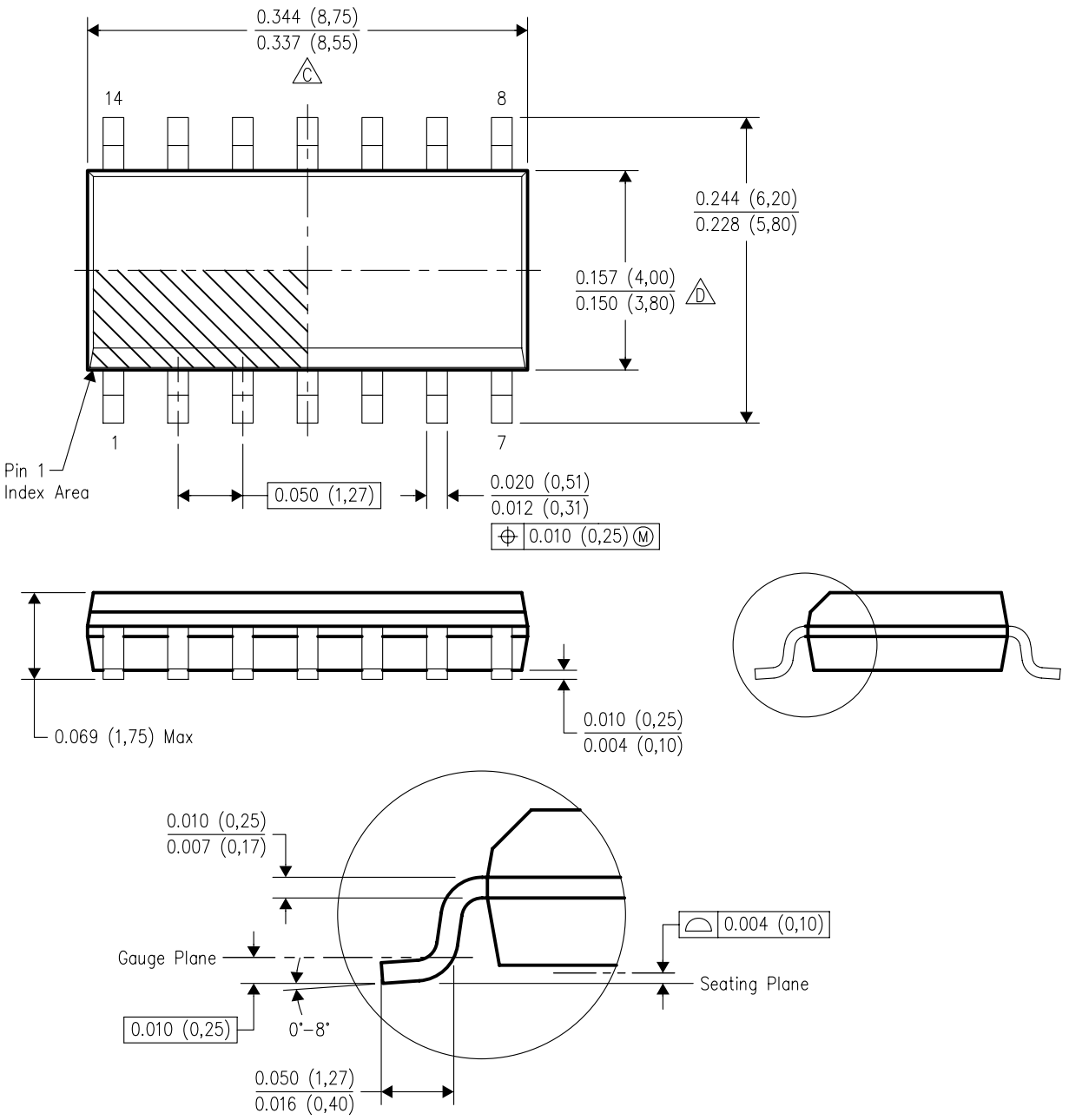
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

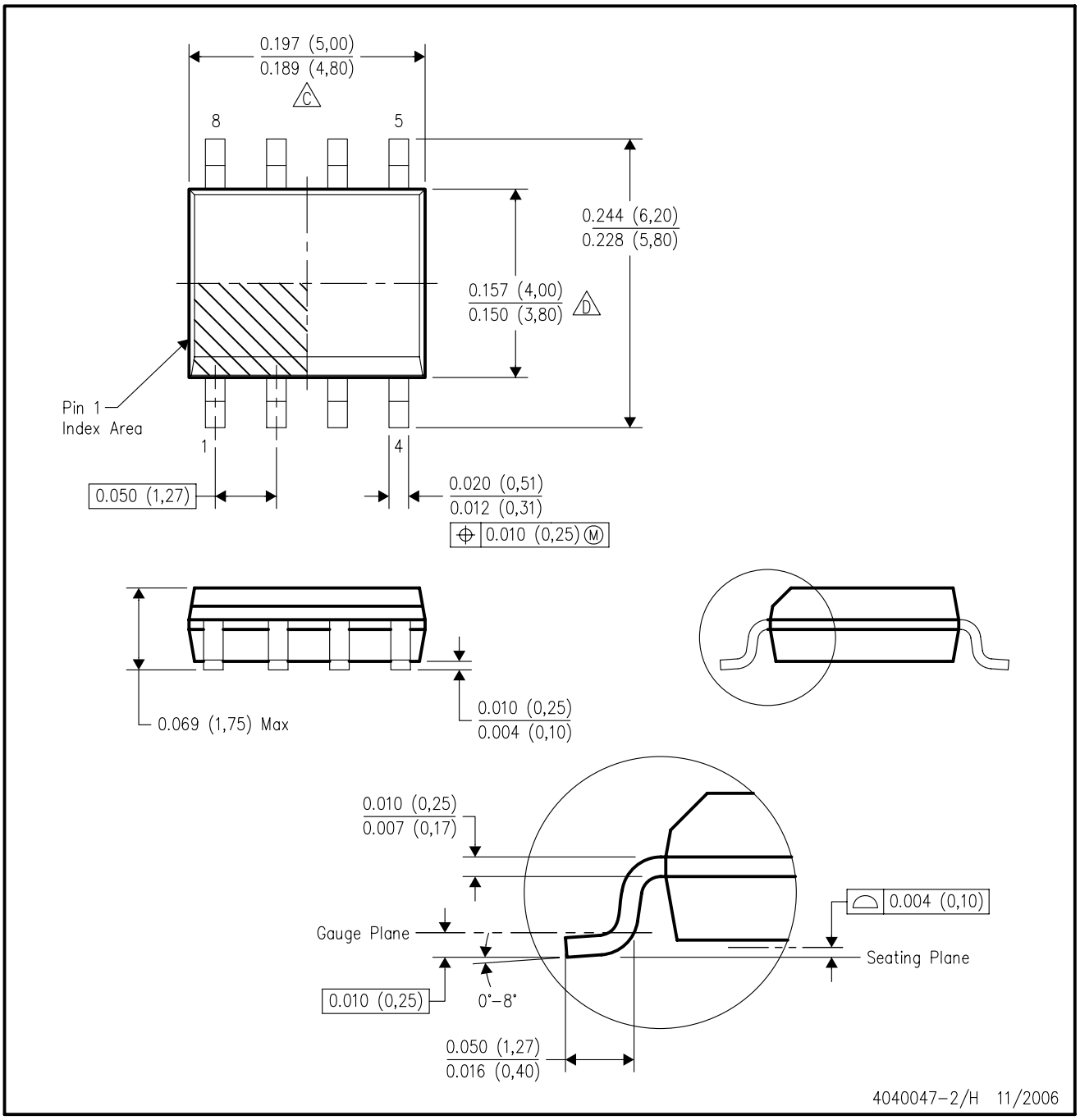
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

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