

March 1997

Features

- Low Operating Current
 - $V_{DD} = 5V$, Cycle Time $1\mu s$ 8mA
- Industry Standard Pinout
- Two Chip-Select Inputs-Simple Memory Expansion
- Memory Retention for Standby Battery Voltage of 2V Minimum
- Output-Disable for Common I/O Systems
- Three-State Data Output for Bus-Oriented Systems
- Separate Data Inputs and Outputs

Ordering Information

5V	10V	PACKAGE	TEMP. RANGE	PKG. NO.
CDP1822CE	CDP1822E	PDIP	-40°C to +85°C	E22.4
CDP1822CEX	CDP1822EX	Burn-In		E22.4
CDP1822CD	CDP1822D	SBDIP	-40°C to +85°C	D22.4A
CDP1822CDX	-	Burn-In		D22.4A

Description

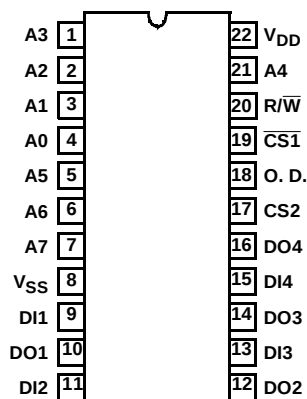
The CDP1822 and CDP1822C are 256-word by 4-bit static random-access memories designed for use in memory systems where high speed, low operating current, and simplicity in use are desirable. The CDP1822 features high speed and a wide operating voltage range. Both types have separate data inputs and outputs and utilize single power supplies of 4V to 6.5V for the CDP1822C and 4V to 10.5V for the CDP1822.

Two Chip-Select inputs are provided to simplify system expansion. An Output Disable control provides Wire-OR capability and is also useful in common Input/Output systems. The Output Disable input allows these RAMs to be used in common data Input/Output systems by forcing the output into a high-impedance state during a write operation independent of the Chip-Select input condition. The output assumes a high-impedance state when the Output Disable is at high level or when the chip is deselected by $\overline{CS1}$ and/or $\overline{CS2}$.

The high noise immunity of the CMOS technology is preserved in this design. For TTL interfacing at 5V operation, excellent system noise margin is preserved by using an external pull-up resistor at each input.

Pinout

CDP1822, CDP1822C
(PDIP, SBDIP)
TOP VIEW



OPERATIONAL MODES

MODE	INPUTS				OUTPUT
	CHIP SELECT 1 ($\overline{CS1}$)	CHIP SELECT 2 ($\overline{CS2}$)	OUTPUT DISABLE (OD)	READ/ WRITE ($\overline{R/W}$)	
Read	0	1	0	1	Read
Write	0	1	0	0	Data In
Write	0	1	1	0	High Impedance
Standby	1	X	X	X	High Impedance
Standby	X	0	X	X	High Impedance
Output Disable	X	X	1	X	High Impedance

NOTE:

Logic 1 = High, Logic 0 = Low, X = Don't Care.

CDP1822, CDP1822C

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
 (All Voltages Referenced to V_{SS} Terminal)
 CDP1822 -0.5V to +11V
 CDP1822C -0.5V to +7V
 Input Voltage Range, All Inputs -0.5V to V_{DD} +0.5V
 DC Input Current, Any One Input ± 10 mA

Thermal Information

Thermal Resistance (Typical) θ_{JA} ($^{\circ}\text{C/W}$) θ_{JC} ($^{\circ}\text{C/W}$)
 PDIP Package 75 N/A
 SBDIP Package 80 21
 Maximum Operating Temperature Range (T_A)
 Package Type D -55 $^{\circ}\text{C}$ to +125 $^{\circ}\text{C}$
 Package Type E -40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$
 Maximum Junction Temperature
 Ceramic Package 175 $^{\circ}\text{C}$
 Plastic Package 150 $^{\circ}\text{C}$
 Storage Temperature Range (T_{STG}) -65 $^{\circ}\text{C}$ to +150 $^{\circ}\text{C}$
 T_A = -40 $^{\circ}\text{C}$ to +60 $^{\circ}\text{C}$ (Package Type E) 500mW
 T_A = +60 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$ (Package Type E) Derate Linearly at
 12mW/ $^{\circ}\text{C}$ to 200mW
 Lead Temperature (During Soldering) 300 $^{\circ}\text{C}$

Recommended Operating Conditions At T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	SYMBOL	LIMITS				UNITS
		CDP1822		CDP1822C		
		MIN	MAX	MIN	MAX	
DC Operating Voltage Range		4	10.5	4	6.5	V
Input Voltage Range		V _{SS}	V _{DD}	V _{SS}	V _{DD}	V

Static Electrical Specifications At T_A = -40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$, Except as Noted

PARAMETER	SYMBOL	CONDITIONS			LIMITS						UNITS
		V _O (V)	V _{IN} (V)	V _{DD} (V)	CDP1822			CDP1822C			
					MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Quiescent Device Current	I _{DD}	-	0, 5	5	-	-	500	-	-	500	μA
		-	0, 10	10	-	-	1000	-	-	-	μA
Output Low (Sink) Current	I _{OL}	0.4	0, 5	5	2	4	-	2	4	-	mA
		0.5	0, 10	10	4.5	9	-	-	-	-	mA
Output High (Source) Current	I _{OH}	4.6	0, 5	5	-1	-2	-	-1	-2	-	mA
		9.5	0, 10	10	-2.2	-4.4	-	-	-	-	mA
Output Voltage Low-Level	V _{OL}	-	0, 5	5	-	0	0.1	-	0	0.1	V
		-	0, 10	10	-	0	0.1	-	-	-	V
Output Voltage High-Level	V _{OH}	-	0, 5	5	4.9	5	-	4.9	5	-	V
		-	0, 10	10	9.9	10	-	-	-	-	V
Input Low Voltage	V _{IL}	0.5, 4.5	-	5	-	-	1.5	-	-	1.5	V
		0.5, 9.5	-	10	-	-	3	-	-	-	V
Input High Voltage	V _{IH}	0.5, 9.5	-	5	3.5	-	-	3.5	-	-	V
		0.5, 9.5	-	10	7	-	-	-	-	-	V
Input Leakage Current	I _{IN}	-	0, 5	5	-	-	±5	-	-	±5	μA
		-	0, 10	10	-	-	±10	-	-	-	μA

CDP1822, CDP1822C

Static Electrical Specifications At $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, Except as Noted (Continued)

PARAMETER	SYMBOL	CONDITIONS			LIMITS						UNITS
		V _O (V)	V _{IN} (V)	V _{DD} (V)	CDP1822			CDP1822C			
					MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Operating Current (Note 2)	I _{DD1}	-	0, 5	5	-	4	8	-	4	8	mA
		-	0, 10	10	-	8	16	-	-	-	mA
Three-State Output Leakage Current	I _{OUT}	0, 5	0, 5	5	-	-	±5	-	-	±5	µA
		0, 10	0, 10	10	-	-	±10	-	-	-	µA
Input Capacitance	C _{IN}	-	-	-	-	5	7.5	-	5	7.5	pF
Output Capacitance	C _{OUT}	-	-	-	-	10	15	-	10	15	pF

NOTES:

1. Typical values are for $T_A = +25^{\circ}\text{C}$ and nominal V_{DD} .
2. Outputs open circuited; Cycle time = $1\mu\text{s}$.

Dynamic Electrical Specifications At $T_A = -40$ to $+85^{\circ}\text{C}$, $V_{DD} \pm 5\%$, Input $t_R, t_F = 20\text{ns}$, $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100\text{pF}$

PARAMETER	TEST CONDITIONS	LIMITS						UNITS
	V _{DD} (V)	CD1822			CDP1822C			
		(NOTE 1) MIN	(NOTE 2) TYP	MAX	(NOTE 1) MIN	(NOTE 2) TYP	MAX	
Read Cycle Times (Figure 1)								
Read Cycle t _{RC}	5	450	-	-	450	-	-	ns
	10	250	-	-	-	-	-	ns
Access from Address t _{AA}	5	-	250	450	-	250	450	ns
	10	-	150	250	-	-	-	ns
Output Valid from $\overline{\text{Chip-Select 1}}$ t _{DOA1}	5	-	250	450	-	250	450	ns
	10	-	150	250	-	-	-	ns
Output Valid from Chip-Select 2 t _{DOA2}	5	-	250	450	-	250	450	ns
	10	-	150	250	-	-	-	ns
Output Valid from Output Disable t _{DOA3}	5	-	-	200	-	-	200	ns
	10	-	-	110	-	-	-	ns
Output Hold from $\overline{\text{Chip-Select 1}}$ t _{DOH1}	5	20	-	-	20	-	-	ns
	10	20	-	-	-	-	-	ns
Output Hold from Chip-Select 2 t _{DOH2}	5	20	-	-	20	-	-	ns
	10	20	-	-	-	-	-	ns
Output Hold from Output Disable t _{DOH3}	5	20	-	-	20	-	-	ns
	10	20	-	-	-	-	-	ns

CDP1822, CDP1822C

Dynamic Electrical Specifications At $T_A + -40$ to $+85^{\circ}\text{C}$, $V_{DD} \pm 5\%$, Input $t_R, t_F = 20\text{ns}$, $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100 \text{ pF}$ (Continued)

PARAMETER	TEST CONDITIONS	LIMITS						UNITS
	V _{DD} (V)	CD1822			CDP1822C			
		(NOTE 1) MIN	(NOTE 2) TYP	MAX	(NOTE 1) MIN	(NOTE 2) TYP	MAX	

NOTES:

1. Time required by a limit device to allow for indicated function.
2. Typical values are for $T_A = 25^{\circ}\text{C}$ and nominal V_{DD} .

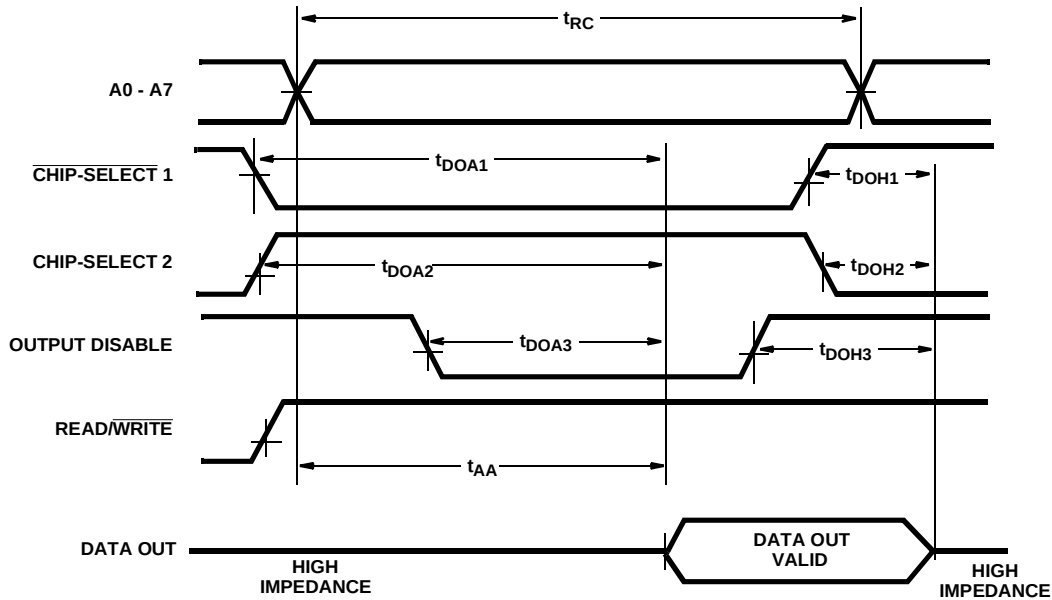


FIGURE 1. READ CYCLE TIMING WAVEFORMS

Dynamic Electrical Specifications At $T_A + -40$ to $+85^{\circ}\text{C}$, $V_{DD} \pm 5\%$, Input $t_R, t_F = 20\text{ns}$, $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100 \text{ pF}$.

PARAMETER	TEST CONDITIONS	LIMITS						UNITS
		CD1822			CDP1822C			
	V _{DD} (V)	(NOTE 1) MIN	(NOTE 2) TYP	MAX	(NOTE 1) MIN	(NOTE 2) TYP	MAX	
Read Cycle Times (Figure 2)								
Write Cycle t _{WC}	5	500	-	-	500	-	-	ns
	10	300	-	-	-	-	-	ns
Address Setup t _{AS}	5	200	-	-	200	-	-	ns
	10	110	-	-	-	-	-	ns
Write Recovery t _{WR}	5	50	-	-	50	-	-	ns
	10	40	-	-	-	-	-	ns
Write Width t _{WRW}	5	250	-	-	250	-	-	ns
	10	150	-	-	-	-	-	ns

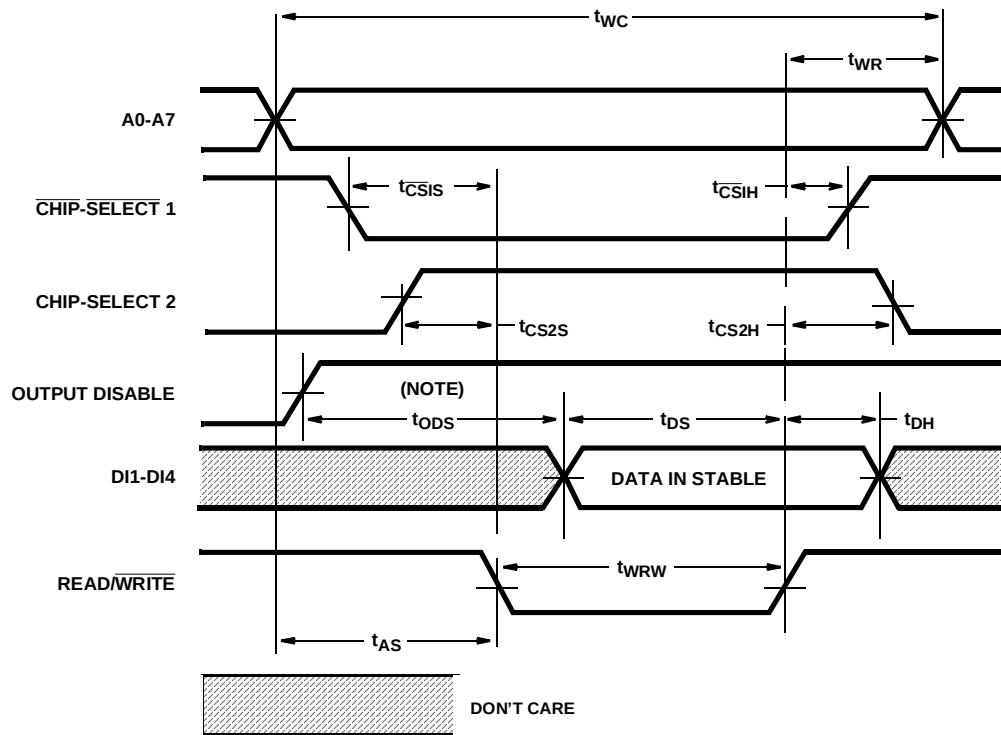
CDP1822, CDP1822C

Dynamic Electrical Specifications At $T_A + -40$ to $+85^{\circ}\text{C}$, $V_{DD} \pm 5\%$, Input $t_R, t_F = 20\text{ns}$, $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100 \text{ pF}$. **(Continued)**

PARAMETER		TEST CONDITIONS	LIMITS						UNITS
			CD1822			CDP1822C			
		V _{DD} (V)	(NOTE 1) MIN	(NOTE 2) TYP	MAX	(NOTE 1) MIN	(NOTE 2) TYP	MAX	
Input Data Setup Time t _{DS}	5	250	-	-	250	-	-	ns	
	10	150	-	-	-	-	-	ns	
Data Hold t _{DH}	5	50	-	-	50	-	-	ns	
	10	40	-	-	-	-	-	ns	
Chip-Select 1 Setup t _{CS1S}	5	200	-	-	200	-	-	ns	
	10	110	-	-	-	-	-	ns	
Chip-Select 2 Setup t _{CS2S}	5	200	-	-	200	-	-	ns	
	10	110	-	-	-	-	-	ns	
Chip-Select 1 Hold t _{CS1H}	5	0	-	-	0	-	-	ns	
	10	0	-	-	0	-	-	ns	
Chip-Select 2 Hold t _{CS2H}	5	0	-	-	0	-	-	ns	
	10	0	-	-	0	-	-	ns	
Output Disable Set-Up t _{ODS}	5	200	-	-	200	-	-	ns	
	10	110	-	-	-	-	-	ns	

NOTES:

1. Time required by a limit device to allow for indicated function.
2. Typical values are for $T_A = 25^{\circ}\text{C}$ and nominal V_{DD} .



NOTE: t_{ODS} is required for common I/O operation only. For separate I/O operations, output disable is don't care.

FIGURE 2. WRITE CYCLE TIME WAVEFORMS

Data Retention Specifications At $T_A = -40$ to $+85^{\circ}\text{C}$, see Figure 3.

PARAMETER		TEST CONDITIONS		LIMITS						UNITS
				CDP1822			CDP1822C			
		V _{DR} (V)	V _{DD} (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Min. Data Retention Voltage	V _{DR}	-	-	-	1.5	2	-	1.5	2	V
Data Retention Quiescent Current	I _{DD}	2	-	-	30	100	-	30	100	μA
Chip Deselect to Data Retention Time	t _{CDR}	-	5	600	-	-	600	-	-	ns
		-	10	300	-	-	-	-	-	ns
Recovery to Normal Operation Time	t _{RC}	-	5	600	-	-	600	-	-	ns
		-	10	300	-	-	-	-	-	ns
V _{DD} to V _{DR} Rise and Fall Time	t _R , t _F	2	5	1	-	-	1	-	-	μA

NOTE: Typical values are for $T_A = 25^{\circ}\text{C}$ and nominal V_{DD} .

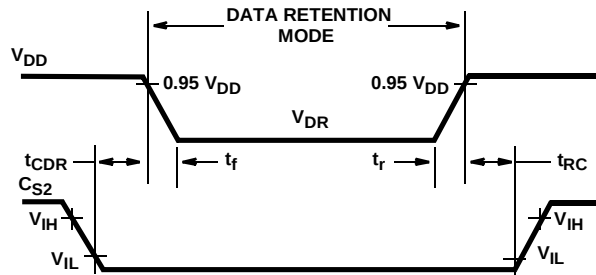


FIGURE 3. LOW V_{DD} DATA RETENTION TIME WAVEFORMS

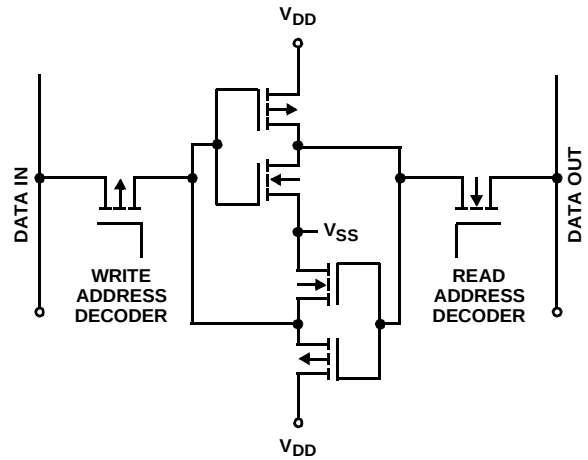


FIGURE 4. MEMORY CELL CONFIGURATION

CDP1822, CDP1822CS

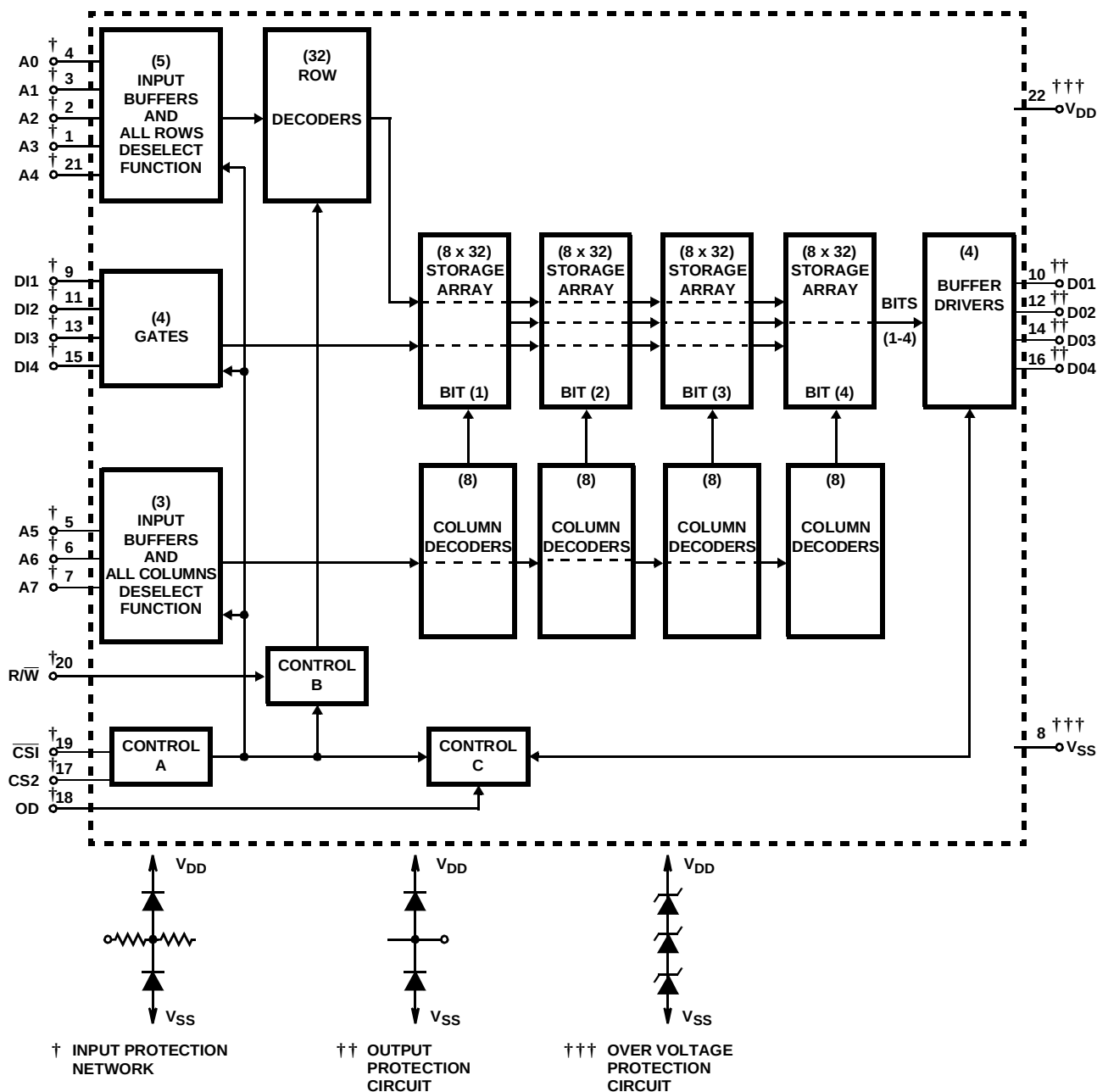


FIGURE 5. FUNCTIONAL BLOCK DIAGRAM FOR CDP1822 AND CDP1822CS
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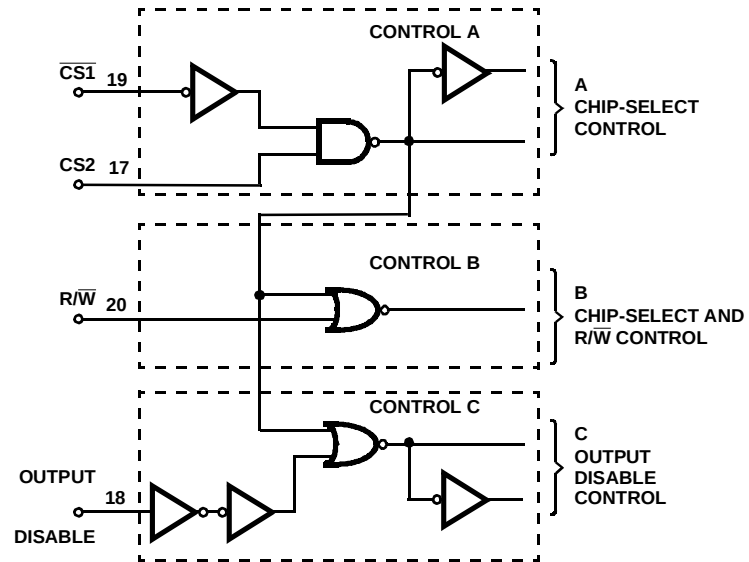


FIGURE 6. LOGIC DIAGRAM OF CONTROLS FOR CDP1822 AND CDP1822C