

2.5V or 3.3V, 200-MHz, 14 Output Zero Delay Buffer

Features

- Output frequency range: 8.3 MHz to 200 MHz
- Input frequency range: 4.2 MHz to 125 MHz
- 2.5V or 3.3V operation
- Split 2.5V/3.3V outputs
- 14 Clock outputs: Drive up to 28 clock lines
- 1 Feedback clock output
- 2 LVCMOS reference clock inputs
- 150 ps max output-output skew
- PLL bypass mode
- Spread Aware™
- Output enable/disable
- Industrial temperature range: -40°C to +85°C
- 52-Pin 1.0-mm TQFP package

Description

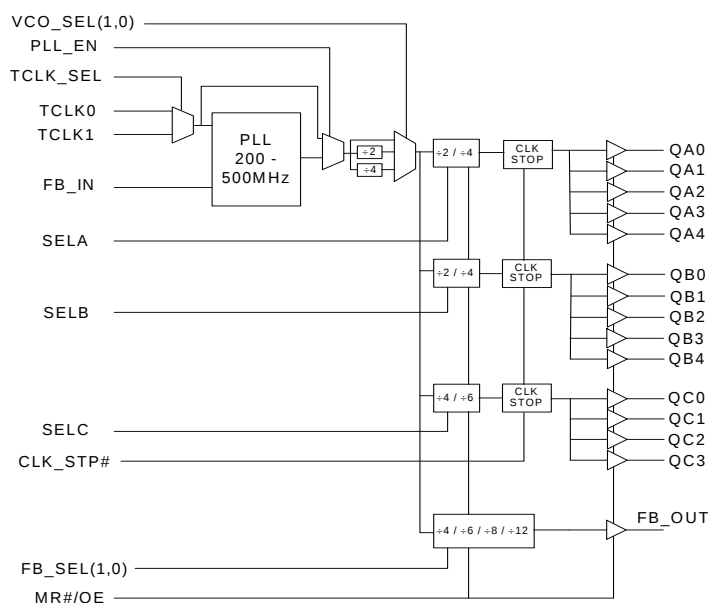
The CY29775 is a low-voltage high-performance 200-MHz PLL-based zero delay buffer designed for high-speed clock distribution applications.

The CY29775 features two reference clock inputs and provides 14 outputs partitioned in 3 banks of 5, 5, and 4 outputs. Bank A and Bank B divide the VCO output by 4 or 8 while Bank C divides by 8 or 12 per SEL(A:C) settings, see [Function Table \(Bank A, B, and C\) on page 4](#). These dividers allow output to input ratios of 6:1, 4:1, 3:1, 2:1, 3:2, 4:3, 1:1, and 2:3. Each LVCMOS compatible output can drive 50Ω series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces giving the device an effective fanout of 1:28.

The PLL is ensured stable given that the VCO is configured to run between 200 MHz to 500 MHz. This allows a wide range of output frequencies from 8.3 MHz to 200 MHz. For normal operation, the external feedback input, FB_IN, is connected to the feedback output, FB_OUT. The internal VCO is running at multiples of the input reference clock set by the feedback divider, see [Frequency Table on page 4](#).

When PLL_EN is LOW, PLL is bypassed and the reference clock directly feeds the output dividers. This mode is fully static and the minimum input clock frequency specification does not apply.

Block Diagram



Pinouts

Figure 1. Pin Diagram - 52-Pin 1.0-mm TQFP package

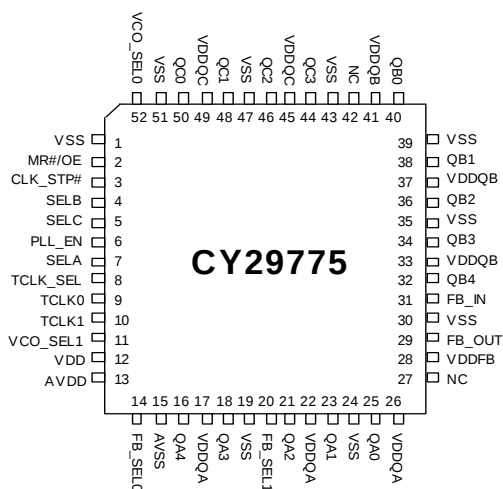


Table 1. Pin Definition - 52-Pin 1.0-mm TQFP package

Pin ^[1]	Name	IO	Type	Description
9	TCLK0	I, PD	LVC MOS	LVC MOS/LVTTL reference clock input
10	TCLK1	I, PU	LVC MOS	LVC MOS/LVTTL reference clock input
16, 18, 21, 23, 25	QA(4:0)	O	LVC MOS	Clock output bank A
32, 34, 36, 38, 40	QB(4:0)	O	LVC MOS	Clock output bank B
44, 46, 48, 50	QC(3:0)	O	LVC MOS	Clock output bank C
29	FB_OUT	O	LVC MOS	Feedback clock output. Connect to FB_IN for normal operation.
31	FB_IN	I, PU	LVC MOS	Feedback clock input. Connect to FB_OUT for normal operation. This input must be at the same voltage rail as input reference clock. See <i>Table 2</i> on page 4.
2	MR#/OE	I, PU	LVC MOS	Output enable/disable input. See <i>Table 3</i> on page 4.
3	CLK_STP#	I, PU	LVC MOS	Clock stop enable/disable input. See <i>Table 3</i> on page 4.
6	PLL_EN	I, PU	LVC MOS	PLL enable/disable input. See <i>Table 3</i> on page 4.
8	TCLK_SEL	I, PD	LVC MOS	Reference select input. See <i>Table 3</i> on page 4.
11, 52	VCO_SEL(1,0)	I, PD	LVC MOS	VCO divider select input. See <i>Tables 3, 4 and 5</i> .
7, 4, 5	SEL(A:C)	I, PD	LVC MOS	Frequency select input, Bank (A:C). See <i>Table 4</i> on page 4.
20, 14	FB_SEL(1,0)	I, PD	LVC MOS	Feedback dividers select inputs. See <i>Table 5</i> on page 5.
17, 22, 26	VDDQA	Supply	VDD	2.5V or 3.3V Power supply for bank A output clocks ^[2,3]
33, 37, 41	VDDQB	Supply	VDD	2.5V or 3.3V Power supply for bank B output clocks ^[2,3]

Notes

1. PU = Internal pull up, PD = Internal pull down
2. A 0.1-μF bypass capacitor must be placed as close as possible to each positive power pin (<0.2"). If these bypass capacitors are not close to the pins their high frequency filtering characteristics is cancelled by the lead inductance of the traces.
3. AVDD and VDD pins must be connected to a power supply level that is at least equal or higher than that of VDDQA, VDDQB, VDDQC, and VDDFB power supply pins.

Table 1. Pin Definition - 52-Pin 1.0-mm TQFP package (Continued)

Pin ^[1]	Name	IO	Type	Description
45, 49	VDDQC	Supply	VDD	2.5V or 3.3V Power supply for bank C output clocks ^[2,3]
28	VDDFB	Supply	VDD	2.5V or 3.3V Power supply for feedback output clock ^[2,3]
13	AVDD	Supply	VDD	2.5V or 3.3V Power supply for PLL ^[2,3]
12	VDD	Supply	VDD	2.5V or 3.3V Power supply for core and inputs ^[2,3]
15	AVSS	Supply	Ground	Analog Ground
1, 19, 24, 30, 35, 39, 43, 47, 51	VSS	Supply	Ground	Common Ground
27, 42	NC			No Connection

Table 2. Frequency Table

Feedback Output Divider	VCO	Input Frequency Range (AVDD = 3.3V)	Input Frequency Range (AVDD = 2.5V)
÷8	Input Clock * 8	25 MHz to 62.5 MHz	25 MHz to 50 MHz
÷12	Input Clock * 12	16.6 MHz to 41.6 MHz	16.6 MHz to 33.3 MHz
÷16	Input Clock * 16	12.5 MHz to 31.25 MHz	12.5 MHz to 25 MHz
÷24	Input Clock * 24	8.3 MHz to 20.8 MHz	8.3 MHz to 16.6 MHz
÷32	Input Clock * 32	6.25 MHz to 15.625 MHz	6.25 MHz to 12.5 MHz
÷48	Input Clock * 48	4.2 MHz to 10.4 MHz	4.2 MHz to 8.3 MHz
÷4	Input Clock * 4	50 MHz to 125 MHz	50 MHz to 100 MHz
÷6	Input Clock * 6	33.3 MHz to 83.3 MHz	33.3 MHz to 66.6 MHz
÷8	Input Clock * 8	25 MHz to 62.5 MHz	25 MHz to 50 MHz
÷12	Input Clock * 12	16.6 MHz to 41.6 MHz	16.6 MHz to 33.3 MHz

Table 3. Function Table (configuration controls)

Control	Default	0	1
TCLK_SEL	0	TCLK0	TCLK1
VCO_SEL0	0	VCO÷2 (mid input frequency range)	VCO÷4 (low input frequency range)
VCO_SEL1	0	Gated by VCO_SEL0	VCO (high input frequency range)
PLL_EN	1	Bypass mode, PLL disabled. The input clock connects to the output dividers	PLL enabled. The VCO output connects to the output dividers
MR#/OE	1	Outputs disabled (three-state) and reset of the device. During reset/output disable the PLL feedback loop is open and the VCO running at its minimum frequency. The device is reset by the internal power on reset (POR) circuitry during power up.	Outputs enabled
CLK_STP#	1	QA, QB, and QC outputs disabled in LOW state. FB_OUT is not affected by CLK_STP#.	Outputs enabled

Table 4. Function Table (Bank A, B, and C)

VCO_SEL1	VCO_SEL0	SELA	QA(4:0)	SELB	QB(4:0)	SELC	QC(3:0)
0	0	0	÷4	0	÷4	0	÷8
0	0	1	÷8	1	÷8	1	÷12
0	1	0	÷8	0	÷8	0	÷16
0	1	1	÷16	1	÷16	1	÷24
1	x	0	÷2	0	÷2	0	÷4
1	x	1	÷4	1	÷4	1	÷6

Table 5. Function Table (FB_OUT)

VCO_SEL1	VCO_SEL0	FB_SEL1	FB_SEL0	FB_OUT
0	0	0	0	÷8
0	0	0	1	÷16
0	0	1	0	÷12
0	0	1	1	÷24
0	1	0	0	÷16
0	1	0	1	÷32
0	1	1	0	÷24
0	1	1	1	÷48
1	x	0	0	÷4
1	x	0	1	÷8
1	x	1	0	÷6
1	x	1	1	÷12

Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V _{DD}	DC Supply Voltage		−0.3	5.5	V
V _{DD}	DC Operating Voltage	Functional	2.375	3.465	V
V _{IN}	DC Input Voltage	Relative to V _{SS}	−0.3	V _{DD} + 0.3	V
V _{OUT}	DC Output Voltage	Relative to V _{SS}	−0.3	V _{DD} + 0.3	V
V _{TT}	Output termination Voltage		−	V _{DD} ÷ 2	V
LU	Latch Up Immunity	Functional	200	−	mA
R _{PS}	Power Supply Ripple	Ripple Frequency < 100 kHz	−	150	mVp-p
T _S	Temperature, Storage	Non Functional	−65	+150	°C
T _A	Temperature, Operating Ambient	Functional	−40	+85	°C
T _J	Temperature, Junction	Functional	−	150	°C
Ø _{JC}	Dissipation, Junction to Case	Functional	−	23	°C/W
Ø _{JA}	Dissipation, Junction to Ambient	Functional	−	55	°C/W
ESD _H	ESD Protection (Human Body Model)		2000	−	Volts
FIT	Failure in Time	Manufacturing test	10		ppm

DC Electrical Specifications ($V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$)

Parameter	Description	Condition	Min	Typ.	Max	Unit
V_{IL}	Input Voltage, Low	LVC MOS	–	–	0.8	V
V_{IH}	Input Voltage, High	LVC MOS	2.0	–	$V_{DD} + 0.3$	V
V_{OL}	Output Voltage, Low ^[4]	$I_{OL} = 24 \text{ mA}$	–	–	0.55	V
		$I_{OL} = 12 \text{ mA}$	–	–	0.30	
V_{OH}	Output Voltage, High ^[4]	$I_{OH} = -24 \text{ mA}$	2.4	–	–	V
I_{IL}	Input Current, Low ^[5]	$V_{IL} = V_{SS}$	–	–	–100	μA
I_{IH}	Input Current, High ^[5]	$V_{IL} = V_{DD}$	–	–	100	μA
I_{DDA}	PLL Supply Current	A_{VDD} only	–	5	10	mA
I_{DDQ}	Quiescent Supply Current	All V_{DD} pins except A_{VDD}	–	–	1	mA
I_{DD}	Dynamic Supply Current	Outputs loaded at 100 MHz	–	225	–	mA
		Outputs loaded at 200 MHz	–	290	–	
C_{IN}	Input Pin Capacitance		–	4	–	pF
Z_{OUT}	Output Impedance		12	15	18	Ω

DC Electrical Specifications ($V_{DD} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$)

Parameter	Description	Condition	Min	Typ.	Max	Unit
V_{IL}	Input Voltage, Low	LVC MOS	–	–	0.7	V
V_{IH}	Input Voltage, High	LVC MOS	1.7	–	$V_{DD} + 0.3$	V
V_{OL}	Output Voltage, Low ^[4]	$I_{OL} = 15 \text{ mA}$	–	–	0.6	V
V_{OH}	Output Voltage, High ^[4]	$I_{OH} = -15 \text{ mA}$	1.8	–	–	V
I_{IL}	Input Current, Low ^[5]	$V_{IL} = V_{SS}$	–	–	–100	μA
I_{IH}	Input Current, High ^[5]	$V_{IL} = V_{DD}$	–	–	100	μA
I_{DDA}	PLL Supply Current	A_{VDD} only	–	5	10	mA
I_{DDQ}	Quiescent Supply Current	All V_{DD} pins except A_{VDD}	–	–	1	mA
I_{DD}	Dynamic Supply Current	Outputs loaded at 100 MHz	–	135	–	mA
		Outputs loaded at 200 MHz	–	160	–	
C_{IN}	Input Pin Capacitance		–	4	–	pF
Z_{OUT}	Output Impedance		14	18	22	Ω

Notes

4. Driving one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, each output drives up to two 50 Ω series terminated transmission lines.
5. Inputs have pull up or pull down resistors that affect the input current

AC Electrical Specifications ($V_{DD} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$)

Parameter ^[6]	Description	Condition	Min	Typ.	Max	Unit
f_{VCO}	VCO Frequency		200	–	400	MHz
f_{in}	Input Frequency	$\div 4$ Feedback	50	–	100	MHz
		$\div 6$ Feedback	33.3	–	66.6	
		$\div 8$ Feedback	25	–	50	
		$\div 12$ Feedback	16.7	–	33.3	
		$\div 16$ Feedback	12.5	–	25	
		$\div 24$ Feedback	8.3	–	16.7	
		$\div 32$ Feedback	6.3	–	12.5	
		$\div 48$ Feedback	4.2	–	8.3	
		Bypass mode (PLL_EN = 0)	0	–	200	
f_{refDC}	Input Duty Cycle		25	–	75	%
t_r, t_f	TCLK Input Rise/Fall Time	0.7V to 1.7V	–	–	1.0	ns
f_{MAX}	Maximum Output Frequency	$\div 2$ Output	100	–	200	MHz
		$\div 4$ Output	50	–	100	
		$\div 6$ Output	33.3	–	66.6	
		$\div 8$ Output	25	–	50	
		$\div 12$ Output	16.7	–	33.3	
		$\div 16$ Output	12.5	–	25	
		$\div 24$ Output	8.3	–	16.7	
DC	Output Duty Cycle		45	–	55	%
t_r, t_f	Output Rise/Fall times	0.7V to 1.8V	0.1	–	1.0	ns
$t_{(\phi)}$	Propagation Delay (static phase offset)	TCLK to FB_IN, does not include jitter	–100	–	100	ps
$t_{sk(O)}$	Output-to-Output Skew	Skew within Bank	–	–	150	ps
$t_{sk(B)}$	Bank-to-Bank Skew	Banks at same frequency	–	–	150	ps
		Banks at different frequency	–	–	225	
$t_{PLZ, HZ}$	Output Disable Time		–	–	10	ns
$t_{PZL, ZH}$	Output Enable Time		–	–	10	ns
BW	PLL Closed Loop Bandwidth (–3 dB)	VCO_SEL = 0	–	0.5 - 1.0	–	MHz
		VCO_SEL = 1	–	1.0 - 2.0	–	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	Same frequency	–	–	150	ps
		Multiple frequencies	–	–	300	
$t_{JIT(PER)}$	Period Jitter		–	–	100	ps
$t_{JIT(\phi)}$	IO Phase Jitter		–	–	150	ps
t_{LOCK}	Maximum PLL Lock Time		–	–	1	ms

Note

6. AC characteristics apply for parallel output termination of 50Ω to V_{TT} . Parameters are guaranteed by characterization and are not 100% tested.

AC Electrical Specifications ($V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$)

Parameter ^[6]	Description	Condition	Min	Typ.	Max	Unit
f_{VCO}	VCO Frequency		200	–	500	MHz
f_{in}	Input Frequency	$\div 4$ Feedback	50	–	125	MHz
		$\div 6$ Feedback	33.3	–	83.3	
		$\div 8$ Feedback	25	–	62.5	
		$\div 12$ Feedback	16.7	–	41.6	
		$\div 16$ Feedback	12.5	–	31.3	
		$\div 24$ Feedback	8.3	–	20.8	
		$\div 32$ Feedback	6.3	–	15.6	
		$\div 48$ Feedback	4.2	–	10.4	
		Bypass mode (PLL_EN = 0)	0	–	200	
f_{refDC}	Input Duty Cycle		25	–	75	%
t_r, t_f	TCLK Input Rise/Fall Time	0.8V to 2.0V	–	–	1.0	ns
f_{MAX}	Maximum Output Frequency	$\div 2$ Output	100	–	200	MHz
		$\div 4$ Output	50	–	125	
		$\div 6$ Output	33.3	–	83.3	
		$\div 8$ Output	25	–	62.5	
		$\div 12$ Output	16.7	–	41.6	
		$\div 16$ Output	12.5	–	31.3	
		$\div 24$ Output	8.3	–	20.8	
DC	Output Duty Cycle		45	–	55	%
t_r, t_f	Output Rise/Fall times	0.8V to 2.4V	0.1	–	1.0	ns
$t_{(\phi)}$	Propagation Delay (static phase offset)	TCLK to FB_IN, same V_{DD} , does not include jitter	–100	–	100	ps
$t_{sk(O)}$	Output-to-Output Skew	Skew within Bank	–	–	150	ps
tsk(B)	Bank-to-Bank Skew	Banks at same voltage, same frequency	–	–	150	ps
		Banks at same voltage, different frequency	–	–	225	
		Banks at different voltage	–	–	250	
$t_{PLZ, HZ}$	Output Disable Time		–	–	10	ns
$t_{PZL, ZH}$	Output Enable Time		–	–	10	ns
BW	PLL Closed Loop Bandwidth (–3dB)	VCO_SEL = 0	–	0.5 - 1.0	–	MHz
		VCO_SEL = 1	–	1.0 - 2.0	–	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	Same frequency	–	–	150	ps
		Multiple frequencies	–	–	300	
$t_{JIT(PER)}$	Period Jitter		–	–	100	ps
$t_{JIT(\phi)}$	IO Phase Jitter	IO at same V_{DD}	–	–	150	ps
t_{LOCK}	Maximum PLL Lock Time		–	–	1	ms

Figure 2. AC Test Reference for $V_{DD} = 3.3V / 2.5V$

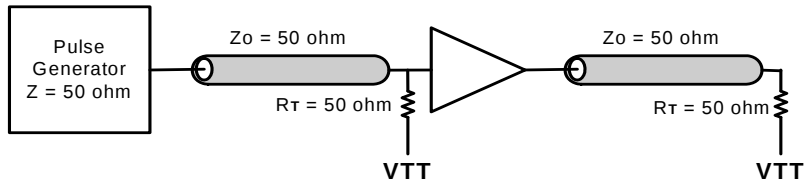


Figure 3. Propagation Delay $t(\phi)$, Static Phase Offset

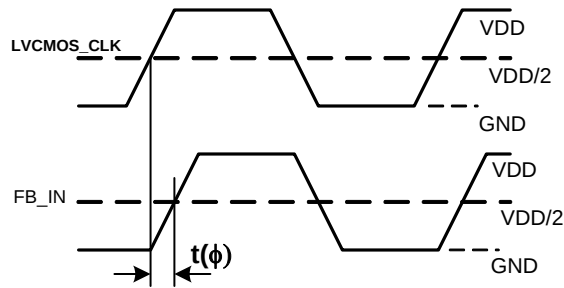


Figure 4. Output Duty Cycle (DC)

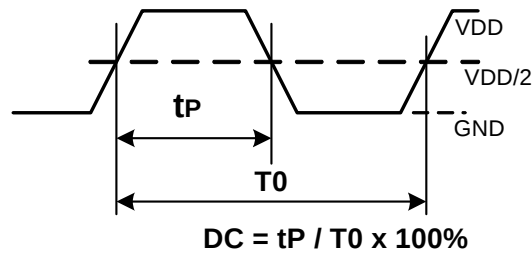
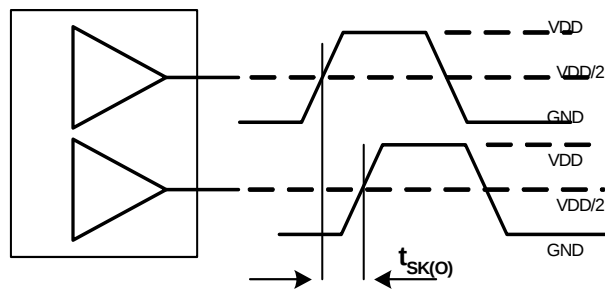


Figure 5. Output-to-Output Skew, $t_{sk(O)}$

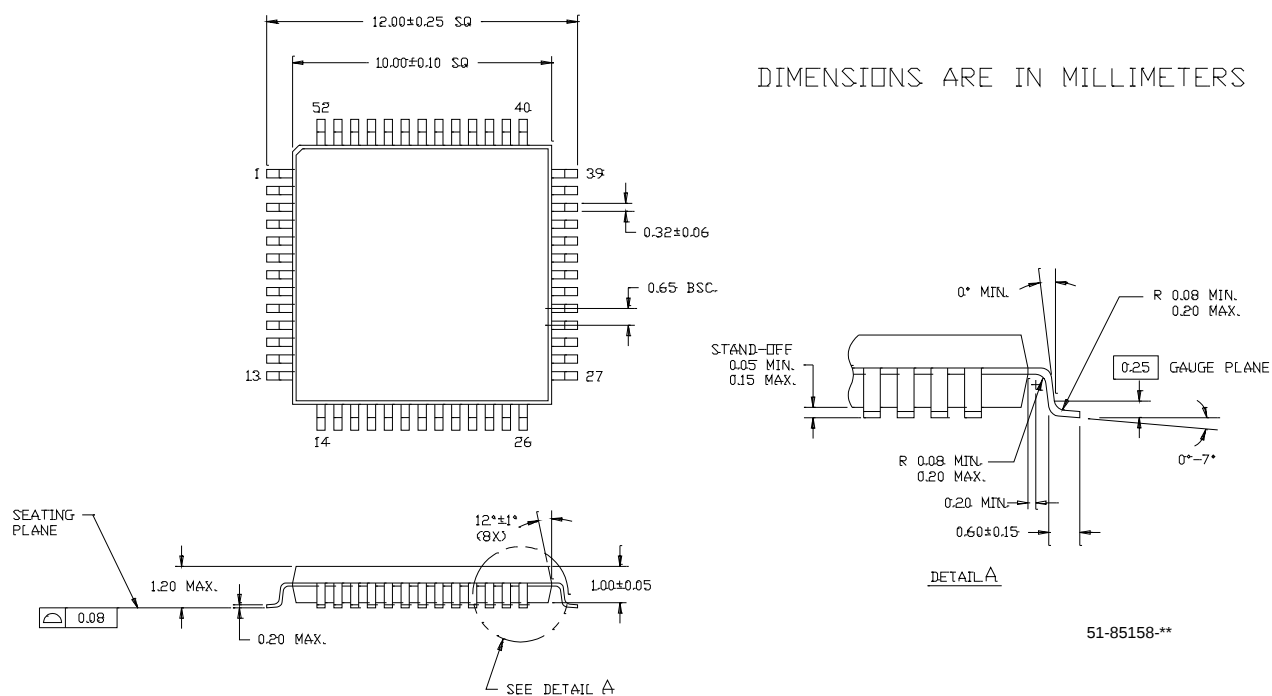


Ordering Information

Part Number	Package Type	Product Flow	Status
CY29775AI	52-pin TQFP	Industrial, -40°C to +85°C	Obsolete
CY29775AIT	52-pin TQFP -Tape and Reel	Industrial, -40°C to 85°C	Obsolete
Pb-free			
CY29775AXI	52-pin TQFP	Industrial, -40°C to +85°C	Active
CY29775AXIT	52-pin TQFP -Tape and Reel	Industrial, -40°C to 85°C	Active

Package Drawing and Dimension

Figure 6. 52-Lead Thin Plastic Quad Flat Pack (10 x 10 x 1.0 mm) A52B



Document History Page

Document Title: CY29775 2.5V or 3.3V, 200-MHz, 14 Output Zero Delay Buffer Document #: 38-07480				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	125955	04/29/03	RGL	New Data Sheet
*A	1875214	See ECN	WWZ/AESA	Added Pb-free part numbers and updated device status

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