National Semiconductor

NMC2816 16k (2k x 8) Electrically Erasable PROM

Max Access/Current	NMC2816-25	NMC2816-35	NMC2816-45
Max Access Time (ns)	250	350	450
Max Active Current (mA)	110	110	110
Max Standby Current (mA)	50	50	50

General Description

The NMC2816 is a 16,384-bit electrically erasable and programmable read-only memory (E^2PROM) fabricated using National's high speed, low power, N-channel double silicon gate technology. The electrical erase/write capability of the NMC2816 makes it ideal for a wide variety of applications requiring in-system, non-volatile erase and write.

The device operates from a 5V power supply in the read mode and, with its very fast read access speed, is compatible with high performance microprocessors.

The NMC2816 is deselected when pin 18 is high and is automatically placed in the standby mode. This mode provides a 52% reduction in power with no increase in access time. The NMC2816 also has an output enable control to eliminate bus contention in a system environment.

The NMC2816 can be easily erased and reprogrammed in a byte-by-byte mode and the entire memory array erased in a chip erase mode. Byte erase mode is identical to byte write mode, with all data inputs at logic ones (TTL high).

Features

- 2048 x 8 organization
- Fully static
- Reliable floating gate technology
- Very fast access time
  - 250 ns max (NMC2816-25)
  - 350 ns max (NMC2816-35)
  - 450 ns max (NMC2816-45)
- Single byte erase/write capability
- 10 ms byte erase/write time
- Chip erase time of 10 ms
- Conforms to JEDEC byte-wide family standard
- Microprocessor compatible architecture
- Low power dissipation
  - 610 mW max (active power ICC + IPP)
  - 295 mW max (standby power ICC + IPP)

Block and Connection Diagrams

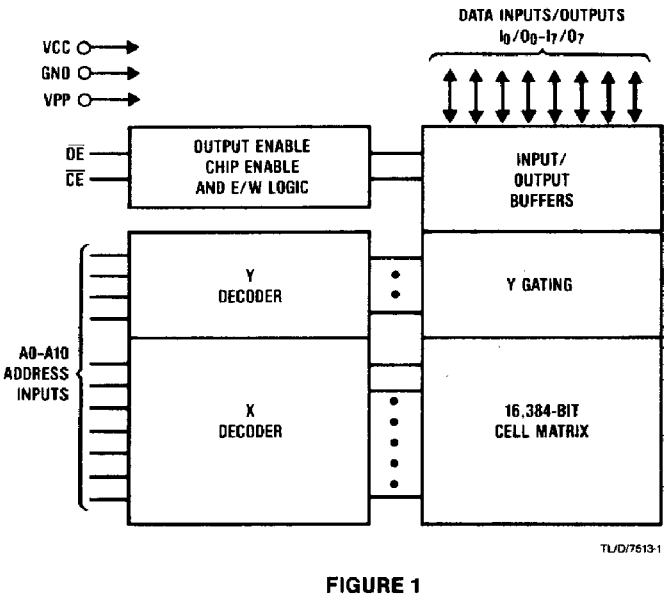
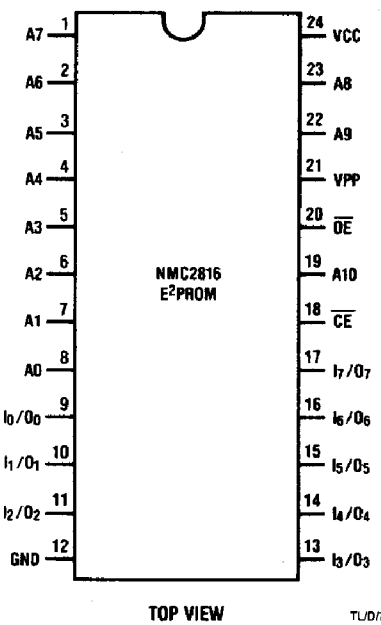


FIGURE 1

Pin Names

A0-A10	Addresses	O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable	I_0-I_7	Data Inputs
$\overline{OE}$	Output Enable	VPP	Program Voltage

Dual-In-Line Package



TOP VIEW

TL/D/7513-2

FIGURE 2

Order Number NMC2816J
NS Package Number J24A

Absolute Maximum Ratings

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input or Output Voltages with Respect to Ground	+6V to −0.3V
VPP Supply Voltage with Respect to Ground During Program	+22.5V to −0.3V
Maximum Duration of VPP Supply at 22V During E/W Inhibit	24 Hrs
Maximum Duration of VPP Supply at 22V During Write/Erase Programming (Note 2)	15 ms
Lead Temperature (Soldering, 10 seconds)	300°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Conditions

Temperature Range	0°C to +70°C
VCC Power Supply (Notes 2 and 3)	5V ± 5%

DC Electrical Characteristics TA = 0°C to 70°C, VCC = 5V ± 5% (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
READ OPERATION						
ILI	Input Leakage Current	VIN = 5.25V			10	μA
ILO	Output Leakage Current	VOUT = 5.25V			10	μA
ICC2	VCC Current (Active)	$\overline{OE} = \overline{CE}$ = VIL		50	110	mA
ICC1	VCC Current (Standby)	$\overline{CE}$ = VIH		10	50	mA
IPP(R)	VPP Current (Read)	VPP = 6V, $\overline{CE}$ = VIH or VIL		1	5	mA
VIL	Input Low Voltage		−0.1		0.8	V
VIH	Input High Voltage		2.0		VCC + 1	V
VOL	Output Low Voltage	IOL = 2.1 mA			0.45	V
VOH	Output High Voltage	IOH = −400 μA	2.4			V
VPP	Read Voltage		4		6	V
WRITE OPERATION						
VPP	Write/Erase Voltage		20	21	22	V
IPP(W)	VPP Current (Write/Erase)	$\overline{OE}$ = VIH, $\overline{CE}$ = VIL, VPP = 22V		6	15	mA
$V\overline{OE}$	$\overline{OE}$ Voltage (Chip Erase)	$I\overline{OE} \leq 10$ μA	9		15	V
IPP(I)	VPP Current (Inhibit)	$\overline{CE}$ = VIH, VPP = 22V		2	5	mA
IPP(C)	VPP Current (Chip Erase)	$\overline{OE} = V\overline{OE}$, $\overline{CE}$ = VIL, VPP = 22V		2	5	mA

Capacitance TA = 25°C, f = 1 MHz (Note 1)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
CIN	Input Capacitance	VIN = 0V		5	10	pF
COUT	Output Capacitance	VOUT = 0V			10	pF
CVCC	VCC Capacitance	$\overline{OE} = \overline{CE}$ = VIH			500	pF
CVPP	VPP Capacitance	$\overline{OE} = \overline{CE}$ = VIH			50	pF

AC Test Conditions

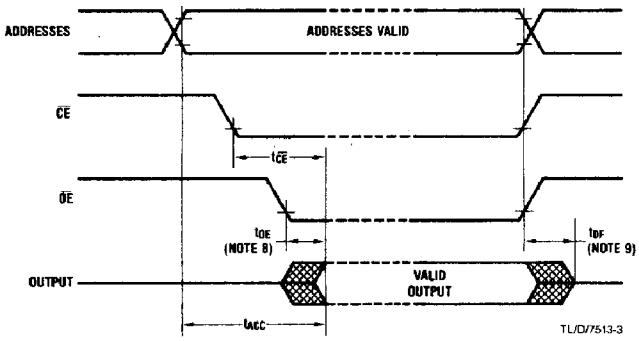
Output Load	1 TTL gate and CL = 100 pF
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Read Mode AC Electrical Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ (Notes 2 and 3)

Symbol	Parameter	Conditions	NMC2816-25			NMC2816-35			NMC2816-45			Units
			Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$			250			350			450	ns
$t_{\overline{CE}}$	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$			250			350			450	ns
$t_{\overline{OE}}$	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	10		100	10		120	10		120	ns
t_{DF}	Output Disable to Output Float (Note 9)	$\overline{CE} = \overline{OE} = V_{IL}$	0		80	0		80	0		100	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0			0			0			ns

Switching Time Waveforms (Note 6)

Read



Write Mode AC Electrical Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
t_{AS}	Address Set-Up Time		150			ns
t_{AH}	Address Hold Time		50			ns
t_{GS}	$\overline{CE}$ to VPP Set-Up Time		150			ns
t_{DS}	Data Set-Up Time	$\overline{OE} = V_{IH}$	0			ns
t_{DH}	Data Hold Time	$\overline{OE} = V_{IH}$	50			ns
t_{WP}	Write Pulse Width (Note 4)		9	10	15	ms
t_{WR}	Write Recovery Time		50			ns
t_{OS}	Chip Clear Set-Up Time		0			ns
t_{OH}	Chip Clear Hold Time		0			ns
t_{PRC}	VPP RC Time Constant		450	600	750	μs
t_{PFT}	VPP Fall Time (Note 5)				100	μs
t_{BOS}	Byte Erase/Write Set-Up Time (Note 12)		0			ns
t_{BOH}	Byte Erase/Write Hold Time (Note 12)		0			ns
t_{CH}	Chip Enable High Time		1			μs

Note 1: This parameter is only sampled and not 100% tested.

Note 2: To prevent spurious device erasure or write, VCC must be applied simultaneously or before 21V application of VPP. VPP cannot be driven to 21V without previously applying VCC.

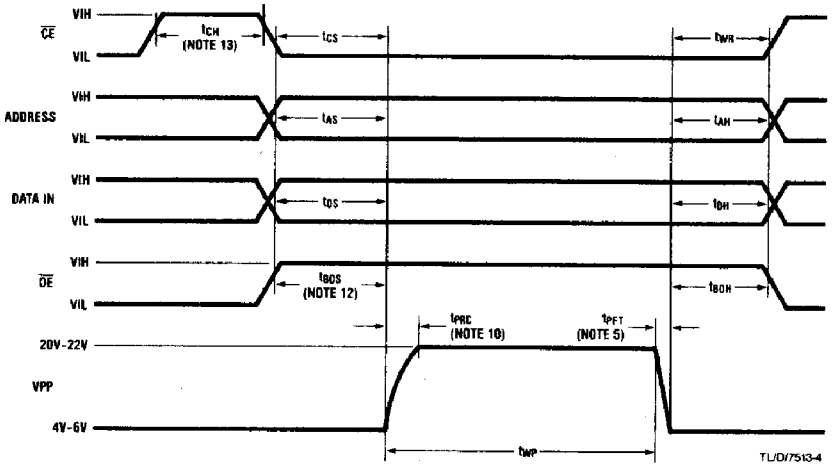
Note 3: VCC must be applied at the same time or before VPP and removed after or at the same time as VPP. To prevent damage to the device it must not be inserted into or removed from a board with power applied.

Note 4: Adherence to t_{WP} specification is important to device reliability.

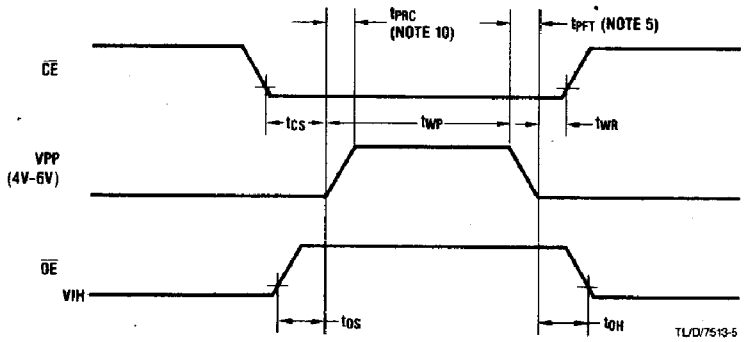
Note 5: To allow immediate read verify capability, VPP can be driven low in less than 50 ns.

Switching Time Waveforms (Note 6)

Byte Erase and Byte Write Programming Cycle (Notes 7 and 12)



Chip Erase (Note 11)



Note 6: All times shown in parentheses are minimum times and are ns unless otherwise specified.

Note 7: Prior to a data write, an erase operation must be performed. For byte erase, data in = VIH, and for chip erase, data in = don't care.

Note 8: $\overline{OE}$ may be delayed up to 230 ns after falling edge of $\overline{CE}$ without impact on t_{CE} for NMC2816-35.

Note 9: t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Note 10: The rising edge of VPP must follow an exponential waveform. That waveform's time constant is specified as t_{PRC}.

Note 11: In the chip erase mode DIN = don't care.

Note 12: In byte erase or write mode, $\overline{OE}$ must be at VIH (logic 1 state).

Note 13: $\overline{CE}$ = VIH places the chip in a low power standby condition and must be applied for a minimum time of t_{CH} before the start of any byte programming cycle.

Device Operation

The NMC2816 has six modes of operation, listed in Table I. All operational modes are designed to provide maximum microprocessor compatibility and system consistency. The device pinout is a part of the JEDEC approved byte-wide non-volatile memory family, allowing appropriate and cost-effective density and functionality upgrades.

All control inputs are TTL compatible with the exception of chip erase. The VPP voltage must be pulsed to 21V during write and erase, and held at 5V during the other two modes.

TABLE I. Mode Selection V_{CC} = 5V ± 10%

Mode \ Pin	$\overline{CE}$ (18)	$\overline{OE}$ (20)	VPP (21)	Inputs/ Outputs
Read	VIL	VIL	4V to 6V	DOUT
Standby	VIH	Don't Care	4V to 6V	Hi-Z
Byte Erase	VIL	VIH	20V to 22V	DIN = VIH
Byte Write	VIL	VIH	20V to 22V	DIN
Chip Erase (Note 11)	VIL	9V to 15V	20V to 22V	DIN = Don't Care
E/W Inhibit	VIH	Don't Care	4V to 22V	Hi-Z

Device Operation (Continued)

READ MODE

Both $\overline{CE}$ and $\overline{OE}$ must be at logic low levels to obtain information from the device. Chip enable ($\overline{CE}$) is the power control pin and could be used for device selection. The output enable ($\overline{OE}$) pin serves to gate internal data to the output pins. Assuming that the address inputs are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output ($t_{\overline{CE}}$). Data is available at the outputs after a time delay of $t_{\overline{OE}}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{\overline{OE}}$.

CHIP ERASE MODE

Should one wish to erase the entire NMC2816 array at once, the device offers a chip erase function. When the chip erase function is performed, all 2k bytes are returned to a logic 1 (FF) state.

The NMC2816's chip erase function is engaged when the output enable ($\overline{OE}$) pin is raised above 9V. When $\overline{OE}$ is greater than 9V and $\overline{CE}$ and VPP are in the normal write mode, the entire array is erased. This chip erase function takes approximately 10 ms. The data input pins are don't care during this time to allow for ease in chip erase. *Figure 3* is an example for an $\overline{OE}$ control switch.

VPP PULSE

The shape of the VPP pulse is important in ensuring long term reliability and operating characteristics. VPP must rise to 21V through an RC waveform (exponential). The t_{PRC} specification has been designed to accommodate changes of RC due to temperature variations.

Figure 4 shows an example for a VPP switch design, useful where programming will occur over the specified temperature and operating voltage conditions.

WRITE MODE

The NMC2816 is erased and reprogrammed electrically rather than optically, as opposed to EPROMs which require UV light. The device offers dramatic flexibility because both byte (single location) and chip erase are possible.

To write a particular location, that byte must be erased prior to a data write. Erasing is accomplished by applying logic 1 (TTL high) inputs to all 8 data input pins, lowering $\overline{CE}$, and applying a 21V programming signal to VPP. The $\overline{OE}$ pin must be equal to VIH during byte erase and write operations. The programming pulse width must be a minimum of 9 ms, and a maximum of 15 ms. The rising edge of VPP must conform to the RC time constant specified previously. Once the location has been erased, the same operation is repeated for a data write. The input pins in this case reflect the byte that is to be stored. $\overline{CE}$ must go from VIH to VIL at the beginning of a byte erase/write cycle and must be held high for a minimum of t_{CH} between E/W cycles.

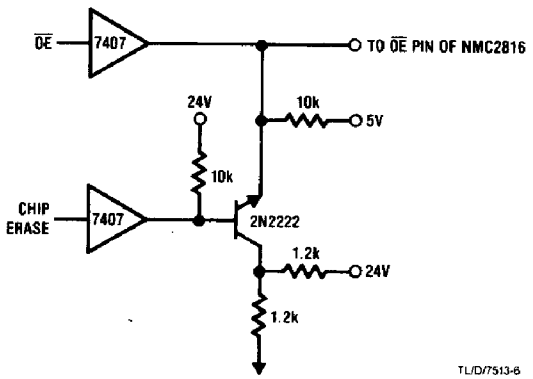
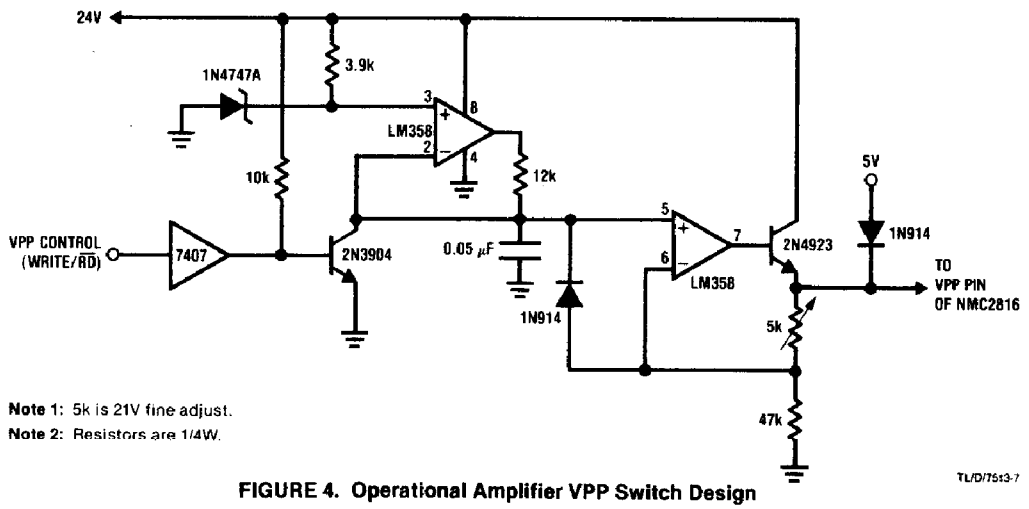


FIGURE 3. $\overline{OE}$ Chip Erase Control



Note 1: 5k is 21V fine adjust.
Note 2: Resistors are 1/4W.

FIGURE 4. Operational Amplifier VPP Switch Design

Device Operation (Continued)

A characteristic of all E^2PROMs is that the total number of erase/write cycles is not unlimited. The NMC2816 has been designed to meet applications requiring up to 1×10^4 erase/write cycles per byte. The erase/write cycling characteristic is completely byte independent. Adjacent bytes are not affected during erase/write cycling.

Because the device is designed to be written in system, all data sheet specifications (including write and erase operations) hold over the full operating temperature range (0°C to 70°C).

OUTPUT OR-TYING

Because NMC2816s are usually used in larger memory arrays, a 2-line control function is provided that accommodates this use of multiple memory connections. The 2-line control function allows low power dissipation (by deselecting unused devices), and the removal of bus contention from the system environment.

To most effectively use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded from addresses as the primary device selection function. $\overline{OE}$ (pin 20) should be made a common connection to all devices in system, and connected to the $\overline{RD}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

STANDBY MODE

The NMC2816 has a standby mode which reduces active power dissipation by 52% from 610 mW to 295 mW (ICC + IPP). The NMC2816 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.