NCP400

150 mA CMOS Low Iq Low-Dropout Voltage Regulator with Voltage Detector Output

The NCP400 is an integration of a low−dropout regulator and a voltage detector in a very small chip scale package. The voltage regulator is capable of supplying 150 mA with a low dropout of 160 mV at 100 mA. It contains a voltage reference unit, an error amplifier, comparators, PMOS power transistor, current limit and thermal shutdown protection circuits for the regulator portion.

A highly accurate voltage detector with hysteresis and an externally programmable time delay generator are implemented to prevent erratic system reset operation. It features complementary output with active low reset function.

The NCP400 is designed to work with low cost ceramic capacitors and requires only a small 1.0 μF capacitor at regulator output. Its low quiescent current is ideal for battery powered applications.

Features

- LDO Voltage Regulator and Voltage Detector Together in a Very Small Wafer Level Package, 6 Bump Flip−Chip, 1.0 x 1.5 mm
- Low Quiescent Current of 50 μA Typical
- Internal Current Limit and Thermal Shutdown Protection
- Low Cost and Small Size Ceramic Capacitors
- Input Voltage Range of 1.8 V to 5.0 V
- Voltage Regulator
  - 1.8 V (*) Output with 2% Accuracy
  - Excellent Line and Load Regulation
  - Low Dropout of 160 mV at 100 mA
- Voltage Detector
  - 2.3 V (*) Threshold with 2% Accuracy
  - Externally Programmable Time Delay Generator
  - Excellent Line and Load Regulation
- This is a Pb−Free Device

(*) Other voltages can be developed upon request.
Please contact your ON Semiconductor representative.

Typical Applications

- Memory Cards
- Cellular Phones
- Digital Still Cameras and Camcorders
- Battery Powered Equipment

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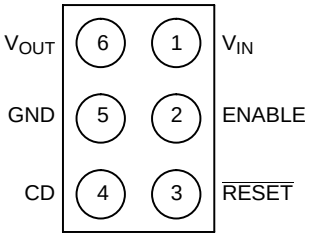
MARKING DIAGRAM

6 Bump Flip−Chip FC SUFFIX CASE 499AH

400 = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

PIN CONNECTIONS



(Bottom View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP400FCT2G	Flip−Chip (Pb−Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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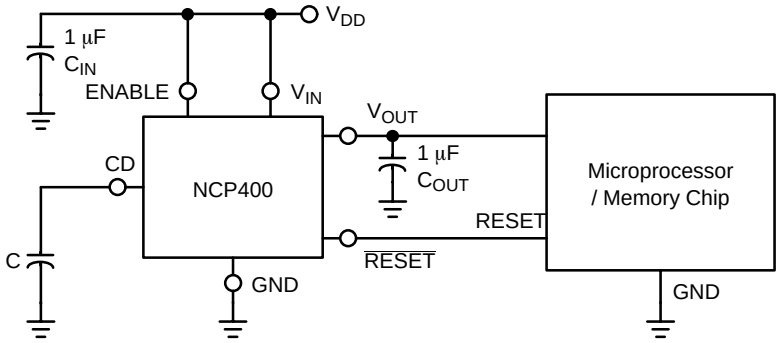
TYPICAL OPERATION CIRCUIT



$$\text{DelayTime : } (\Delta t) = \frac{(C \times 0.97\ V)}{1.56\ \mu A}$$

Figure 1. Power Supply and Reset Circuit for Microprocessor and/or Memory Chip

PIN DESCRIPTION

Pin No.	Symbol	Description
1	V_{IN}	Positive power supply input voltage.
2	ENABLE	This input is used to place the device into low–power standby. When this input is pulled low, the device is disabled. If this function is not used, ENABLE should be connected to V_{IN}.
3	$\overline{RESET}$	Voltage detect output signal.
4	CD	Delay capacitor pin.
5	GND	Power supply ground.
6	V_{OUT}	Voltage regulator output voltage.

REPRESENTATIVE BLOCK DIAGRAM

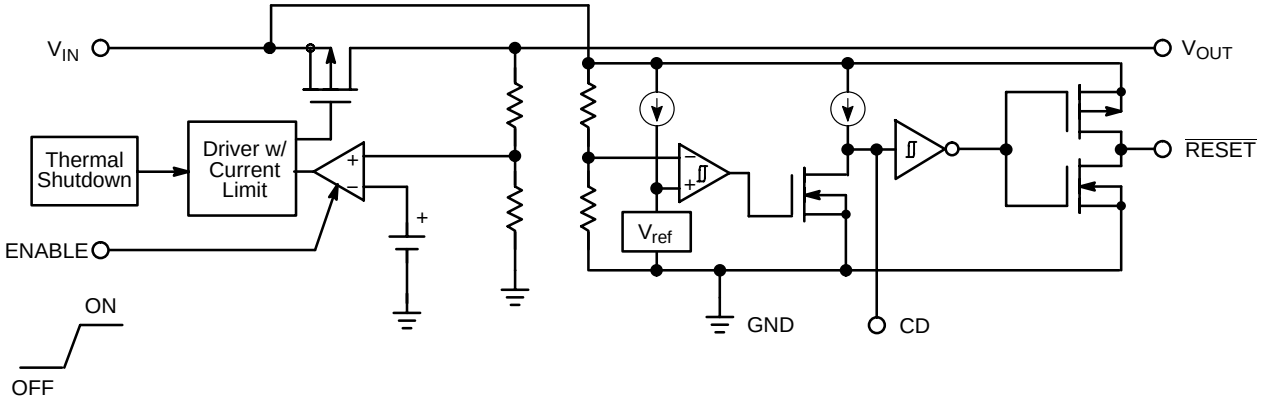


Figure 2. Representative Block Diagram

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{IN}	0 to 5.5	V
Enable Voltage	ENABLE	−0.3 to V_{IN}+0.3	V
Output Voltage	V_{OUT}	−0.3 to V_{IN}+0.3	V
Delay Capacitor Pin Voltage	V_{CD}	−0.3 to V_{IN}+0.3	V
Reset Pin Voltage	Vreset	−0.3 to V_{IN}+0.3	V
Reset Pin Current	Ireset	70	mA
Power Dissipation and Thermal Characteristics for Microbump−6 Thermal Resistance Junction−to−Air (Note 3)	$R_{\theta JA}$	Refer to Figure 22	°C/W
Operating Junction Temperature	T_J	−40 to +125	°C
Operating Ambient Temperature	T_A	−40 to +85	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

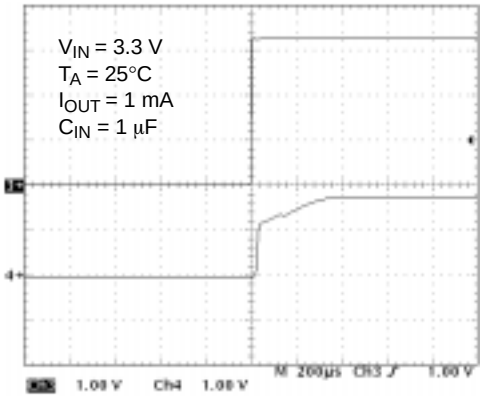
1. This device contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) ±2000 V per MIL−STD−883, Method 3015
   Machine Model (MM) ±200 V.
2. Latchup capability (85°C)100 mA DC with trigger voltage.
3. PCB top layer uses a single copper layer and is tested @ 250 mW.

ELECTRICAL CHARACTERISTICS (V_{IN} = $V_{OUT(nom.)}$ + 1.0 V, ENABLE = V_{IN}, C_{IN} = 1.0 μF, C_{OUT} = 1.0 μF, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage (T_A = –40°C to 85°C)	V_{IN}	1.8	–	5.0	V
Output Voltage (T_A= 25°C, I_{OUT} = 1.0 mA)	V_{OUT}	1.764	1.8	1.836	V
Output Voltage (T_A = –40°C to 85°C, I_{OUT} = 1.0 mA)	V_{OUT}	1.746	1.8	1.854	V
Line Regulation (I_{OUT} = 10 mA, V_{IN} = 2.8 V to 5.0 V)	Reg line	–	1.0	3.5	mV/V
Load Regulation (I_{OUT} = 1.0 mA to 150 mA)	Reg load	–	0.3	0.8	mV/mA
Maximum Output Current	$I_{OUT(nom.)}$	–	150	–	mA
Dropout Voltage (I_{OUT} = 100 mA, Measured at V_{OUT} –3.0%)	V_{IN}–V_{OUT}	–	160	200	mV
Quiescent Current (Enable Input = 0V, I_{OUT} = 0 mA) (Enable Input = V_{IN} , I_{OUT} = 1.0 mA to Io(nom.))	 I_{Q_SD} I_{Q_EN}	 – –	 0.25 37	 1.0 100	μA
Enable Input Threshold Voltage (Voltage Decreasing, Output Turns Off, Logic Low) (Voltage Increasing, Output Turns On, Logic High)	$V_{TH(EN)}$	 0.17 –	 0.25 1.25	 – 1.65	V
Output Short Circuit Current (V_{OUT} = 0 V, V_{IN} = 5.0 V) (Note 4)	$I_{OUT(MAX)}$	200	400	800	mA
Ripple Rejection (f = 1.0 kHz, Io = 60 mA)	RR	–	50	–	dB
Output Noise Voltage (f = 20 Hz to 100 kHz, I_{OUT} = 60 mA)	V_N	–	110	–	μVrms
Output Voltage Temperature Coefficient	T_C	–	±100	–	ppm°C
Detector Threshold (T_A = 25°C)	V_{DET}	2.254	2.30	2.346	V
Detector Threshold Hysteresis	V_{HYS}	0.069	0.115	0.161	V
Reset Output Current N−Channel Sink Current (Reset = 0.5 V, V_{IN} = 1.8 V) P−Channel Source Current (Reset = 2.4 V, V_{IN} = 4.5 V)	I_{RESET}	 1.0 1.0	 7.0 5.5	 – –	mA
CD Delay Pin Threshold Voltage (Pin 4) (V_{IN}=2.0 V)	$V_{TH(CD)}$	0.76	0.97	1.14	V
Delay Capacitor Pin Sink Current (Pin 4) (V_{IN} = 1.8 V, VCD = 0.5 V)	I_{CD_SINK}	 0.2	 39	 –	mA
Delay Current Pin Source Current (Pin 4) (VCD = 0, V_{IN} = 2.8 V)	I_{CD_SOURCE}	 0.78	 1.56	 3.12	μA

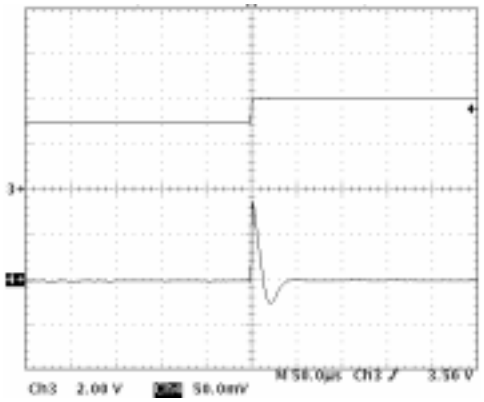
4. Values are guaranteed by design.

TYPICAL CHARACTERISTICS



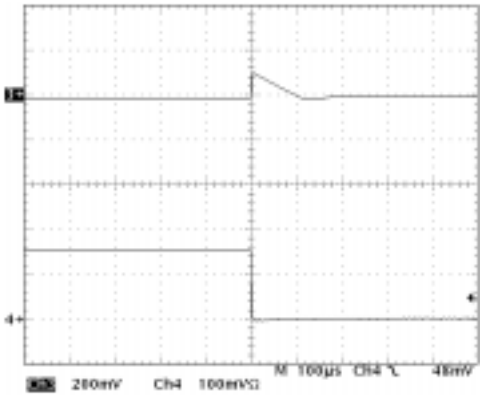
Upper Trace: Input Voltage 1 V/div
Lower Trace: Output Voltage 1 V/div

Figure 3. Turn−ON Response



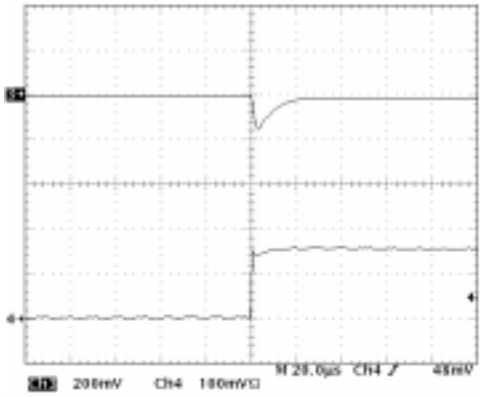
Upper Trace: Input voltage 2 V/div
Lower Trace: Output voltage 50 mV/div

Figure 4. Line Transient Response



I_{OUT} = 150 mA to 1 mA,V_{IN} = 3.3 V, C_{IN} = 1 μF
Upper Trace: Output Voltage 200 mV/div
Lower Trace: Output Loading Current 100 mA/div

Figure 5. Load Transient Response



I_{OUT} = 1 mA to 150 mA,V_{IN} = 3.3 V,C_{IN} = 1 μF
Upper Trace: Output Voltage 200 mV/div
Lower Trace: Output Loading Current 100 mA/div

Figure 6. Load Transient Response

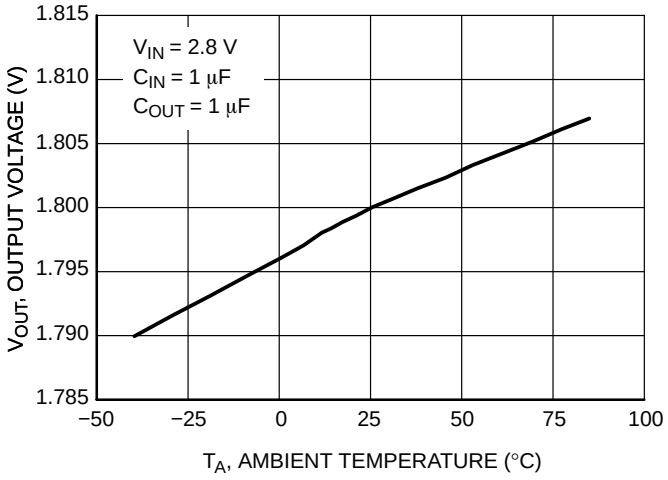


Figure 7. Output Voltage vs. Temperature

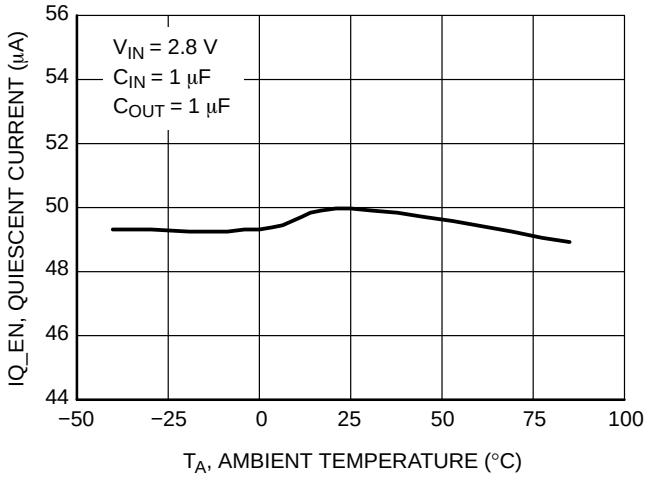


Figure 8. Quiescent Current (Enable) vs. Temperature

TYPICAL CHARACTERISTICS

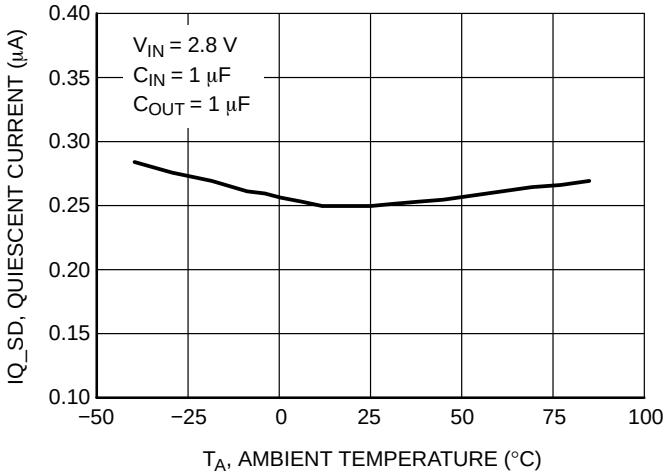


Figure 9. Quiescent Current (Shutdown) vs. Temperature

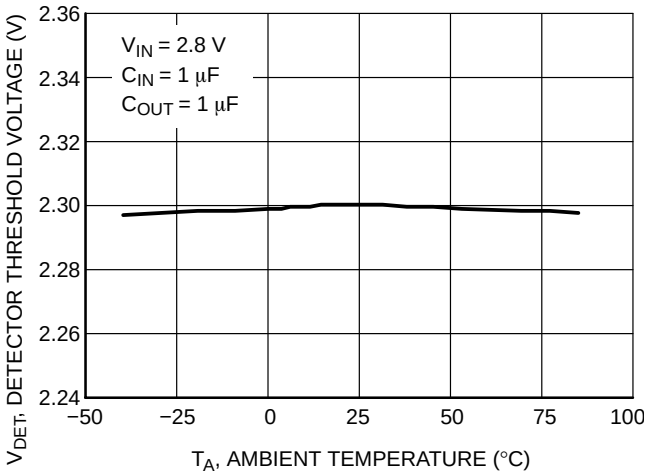


Figure 10. Detector Threshold Voltage vs. Temperature

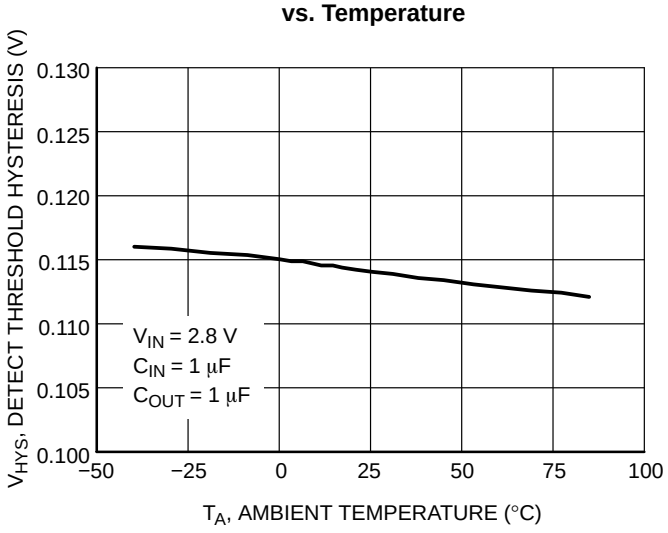


Figure 11. Dectector Threshold Hysteresis Voltage vs. Temperature

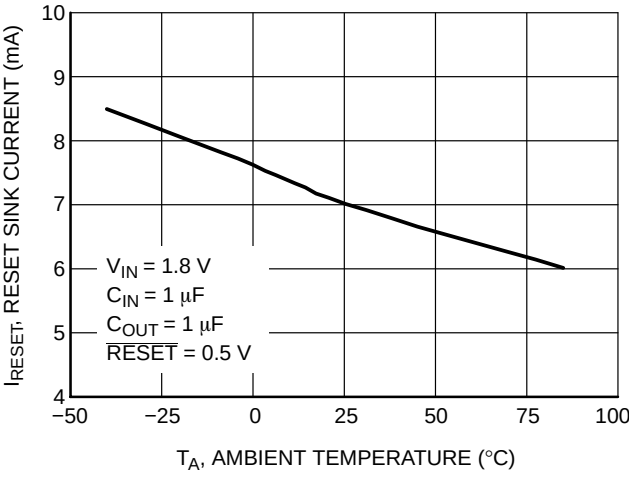


Figure 12. $\overline{\text{RESET}}$ Pin N−Channel Sink Current vs. Temperature

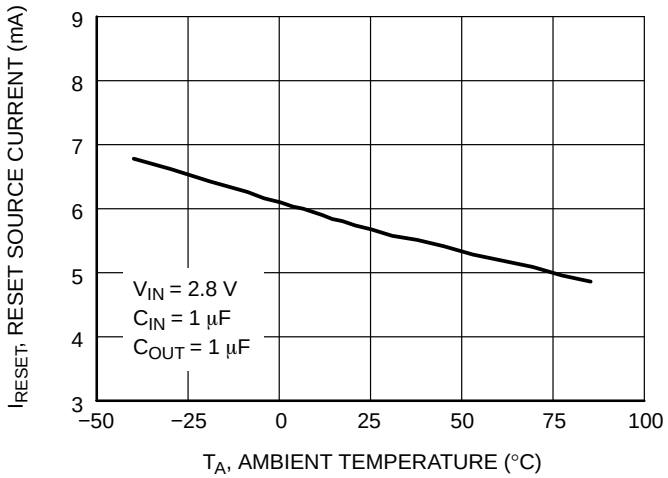


Figure 13. $\overline{\text{RESET}}$ Pin P−Channel Source Current vs. Temperature

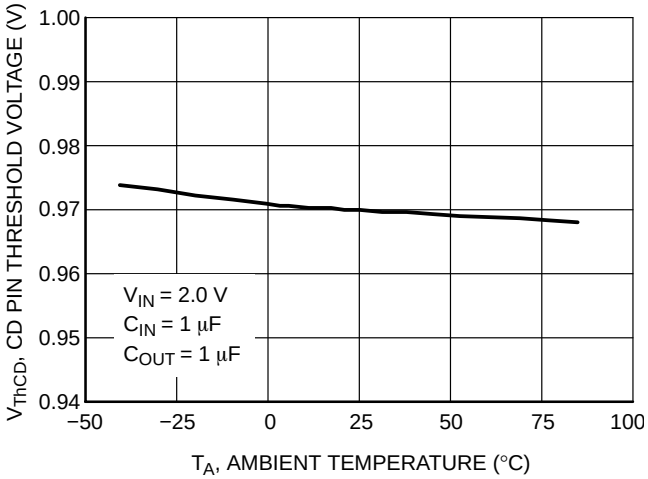


Figure 14. CD Delay Pin Threshold Voltage vs. Temperature

TYPICAL CHARACTERISTICS

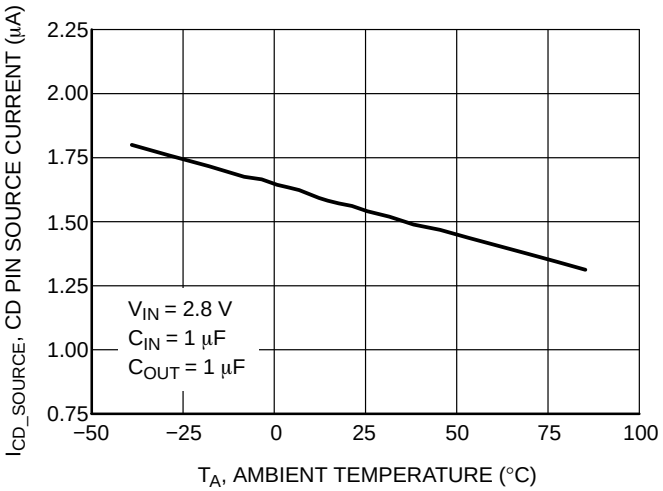


Figure 15. CD Pin Source Current vs. Temperature

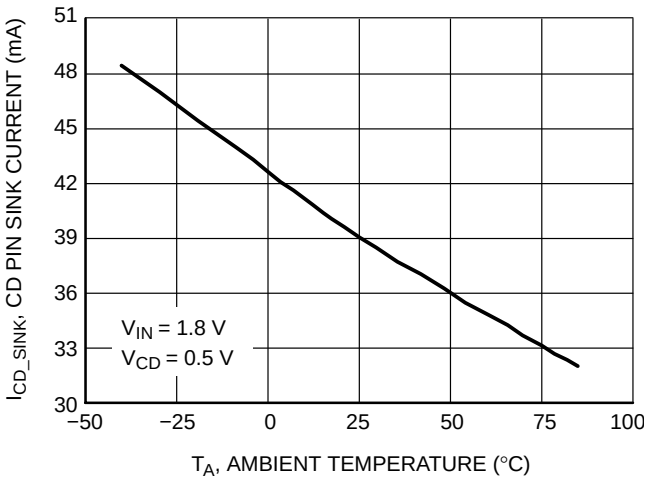


Figure 16. CD Pin Sink Current vs. Temperature

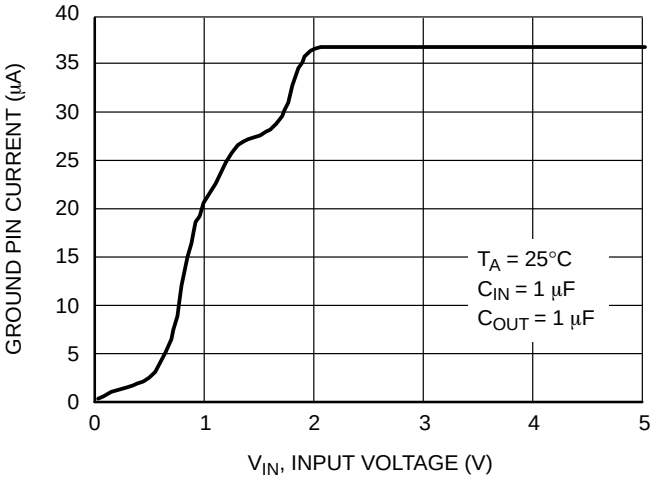


Figure 17. Ground Pin Current vs. Input Voltage

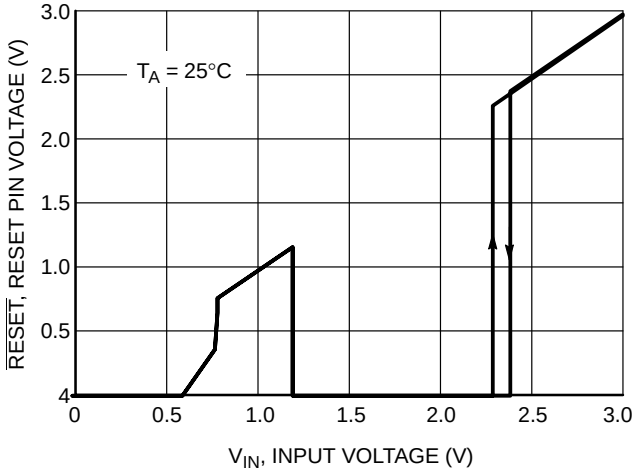


Figure 18. $\overline{\text{RESET}}$ Pin Voltage vs. Input Voltage

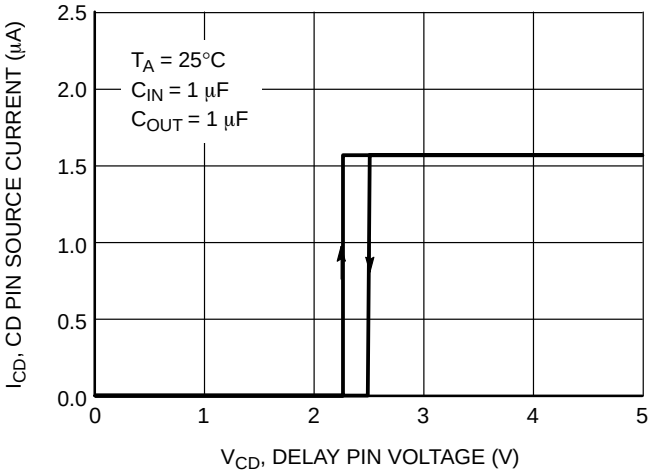


Figure 19. Delay Pin Source Current vs. Voltage

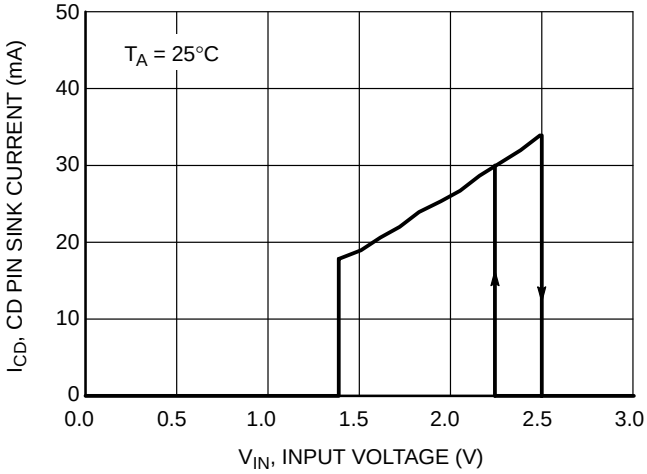


Figure 20. CD Pin Sink Current vs. Input Voltage

TYPICAL CHARACTERISTICS

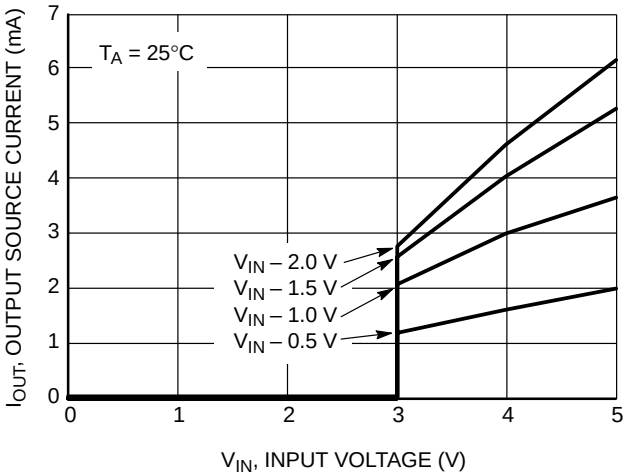


Figure 21. Reset Output Source Current vs. Input Voltage

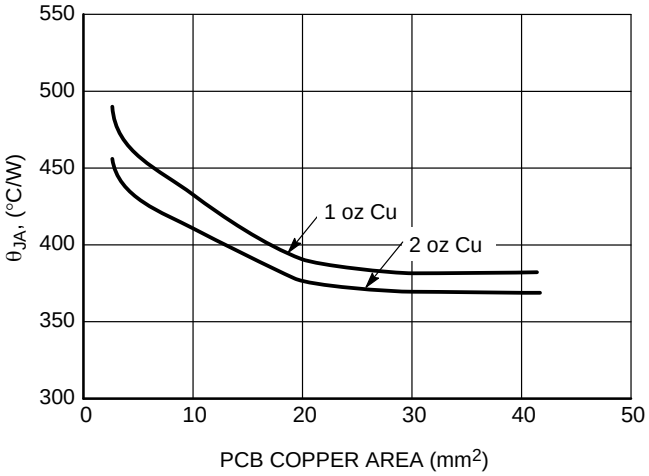


Figure 22. θ_{JA} vs. Copper Area

OPERATION DESCRIPTION

Low Dropout Voltage Regulator

The low dropout voltage regulator contains a voltage reference unit, an error amplifier, a PMOS power transistor, resistors for setting output voltage, current limit and thermal shutdown protection circuits.

Enable Operation

The enable pin will turn on or off the regulator. The limits of threshold are covered in the electrical specification section of this data sheet. If the enable is not used then the pin should be connected to V_{in}.

Voltage Detector

The NCP400 consist of a precision voltage detector that drives a time delay generator. Figures 23 and 24 show a timing diagram and a typical application. Initially consider that input voltage V_{in} is at a nominal level and it is greater than the voltage detector upper threshold (V_{DET+}). The voltage at CD Pin (Pin 4) will be at the same level as Vin, and the reset output (Pin 3) will be in the high state. If there is a power interruption and Vin becomes significantly deficient, it will fall below the lower detector threshold (V_{DET-}) and the external time delay capacitor CD will be immediately discharged by an internal N−Channel MOSFET that connects to Pin 4. This sequence of events causes the Reset output to be in the low state. After completion of the power interruption, V_{in} will again return to its nominal level and become greater than the V_{DET+}. The voltage detector will turn off the N−Channel MOSFET and allow internal current source to charge the external capacitor CD, thus creating a programmable delay for releasing the reset signal. When the voltage at CD Pin 4 exceeds the inverter threshold, typically 0.97 V, the reset output will revert back to its original state. The detail reset output time delay calculation is shown in Figure 24.

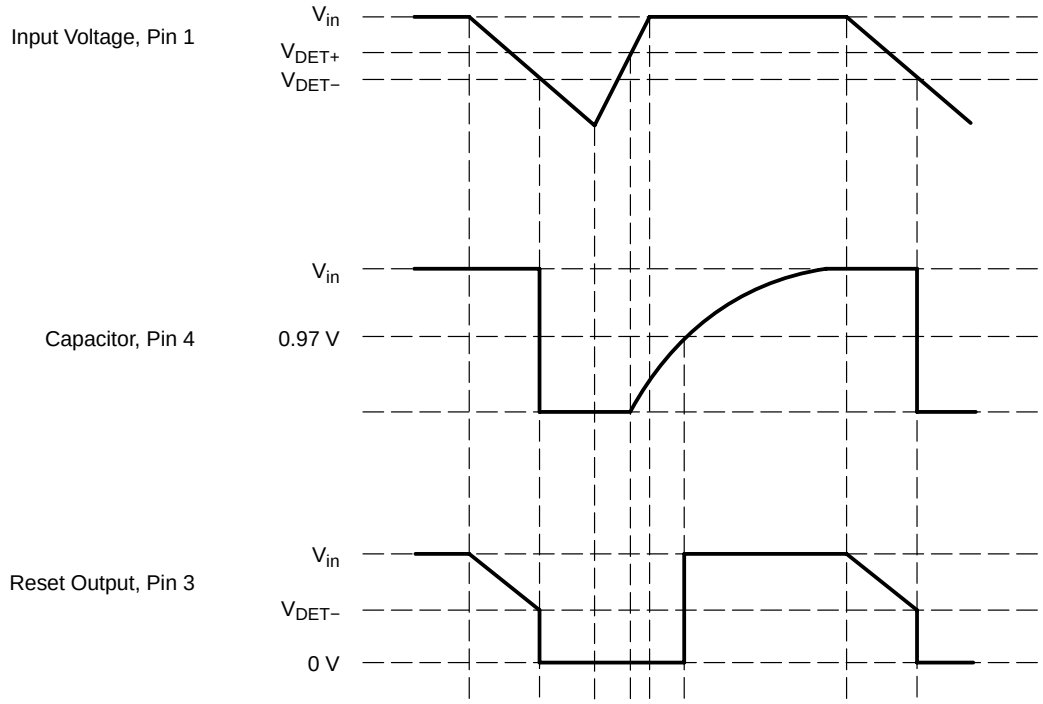


Figure 23. Timing diagram

APPLICATION NOTES

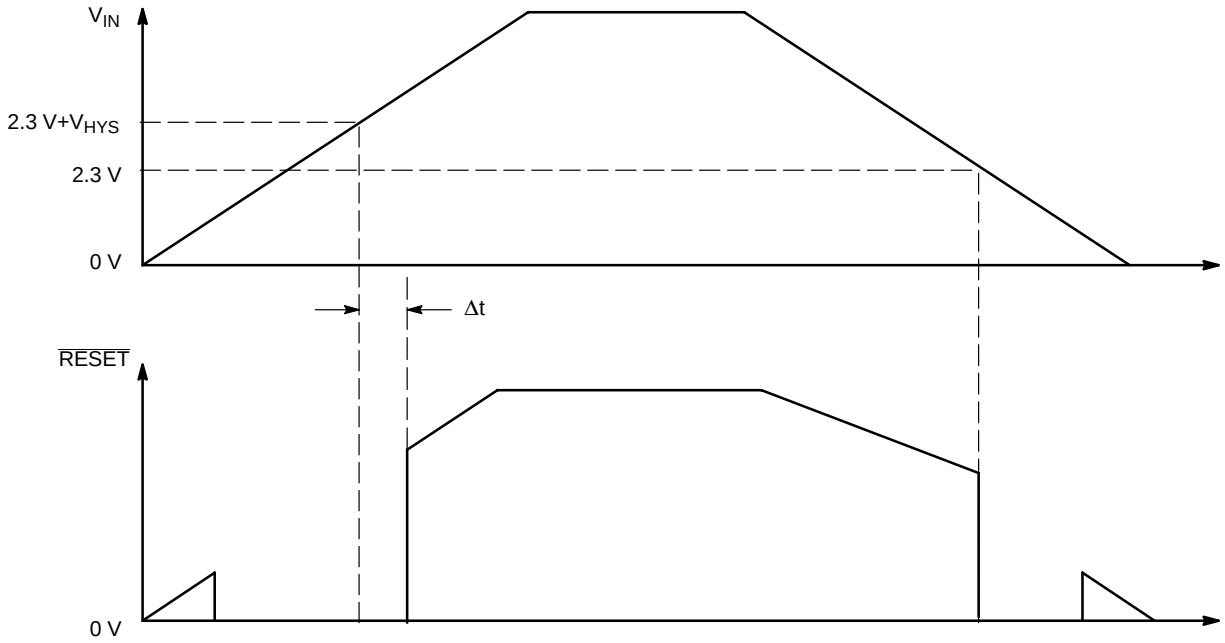


Figure 24. Timing Diagram

$$\text{Delay Time: } (\Delta t) = \frac{(C \times \Delta V_{ThCD})}{I_{CD}}$$

where: C is the CD pin capacitor
ΔV_{ThCD} is the delay threshold voltage
I_{CD} is delay current source.

As target use C = 3300 pF and have Δt = 2 ms:
With internal ΔV_{ThCD} = 0.97 V and I_{CD} =1.56 μA, then

$$\Rightarrow \text{Delay Time: } (\Delta t) = \frac{(3300\ \text{pF} \times 0.97\ \text{V})}{1.56\ \mu\text{A}} = 2.05\ \text{ms}$$

APPLICATION INFORMATION

Low Dropout Voltage Regulator

−Input Decoupling

A 1.0 μF capacitor either ceramic or tantalum is recommended and should be connected close to the NCP400 package. Higher values and lower ESR will improve the overall line transient response.

−Output Decoupling

The NCP400 is a stable Regulator and does not require any specific Equivalent Series Resistance (ESR) or a minimum output current. Capacitors exhibiting ESRs ranging from a few mΩ up to 10 Ω can thus safely be used. The minimum decoupling value is 1.0 μF and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load regulation transient response. Figure 25 shows the stable area of the regulator with different output capacitor ESR and output current.

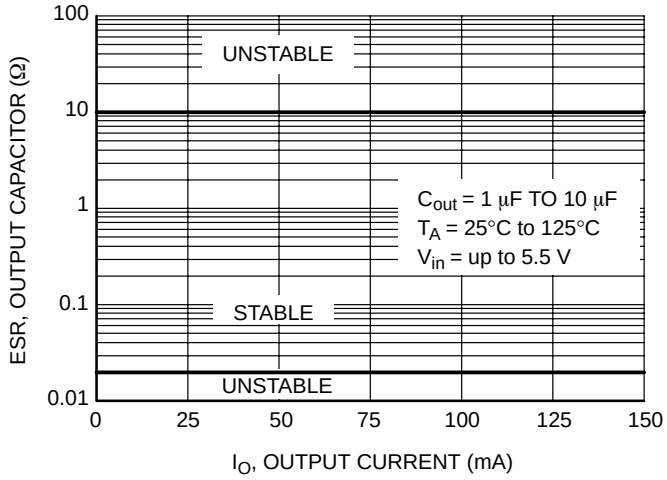


Figure 25. Output Capacitor versus Output Current

−Thermal Protection

Internal thermal shutdown circuit is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When the thermal protection activated, higher than 150°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

−Hints

Please be sure the Vin and GND lines are sufficiently wide. When the impedance of these lines is high, there is a chance to pick up noise or cause the regulator to malfunction. Set external components, especially the output capacitor, as close as possible to the circuit, and make leads a short as possible.

Voltage Detector

The voltage detector has built−in hysteresis to prevent erratic reset operation. This device is specifically designed for use as reset controllers in portable microprocessor based systems, it can offer a cost−effective solution in numerous applications where precise voltage monitoring and time delay are required. Figures 26 through 27 shows various application examples.

APPLICATION CIRCUIT INFORMATION

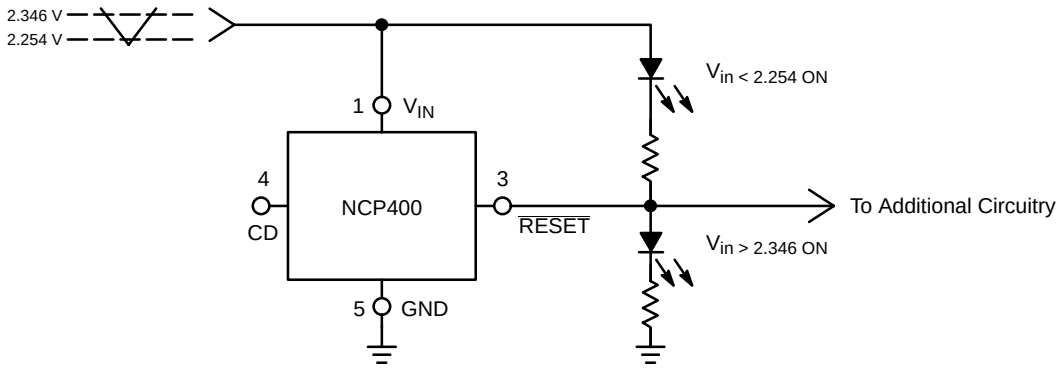
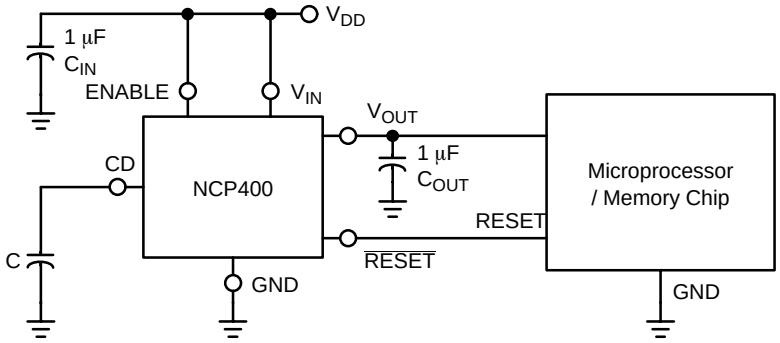


Figure 26. Input Voltage Indicator

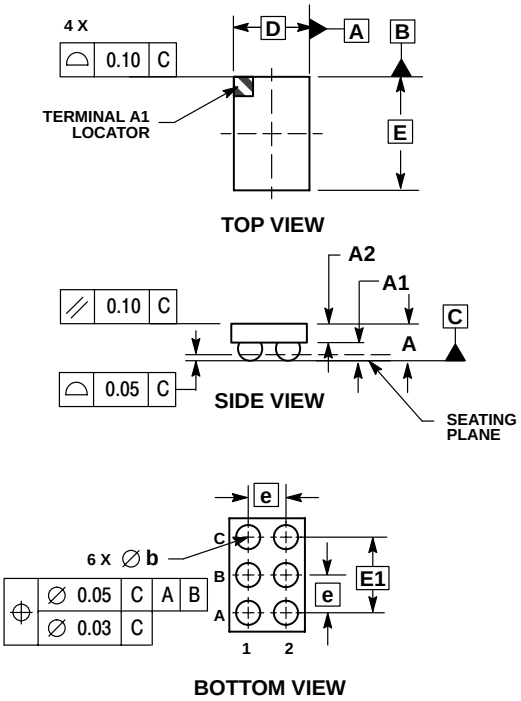


$$\text{DelayTime}: \ (\Delta t) = \frac{(C \times 0.97\ V)}{1.56\ \mu A}$$

Figure 27. Microprocessor Reset Circuit

PACKAGE DIMENSIONS

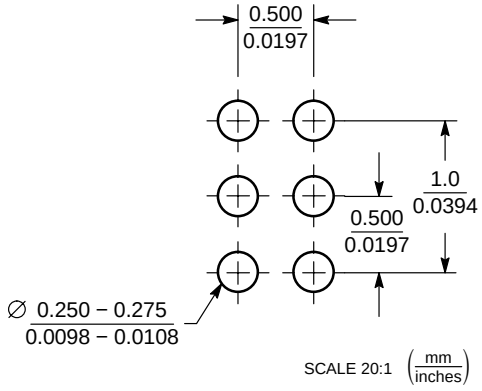
6 PIN FLIP−CHIP
CASE 499AH−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.448	0.533
A1	0.210	0.270
A2	0.238	0.263
D	1.000 BSC	
E	1.50 BSC	
b	0.290	0.340
e	0.500 BSC	
E1	1.000 BSC	

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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