D16450

Configurable UART

ver 2.07

OVERVIEW

The D16450 is a soft Core of a Universal Asynchronous Receiver/Transmitter (UART) functionally identical to the TL16C450. D16450 performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the UART, as well as any error conditions (parity, overrun, framing, or break interrupt). D16450 includes a programmable baud rate generator that is capable of dividing the timing reference clock input by divisors of 1 to (2^{16}-1), and producing a 16 × clock for driving the internal transmitter logic. Provisions are also included to use this 16 × clock to drive the receiver logic. The D16450 has complete MODEM control capability, and a processor-interrupt system. Interrupts can be programmed to the user's requirements, minimizing the computing required to handle the communications link.

The separate BAUD CLK line allows to set an exact transmission speed, while the UART internal logic is clocked with the CPU frequency

The core is perfect for applications, where the UART Core and microcontroller are clocked by the same clock signal and are implemented inside the same ASIC or FPGA chip, as well as for standalone implementation, where several UARTs are required to be implemented inside a single chip, and driven by some off-chip devices. Thanks to universal interface D16450 core implementation and verification are very simply, by eliminating a number of clock trees in complete system.

KEY FEATURES

- Software compatible with 16450 UART
- **Configuration capability**
- **Separate configurable BAUD clock line**
- Majority Voting Logic
- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from the serial data
- In UART mode receiver and transmitter are double buffered to eliminate a need for precise synchronization between the CPU and serial data
- Independently controlled transmit, receive, line status, and data set interrupts
- False start bit detection
- 16 bit programmable baud generator
- MODEM control functions (CTS, RTS, DSR, DTR, RI, and DCD)

http://www.DigitalCoreDesign.com
http://www.dcd.pl

- Fully programmable serial-interface characteristics:
  - *5-, 6-, 7-, or 8-bit characters*
  - *Even, odd, or no-parity bit generation and detection*
  - *1-, 1½-, or 2-stop bit generation*
  - *Baud generation*
- Complete status reporting capabilities
- Line break generation and detection. Internal diagnostic capabilities:
  - *Loop-back controls for communications link fault isolation*
  - *Break, parity, overrun, framing error simulation*
- Technology independent HDL Source Code
- Full prioritized interrupt system controls
- Fully synthesizable static design with no internal tri-state buffers

APPLICATIONS

- Serial Data communications applications
- Modem interface

DELIVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted, or plain text EDIF netlist
- VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery the IP Core updates, minor and major versions changes
    - Delivery the documentation updates
    - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods without royalty fees make using of IP Core easy and simply.

Single Design license allows use IP Core in single FPGA bitstream and ASIC implementation.

Unlimited Designs, *One Year* licenses allow use IP Core in unlimited number of FPGA bitstreams and ASIC implementations.

In all cases number of IP Core instantiations within a design, and number of manufactured chips are unlimited. There is no time restriction except *One Year* license where time of use is limited to 12 months.

- Single Design license for
  - *VHDL, Verilog source code called HDL Source*
  - *Encrypted, or plain text EDIF called Netlist*
- One Year license for
  - *Encrypted Netlist only*
- Unlimited Designs license for
  - *HDL Source*
  - *Netlist*
- Upgrade from

- *HDL Source to Netlist*
- *Single Design to Unlimited Designs*

CONFIGURATION

The following parameters of the D16450 core can be easy adjusted to requirements of dedicated application and technology. Configuration of the core can be prepared by effortless changing appropriate constants in package file. There is no need to change any parts of the code.

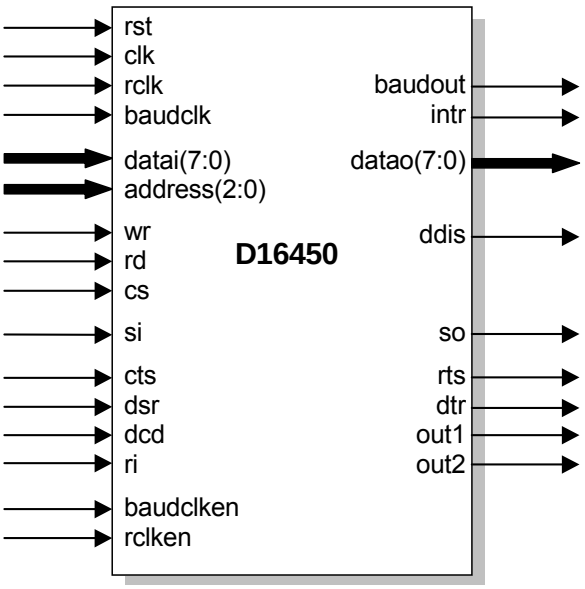
• Baud generator	- enable - disable
• External RCLK source	- enable - disable
• External BAUDCLK source	- enable - disable
• Modem Control logic	- enable - disable
• SCR Register	- enable - disable

DESIGN FEATURES

The functionality of the D16450 core was based on the Texas Instruments TL16C450. The following characteristics differentiate the D16450 from Texas Instruments devices:

- The bi-directional data bus has been split into two separate buses: datai(7:0), datao(7:0)
- Signals rd2 and wr2, xin, and xout have been removed from interface
- Signal ADS and address latch have been removed
- The DLL, DLM and THR registers are reset to all zeros
- TEMT and THRE bits of Line Status Register, are reset during the second clock rising edge following a THR write
- RCLK clock is replaced by global clock CLK, internally divided by BAUD factor.
- Asynchronous microcontroller interface is replaced by equivalent Universal interface
- All latches implemented in original 16450 devices are replaced by equivalent flip-flop registers, with the same functionality

SYMBOL

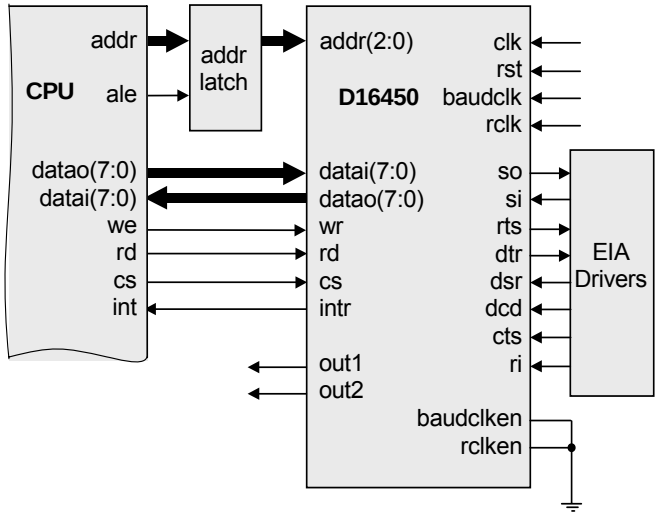


PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
rst	input	Global reset
clk	input	Global clock
datai[7:0]	input	Parallel data input
addr[2:0]	input	Address bus
cs	input	Chip select input
wr	input	Write input
rd	input	Read input
rclk	input	Receiver clock
baudclk	input	Baud generator clock
si	input	Serial data input
cts	input	Clear to send input
dsr	input	Data set ready input
dcd	input	Data carrier detect input
ri	input	Ring indicator input
baudclken	input	Baud generator clock enable
rclken	input	Receiver clock enable
baudout	output	Baud generator output
datao[7:0]	output	Parallel data output
so	output	Serial data output
ddis	output	Driver disable output
rts	output	Request to send output
dtr	output	Data terminal ready output
out1	output	Output 1
out2	output	Output 2
intr	output	Interrupt request output

Note: When enabled RCLK and BAUDCLK pins frequency should be at least two times lower than CLK, $2*f_{RCLK} < f_{CLK}$

APPLICATION



Typical D16450 and processor connection is shown in figure above.

BLOCK DIAGRAM

Data Bus Buffer - The data Bus Buffer accepts inputs from the system bus and generates control signals for the other D14750 functional blocks. Address bus ADDR(2:0) selects one of the register to be read from/written into. Both RD and WE signals are active low, and are qualified by CS; RD and WE are ignored unless the D16450 has been selected by holding CS low.

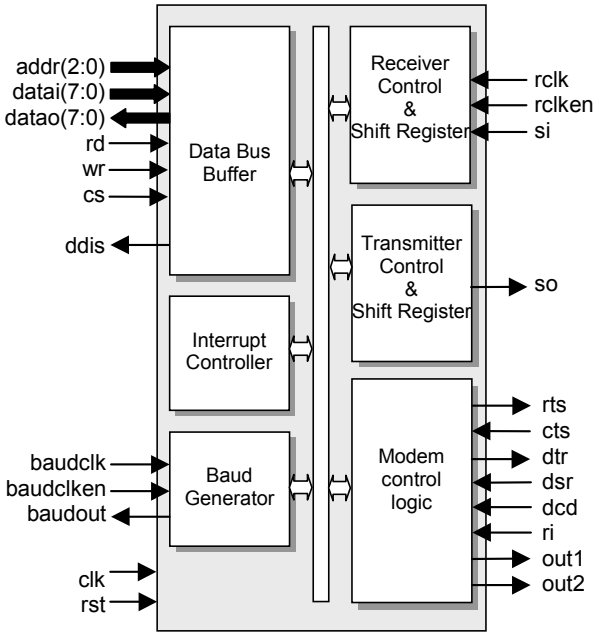
Baud Generator - The D16450 contains a programmable 16 bit baud generator that divides clock input by a divisor in the range between 1 and (2^{16}–1). The output frequency of the baud generator is 16× the baud rate. The formula for the divisor is:

$$divisor = \frac{frequency}{baudrate * 16}$$

Two 8-bit registers, called divisor latches DLL and DLM, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the D16450 in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded on the CLK rising edge following the write to DLL or DLM to prevent long counts on initial load.

Modem Control Logic controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM).

Interrupt Controller - D16450 consists fully prioritized interrupt system controller. It controls interrupt requests to the CPU and interrupt priority. Interrupt controller contains Interrupt Enable (IER) and Interrupt Identification (IIR) registers.



Receiver Control - Receiving starts when the falling edge on Serial Input (SI) during IDLE State is detected. After starting the SI input is sampled every 16 internal baud cycles as it is shown in figure below. When the logic 1 state is detected during START bit it means that the False Start bit was detected and receiver back to the IDLE state.

Transmitter Control module controls transmission of written to THR (Transmitter Holding register) character via serial output SO. The new transmission starts on the next overflow signal of internal baud generator, after writing to THR register or Transmitter FIFO. Transmission control contains THR register and transmitter shift register.

PERFORMANCE

The following table gives a survey about the Core area and performance in the ALTERA® devices after Place & Route:

Device	Speed grade	Logic Cells	F_{max}
CYCLONE	-6	301	190 MHz
CYCLONE 2	-6	303	222 MHz
STRATIX	-5	301	213 MHz
STRATIX 2	-3	248	283 MHz
STRATIXGX	-5	301	212 MHz
MERCURY	-5	350	222 MHz
EXCALIBUR	-1	340	137 MHz
APEX II	-7	340	145 MHz
APEX20KC	-7	340	143 MHz
APEX20KE	-1	340	122 MHz
APEX20K	-1	340	83 MHz
ACEX1K	-1	363	99 MHz
FLEX10KE	-1	363	98 MHz

Core performance in ALTERA® devices

D16X50 UARTS FAMILY OVERVIEW

The family of DCD D16X50 UART IP Cores combine a high–performance, low cost, and small compact size, offering the best price/performance ratio in the IP Market. The DCD's Cores are dedicated for use in cost-sensitive consumer products, computer peripherals, office automation, automotive control systems, security and telecommunication applications.

The D16X50 IP Cores are written in pure VHDL/VERILOG HDL languages which make them technologically independent. All of the D16X50 IP Cores can be fully customized according to customer needs.

Design	UARTS number	UART Mode	FIFO Mode of operation	FIFO Size (Bytes)	Majority voting logic	Separate BAUD Clock line	Software Flow Control	RTS/CTS Flow Control	MODEM Control	False START Bit detection	Complete status reporting	Internal diagnostic capabilities	Prioritized interrupt system	Break generation and detection	IRDA Port	1284 Parallel Port
D16450	1	✓	-	-	✓	✓	-	-	✓	✓	✓	✓	✓	✓	-*	-*
D16550	1	✓	✓	2* 16	✓	✓	-	-	✓	✓	✓	✓	✓	✓	-*	-*
D16750	1	✓	✓	2* 64	✓	✓	-	✓	✓	✓	✓	✓	✓	✓	-*	-*
D16552	2	✓	✓	4* 16	✓	✓	-	-	✓	✓	✓	✓	✓	✓	✓	✓
D16752	2	✓	✓	4* 64	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	-*	-*
D16754	4	✓	✓	8* 64	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	-*	-*

**-Optional*

D16X50 family of Configurable UARTs with FIFO IP Cores

CONTACTS

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