XC612 Series

2 Channel Voltage Detectors

TOREX

- ◆CMOS Low Power Consumption
- ◆2 Voltage Detectors Built-in
- ◆Detect Voltage Accuracy : ± 2%
- ◆Detect Voltage Range : 1.5V ~ 5.0V
- ◆SOT-25 Package

■Applications

- ●Memory battery back-up circuitry
- ●Microprocessor reset circuits
- ●Power failure detection
- ●System power-on reset circuits
- ●System battery life monitors and re-charge voltage monitors
- ●Delay circuitry

■General Description

The XC612 series consist of 2 voltage detectors, in 1 mini-molded, SOT-25 package.

The series provides accuracy and low power consumption through CMOS processing and laser trimming and consists of a highly accurate voltage reference source, 2 comparators, hysteresis and output driver circuits.

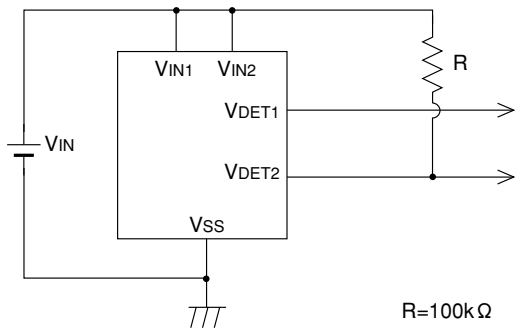
The input (V_{IN1}) for voltage detector 1 (V_{D1}) dually functions as the power supply pin for both detector 1 (V_{D1}) and detector 2 (V_{D2}).

■Features

Highly accurate	: Set-up voltage accuracy ±2%
Low-power consumption	: Typ.2.0μA (V_{IN1}=V_{IN2}=2.0V, quiescent state)
Detect voltage	: 1.5V ~ 5.0V programmable in 0.1V steps. Detector's voltages can be set-up independently Conditionaly, XC612N : V_{DET1}>V_{DET2} XC612D, XC612E : V_{DET1}≥V_{DET2}, V_{DET1}<V_{DET2}
Operating Voltage Range	: 1.0V ~ 10.0V
Temperature characteristics	: ±100ppm/°C
Output configuration	: N-channel open drain
Small package	: SOT-25 (150mW) mini-mold

*** CMOS Output is under development**

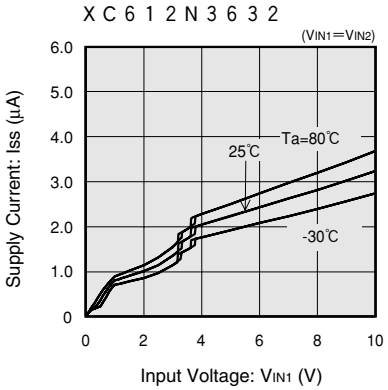
■Typical Application Circuit



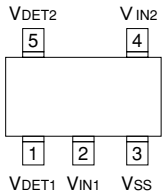
V_{DET1} : CMOS, V_{DET2} : N-ch Open drain

■Typical Performance Characteristic

SUPPLY CURRENT vs. INPUT VOLTAGE



■Pin Configuration



SOT-25
(TOP VIEW)

■Pin Assignment

PIN NUMBER	PIN NAME	FUNCTION
1	V_{DET1}	Voltage Detector 1 output
2	V_{IN1}	Detector 1 input, Power Supply.
3	V_{SS}	Ground
4	V_{IN2}	Voltage Detector 2 Input
5	V_{DET2}	Voltage Detector 2 Output

■Product Classification

●Selection Guide

Type	V_{DET1}	V_{DET2}
XC612N	N-ch Open drain	N-ch Open drain
XC612D	N-ch Open drain	CMOS
XC612E	CMOS	N-ch Open drain

●Ordering Information

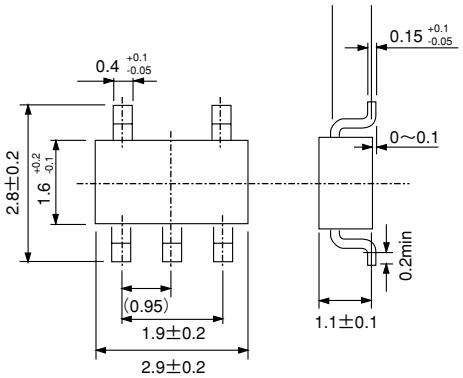
XC612 x x x x x x

a b c d e

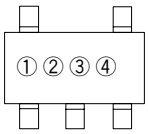
DESIGNATOR	DESCRIPTION	DESIGNATOR	DESCRIPTION
a	Output Configuration: N=N-Channel Open Drain D=V_{DET1} N-ch Open Drain, V_{DET2} CMOS E=V_{DET1} CMOS, V_{DET2} N-ch Open Drain	d	Package Type: M=SOT-25
b	Detect Voltage (V_{DET1}) e.g.25=2.5V 38=3.8V	e	Device Orientation R=Embossed Tape (Orientation of Device: Right) L=Embossed Tape (Orientation of Device: Left)
c	Detect Voltage (V_{DET2}) e.g.33=3.3V 50=5.0V		

■Packaging Information

●SOT-25



■Marking



SOT-25
(TOP VIEW)

① Represents the output configuration

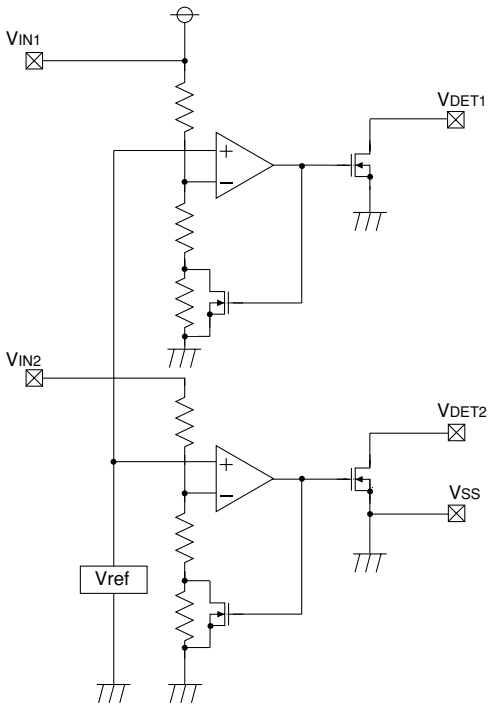
DESIGNATOR	CONFIGURATION		PRODUCT NAME
	V_{DET1}	V_{DET2}	
N	N-ch Open drain	N-ch Open drain	XC612N****M*
D	N-ch Open drain	CMOS	XC612D****M*
E	CMOS	N-ch Open drain	XC612E****M*

②③ Represents the entry order.

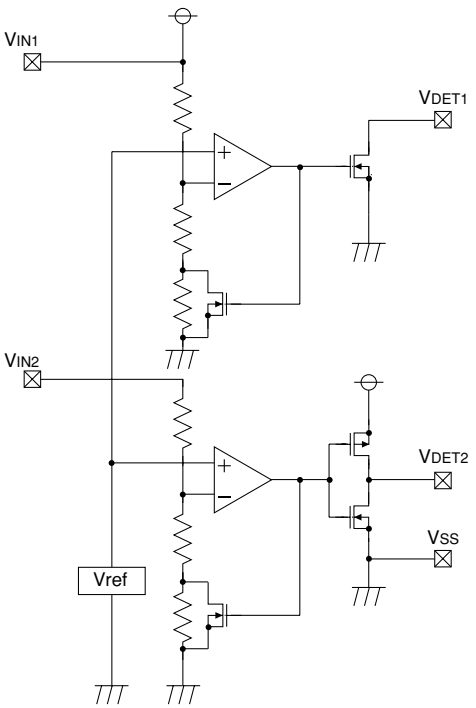
④ Denotes the production lot number
0 to 9, A to Z repeated. (G.I.J.O.Q.W excepted)

■Block Diagram

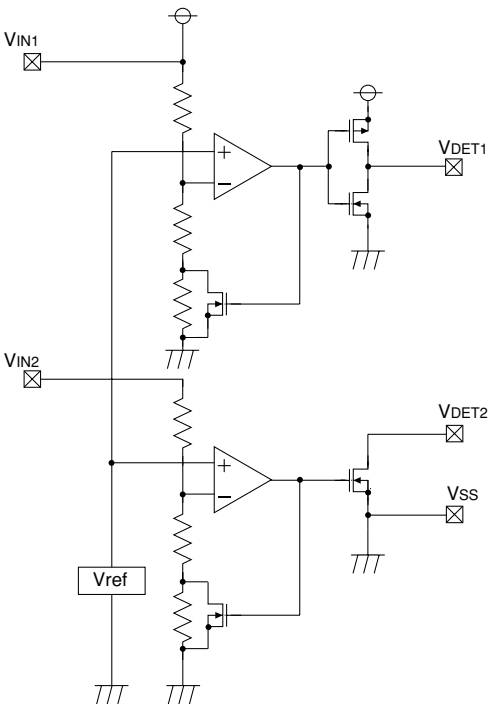
XC612N Series



XC612D Series



XC612E Series



■Absolute Maximum Ratings

Ta=25℃

PARAMETER	SYMBOL	CONDITIONS	UNITS
Input Voltage V_{IN1}	V_{IN1}	12	V
Input Voltage V_{IN2}	V_{IN2}	12	V
Output Voltage V_{DET1}(N-ch Open drain)	V_{VDET1}	V_{SS}−0.3～12	V
Output Voltage V_{DET1}(CMOS)	V_{VDET1}	V_{SS}−0.3～V_{IN1}+0.3	V
Output Current V_{DET1}	I_{VDET1}	50	mA
Output Voltage V_{DET2}(N-ch Open drain)	V_{VDET2}	V_{SS}−0.3～12	V
Output Voltage V_{DET2}(CMOS)	V_{VDET2}	V_{SS}−0.3～V_{IN1}+0.3	V
Output Current V_{DET2}	I_{VDET2}	50	mA
Power Dissipation	Pd	150	mW
Operating Ambient Temperature	Topr	−30～+80	℃
Storage Temperature	Tstg	−40～+125	℃

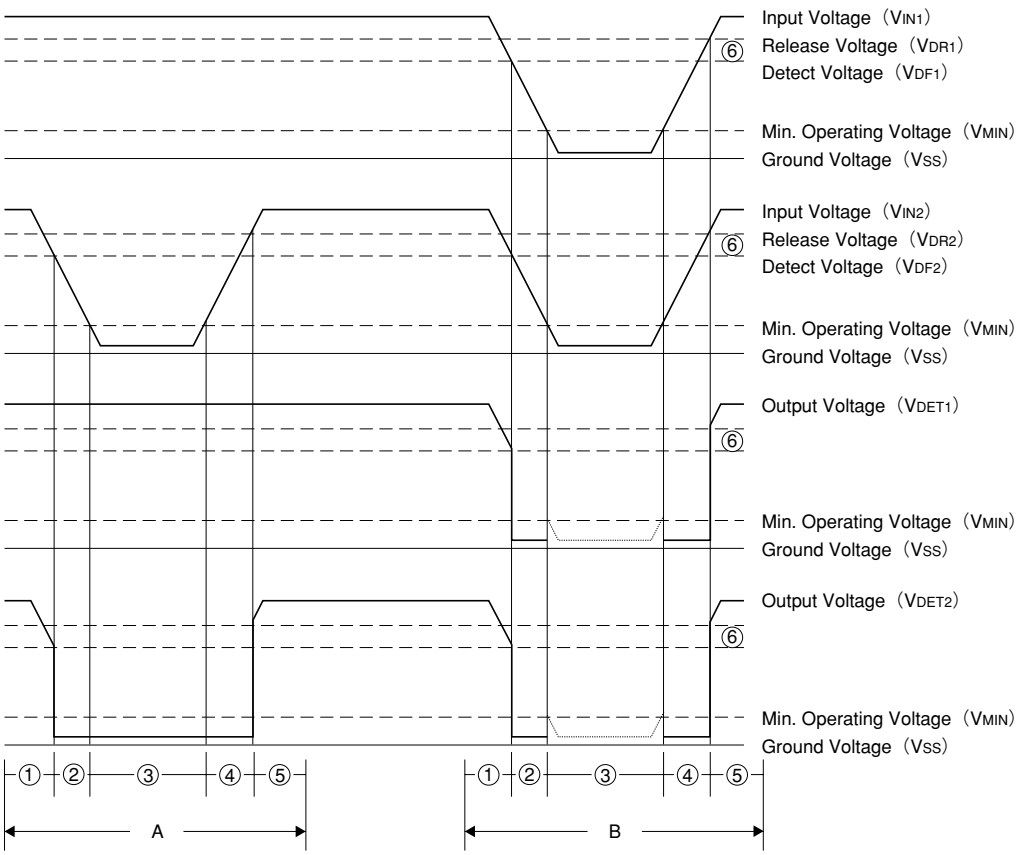
■Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	CIRCUIT
Detect Voltage V_{DET1}	V_{DF1}	Voltage when V_{DET1} changes from H to L following a reduction of V_{IN1}	V_{DF1} x 0.98	V_{DF1}	V_{DF1} x 1.02	V	1
Detect Voltage V_{DET2}	V_{DF2}	Voltage when V_{DET2} changes from H to L following a reduction of V_{IN2}	V_{DF2} x 0.98	V_{DF2}	V_{DF1} x 1.02	V	1
Hysteresis Range 1	V_{HYS1}	Voltage (V_{DR1}) - V_{DF1} when V_{DET1} changes from L to H following an increase of V_{IN1}	V_{DF1}(T) x 0.02	V_{DF1}(T) x 0.05	V_{DF1}(T) x 0.08	V	1
Hysteresis Range 2	V_{HYS2}	Voltage (V_{DR2}) - V_{DF2} when V_{DET2} changes from L to H following an increase of V_{IN2}	V_{DF2}(T) x 0.02	V_{DF}2(T) x 0.05	V_{DF2}(T) x 0.08		1
Supply Current (Input Current V_{IN1})	I_{SS}	V_{IN1}=1.5V 2.0V 3.0V 4.0V 5.0V		1.35 1.50 1.95 2.40 3.00	3.90 4.50 5.10 5.70 6.30	µA	2
Input Current V_{IN2}	I_{IN2}	V_{IN1}=1.5V 2.0V 3.0V 4.0V 5.0V		0.45 0.50 0.65 0.80 1.00	1.30 1.50 1.70 1.90 2.10	µA	2
Operating Voltage	V_{IN1}	V_{DF} (T) = 1.5V to 6.0V	1.5		10	V	–
Output Current*	I_{VDET}	N-ch V_{DS} = 0.5V V_{IN1}=1.0V V_{IN1}=2.0V V_{IN1}=3.0V V_{IN1}=4.0V V_{IN1}=5.0V P-ch V_{DS} = -2.1V V_{IN1}=8.0V (CMOS)	 0.3 3.0 5.0 6.0 7.0 	 2.2 7.7 10.1 11.5 13.0 -10.0	 -2.0	mA	3
Temperature Characteristics*	$\frac{\Delta V_{DF}}{\Delta Topr \cdot V_{DF}}$	–30℃ ≤ Topr ≤ 80℃		±100	–	ppm/℃	–
Transient Delay Time* (Release Voltage→ Output Conversion)	tDLY	(V_{DR}→V_{OUT} conversion)			0.2	ms	5

1. V_{DF1}(T), V_{DF2}(T) : User specified detect voltage.
2. Release voltage (V_{DR}) = V_{DF} +V_{HYS}
3. Those parameters marked with an asterisk apply to both V_{DET1} and V_{DET2}.
4. Input Voltage : please ensure that V_{IN1} > V_{IN2}
   (Input voltage of XC612D and XC612E series : please ensure that V_{IN1} ≥ V_{IN2}, V_{IN1}< V_{IN2}.)
5. V_{IN1} pin serve both I_{SS} and power supply pin so that V_{IN2} operates V_{IN1} as a power supply source. For normal operation of V_{IN2}, operating voltage higher than the minimum is needed to be applied to power supply pin V_{IN1}.
6. For CMOS output products, high level output voltage which is generated when the transient response is released becomes input voltage of V_{IN}.

■Operating Explanation

●Timing Chart (Pull up voltage =Input voltage V_{IN1})



●Operational Notes (N-ch Open drain)

Timing Chart A (V_{IN1}=voltages above release voltage, V_{IN2}=sweep voltage)

Because a voltage higher than the minimum operating voltage is applied to the voltage input pin (V_{IN}), ground voltage will be output at the output pin (V_{DET}) during stage 3. (Stages 1, 2, 4, 5 are the same as in B below).

Timing Chart B (V_{IN1}=V_{IN2})

① When a voltage greater than the release voltage (V_{DR}) is applied to the voltage input pin (V_{IN1}, V_{IN2}), input voltage (V_{IN1}, V_{IN2}) will gradually fall.
When a voltage greater than the detect voltage (V_{DF}) is applied to the voltage input pin (V_{IN1}, V_{IN2}), a state of high impedance will exist at the output pin (V_{DET1}, V_{DET2}), so should the pin be pulled up, voltage will be equal to pull up voltage.

② When input voltage (V_{IN1}, V_{IN2}) falls below detect voltage (V_{DF}), output voltage (V_{DET1}, V_{DET2}) will be equal to ground level (V_{SS}).

③ Should input voltage (V_{IN1}, V_{IN2}) fall below the minimum operational voltage (V_{MIN}), output will become unstable. Should V_{IN2} fall below V_{MIN}, voltage at the output pin (V_{DET2}) will be equal to ground level (V_{SS}) if the power supply (V_{IN1}) is within the operating voltage range.
*In general the output pin is pulled up so output will be equal to pull up voltage.

④ Should input voltage (V_{IN1}, V_{IN2}) rise above ground voltage (V_{SS}), output voltage (V_{DET1}, V_{DET2}) will equal ground level until the release voltage level (V_{DR}) is reached.

⑤ When input voltage (V_{IN1}, V_{IN2}) rises above release voltage, the output pin's (V_{DET1}, V_{DET2}) voltage will be equal to the voltage dependent on pull up.

Note : The difference between release voltage (V_{DR}) and detect voltage (V_{DF}) is the Hysteresis Range ⑥.

■Directions for use

●Notes on Use

1. Please use this IC within the specified maximum absolute ratings.
2. Please ensure that input voltage V_{IN2} is less than V_{IN1} + 0.3V. (refer to N.B. 1 below)
3. With a resistor connected between the V_{IN1} pin and the input, oscillation is liable to occur as a result of through current at the time of release. (refer to N.B. 2 below)
4. With a resistor connected between the V_{IN1} pin and the input, detect and release voltage will rise as a result of the IC's supply current flowing through the V_{IN1} pin.
5. In order to stabilise the IC's operations, please ensure that the V_{IN1} pin's input frequency's rise and fall times are more than 5 μ sec/V.
6. Should the power supply voltage V_{IN1} exceed 6V, voltage detector 2's detect voltage (V_{DF2}) and the release voltage (V_{DR2}) will shift somewhat.
7. For CMOS output products, high level output voltage which is generated when the transient response is released becomes input voltage of V_{IN}.

●N.B.

1. Voltage detector 2's input voltage (V_{IN2})
   An input protect diode is connected from input detector 2's input (V_{IN2}) to input detector 1's input. Therefore, should the voltage applied to V_{IN2} exceed V_{IN1}, current will flow through V_{IN1} via the diode. (refer to diagram1)
2. Oscillation as a result of through current
   Since the XC612 series are CMOS ICs, through current will flow when the IC's internal circuit switching operates (during release and detect operations). Consequently, oscillation is liable to occur as a result of drops in voltage at the through current's resistor (R_{IN}) during release voltage operations. (refer to diagram 2)
   Since hysteresis exists during detect operations, oscillation is unlikely to occur.

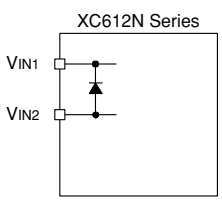


Diagram 1. Voltage detector 2's input voltage V_{IN2}

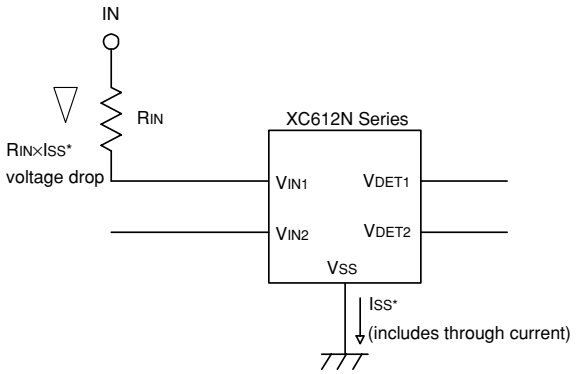
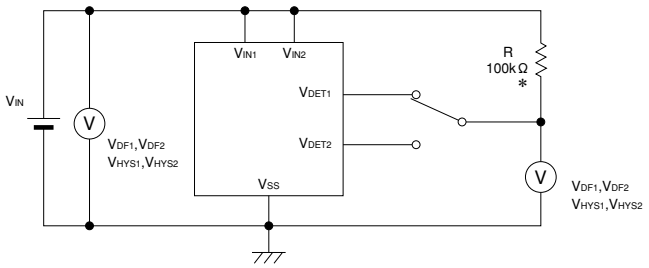


Diagram 2. Through current oscillation

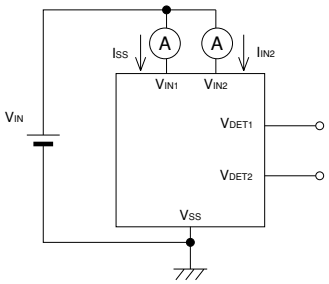
■Test Circuits

Circuit 1.



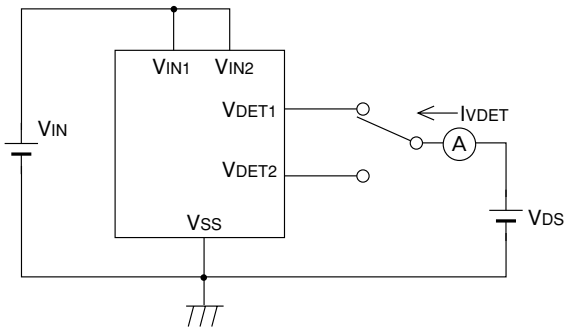
* A resistor is not needed if the product is CMOS output type.

Circuit 2.

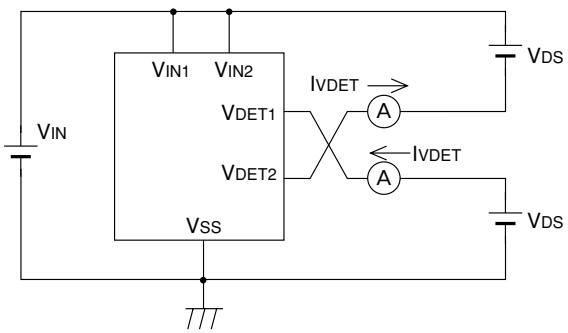


Circuit 3.

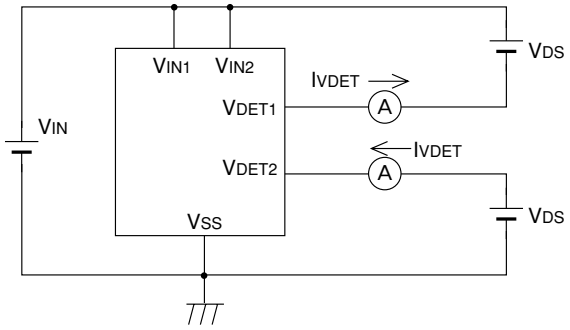
XC612N Series



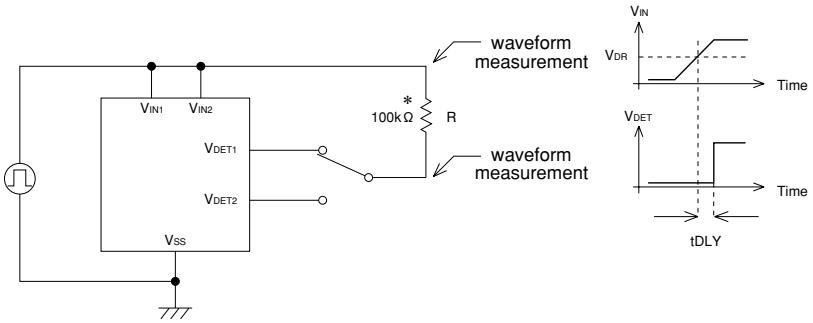
XC612D Series



XC612E Series

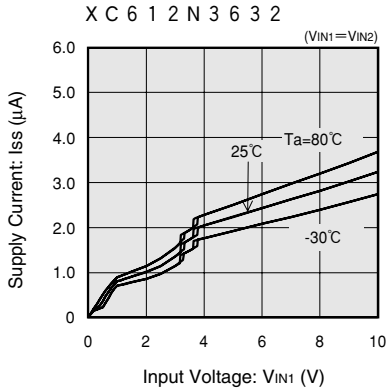


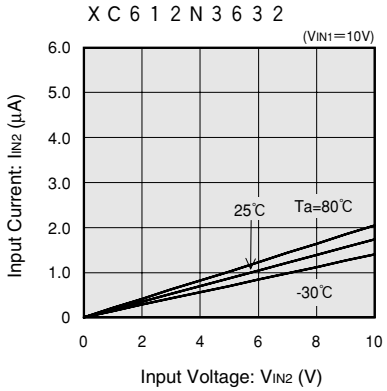
Circuit 4.



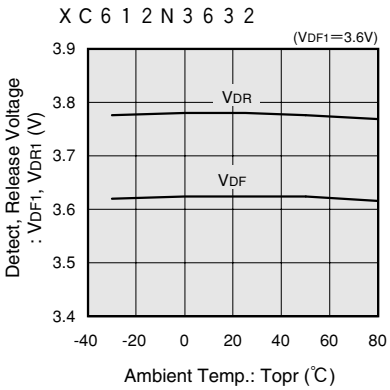
■Typical Performance Characteristics

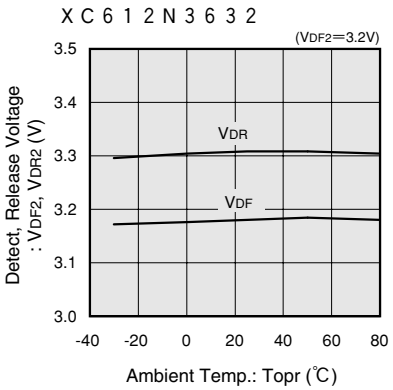
(1) SUPPLY CURRENT vs. INPUT VOLTAGE





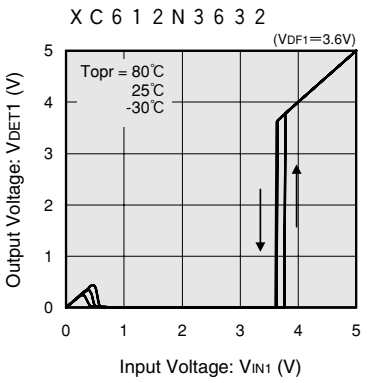
(2) DETECT & RELEASE VOLTAGE vs. AMBIENT TEMPERATURE

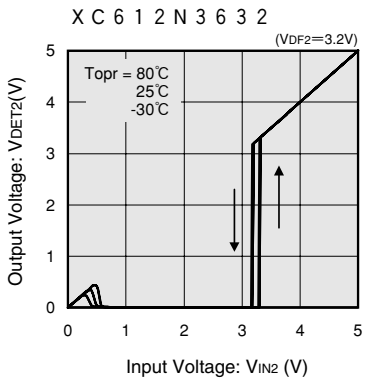




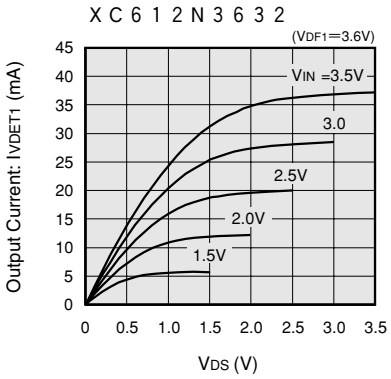
Note : Unless otherwise stated, pull up resistance = 100kΩ with N-ch open drain output types.

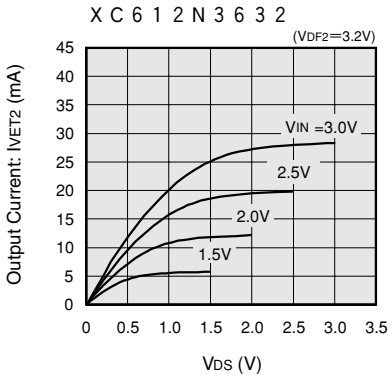
(3) OUTPUT VOLTAGE vs. INPUT VOLTAGE

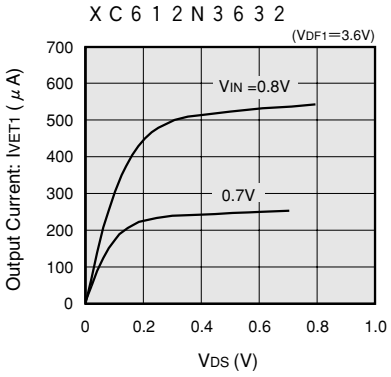


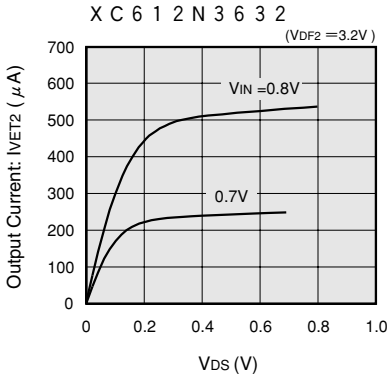


(4) N-CH DRIVER OUTPUT CURRENT vs. VDS

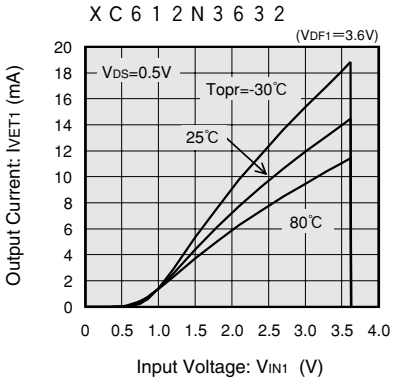


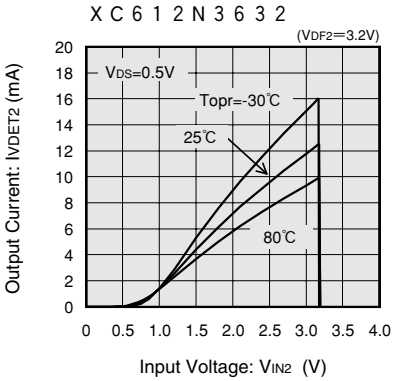






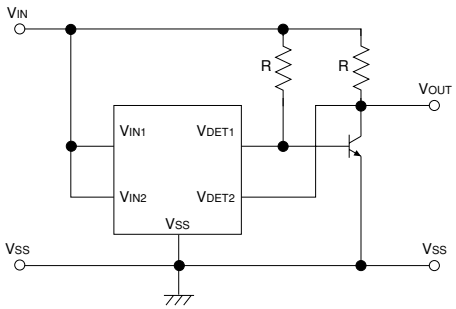
(5) N-CH DRIVER OUTPUT CURRENT vs. INPUT VOLTAGE

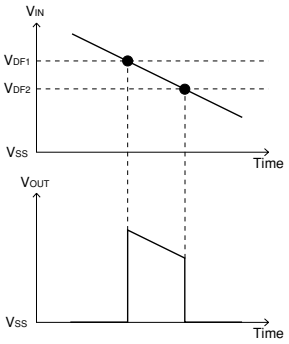




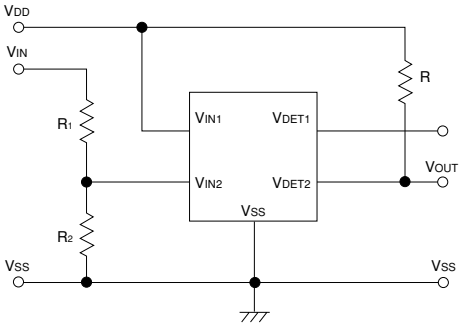
■Typical Application Circuits

●Window comparator circuit (Example covers N-channel open drain product's circuits.)





●Detect voltages above respective established voltages circuit (Example covers N-channel open drain product's circuits.)



Notes on resistors R1 and R2's (1), (2) functions :

Detect voltage = { (R1 + R2) ÷ R2} × V_{DF2} (1)

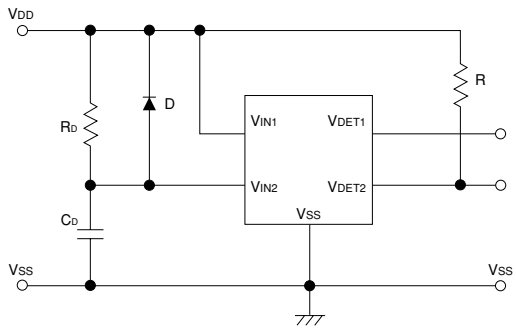
N.B. V_{DF2} = detect voltage VD2

Please set-up so that

Hysteresis (V_{HYS2}) = { (R1 + R2) ÷ } × V_{HYS2} (2)

Note : Please ensure that input voltage 2 (V_{IN2}) is less than V_{IN1} + 0.3V

●Voltage detect circuit with delay built-in (Example covers N-channel open drain product's circuits.)



Note : Delay operates at both times of release and detect operations.