



ISO²-CMOS MT35212A BELL 212A/CCITT V.22 Modem Filter

9161-002-038-NA

ISSUE 3

November 1990

Features

- Bell 212A and CCITT V.22 compatible
- Usable for Bell 103 and V.22 Bis Applications
- Guard tone notch filters for V.22 Applications
- High and low bandfilters with compromise group delay equalizers and smoothing filters
- Answer/originate operating modes
- Detection of call progress tones
- Choice of clocking frequencies: 2.4576 MHz, 1.2288 MHz, or 153.6 kHz
- Analog loopback test capability
- Two uncommitted operational amplifiers
- Pin compatible with AMI S35212A

Applications

- Modem filter/equalizer for 1200 bps full duplex modem implementation
- Detection of tones in the call progress band by selecting filters

Description

The MT35212A is an ISO²-CMOS integrated circuit designed to implement both the filtering and equalizing functions required in Bell 212A and CCITT V.22 modems. The MT35212A includes both

Pin Connections	
SEL2	1
VEE	2
RX(IN)	3
CLK1	4
R(OUT)	5
R -	6
R +	7
VDD	8
SEL1	9
AGND	10
A/O MODE	11
NC	12
24	RX (OUT)
23	DGND
22	CLK2
21	T -
20	T +
19	T (OUT)
18	TX (IN)
17	NSEL
16	NFO
15	TX(OUT)
14	AL
13	NC

Ordering Information 0°C to 70°C

MT35212AE	Plastic DIP
MT35212AP	PLCC

the transmit signal shaping filter and the receive signal separation filter and features on-chip originate/answer mode selection. In addition, half-channel compromise amplitude and group delay equalizers are included. Provision is made for the receive smoothing filter to switch between the Call Progress mode and the normal data transmission mode.

5

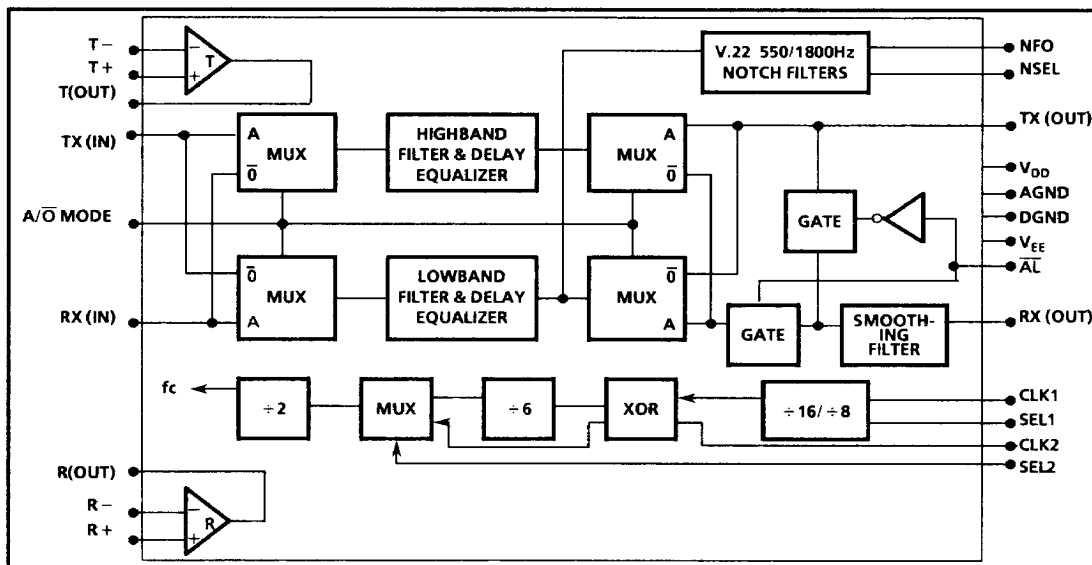


Figure 1- Functional Block Diagram

5-3

MT35212A ISO²-CMOS

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Positive Supply Voltage	V _{DD}		6.75	V
2	Negative Supply Voltage	V _{EE}		-6.75	V
3	Storage Temperature Range	T _{STG}	-55	+125	°C
4	Analog Input	V	V _{EE} - 0.3	V _{DD} + 0.3	V

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground unless otherwise stated.

	Characteristics	Sym	Min	Typ [†]	Max	Units	Test Conditions
1	Positive Supply Voltage	V _{DD}	4.75	5	5.25	V	DGND = AGND = 0 V
2	Negative Supply Voltage	V _{EE}	-4.75	-5	-5.25	V	DGND = AGND = 0 V
3	Operating Temperature Range	T _O	0	25	70	°C	

[†] Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Operating Conditions - T_O = 0°C to 70°C.

	Characteristics	Sym	Min	Typ [†]	Max	Units	Test Conditions
1	Positive Supply Voltage	V _{DD}	+4.75	5.0	5.25	V	
2	Negative Supply Voltage	V _{EE}	-4.75	-5.0	-5.25	V	
3	Power Consumption	P _C		75	150	mW	V _{DD} = 5.25V; V _{EE} = -5.25V

[†] Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - V_{DD} = +5 V ± 5%, V_{EE} = -5 V ± 5%, AGND = DGND = 0 V, T_O = 0°C to 70°C.

	Characteristics	Sym	Min	Typ [†]	Max	Units	Test Conditions
1	I ₁ High Level Logic	V _{IH}	4		V _{DD}	V	Pins 1, 9, 11, 14, 17.
2	I ₂ High Level Logic	V _{IH}	2.0		V _{DD}	V	Pins 4, 22.
3	I ₃ Low Level Logic	V _{IL}	V _{EE}		0.8	V	Pins 1, 4, 9, 11, 14, 17, 22.
4	I ₄ Resistance	R _{IN}		5		MΩ	Pins 3, 18.
5	I ₅ Capacitance	C _{IN}		10		pF	Pins 3, 18.

[†] Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics - V_{DD} = +5 V ± 5%, V_{EE} = -5 V ± 5%, AGND = DGND = 0 V, T_O = 0°C to 70°C.

	Characteristics	Sym	Min	Typ [†]	Max	Units	Test Conditions
1	Reference Signal Level Input	V _{REF}		1		V _{RMS}	
2	Maximum Signal Level Input	V _{MAX}			1.4125	V _{RMS}	
3	Bandwidth (both bands)	BW		960		Hz	
4	Gain at Center Frequencies	A _{FO}	-1.0	0	+1.0	dB	
5	Idle Channel Noise - Low Band Filter High Band Filter			23 22	33 33	dB _{BrnC0} dB _{BrnC0}	No load.
6	Harmonic Distortion	THD		-55		dB	
7	Clock Feed Through with respect to signal level	CLK _{FT}		-23 -60		dB dB	T _X (clock feedthrough R _X frequency is 76.8 kHz)

[†] Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

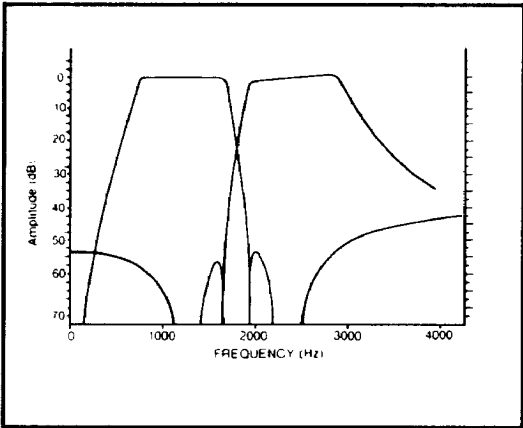


Fig. 2 - Typical Amplitude vs. Frequency Plot

FREQUENCY (Hz)	RELATIVE GAIN	
	MIN.	MAX.
Lowband	400	-35
	800	+1
	1200	+1
	1600	+1
	1800	-18
	2000	-48
	2400	-55
	2800	-50
Highband	800	-50
	1200	-53
	1600	-50
	2000	+0.5
	2400	+1
	2800	+2.5
	3200	-10
	3500	-20

Table 1 - Amplitude vs. Frequency Response

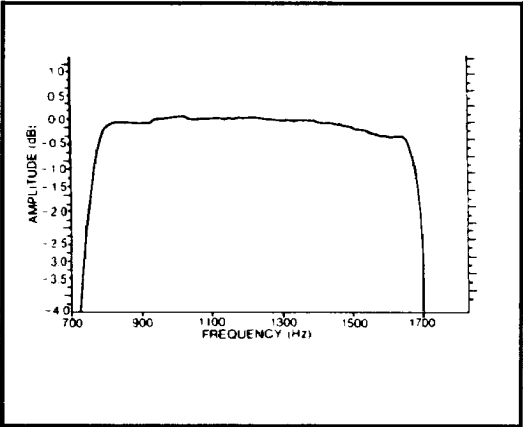


Fig. 3 - Typical Lowband Amplitude vs. Frequency Plot

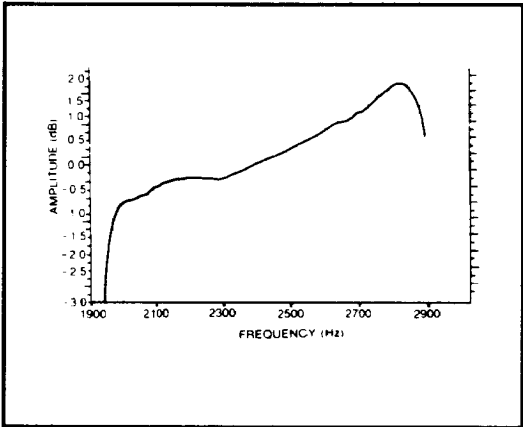


Fig. 5 - Typical Highband Amplitude vs. Frequency Plot

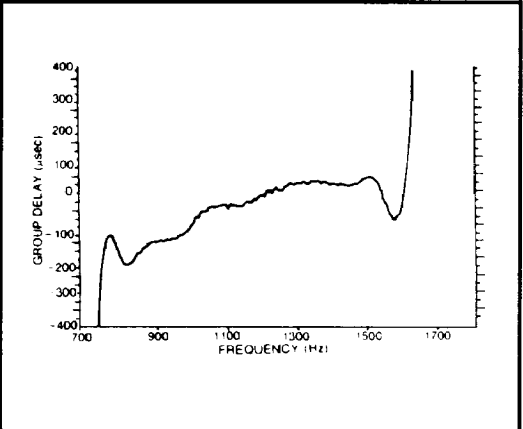


Fig. 4 - Typical Lowband Group Delay vs. Frequency Plot

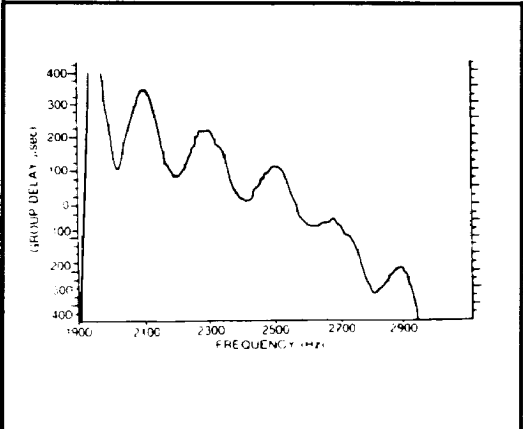


Fig. 6 - Typical Highband Group Delay vs. Frequency Plot

MT35212A ISO²-CMOS

Pin Description

Pin #	Name	Description
1	SEL2	Select 2. A logic '0' selects normal operation. A logic '1' scales the filter frequency response by a factor of six for Call Progress Tone Detection with the high group filter.
2	V _{EE}	Negative supply voltage (typically – 5 V) .
3	RX(IN)	Receive signal input.
4	CLK1	Digital Clock 1. TTL/CMOS input clock at 2.4576 or 1.2288 MHz. If CLK2 is used, CLK1 should be left unconnected.
5	R(OUT)	Receive uncommitted Op Amp Output.
6	R–	Receive uncommitted Op Amp Input. Inverting input.
7	R+	Receive uncommitted Op Amp Input. Non-inverting input.
8	V _{DD}	Positive supply voltage (typically + 5 V).
9	SEL1	Select 1. Logic '0' permits operation at 1.2288 MHz; Logic '1' permits operation at 2.4576 MHz.
10	AGND	Analog ground.
11	A/ \bar{O} MODE	Mode Answer/Originate. A logic '0' sets the device in originate mode - the transmit signal in the low band, and the receive signal in the high band. A logic '1' sets the device in the answer mode (the opposite bands to the originate mode).
12	NC	No Connection.
13	NC	No Connection.
14	$\bar{A}L$	Analog Loopback control input. A logic '0' sets the device in loopback mode. A logic "1" sets the device in normal mode.
15	TX(OUT)	Transmit Signal Output. Filtered transmit signal. This output will drive a 20 k Ω load.
16	NFO	Notch Filter Output. This output is capable of driving 20 k Ω .
17	NSEL	Notch Select. A logic '0' on this input will select the notch filter to reject 550 Hz. A logic '1' selects a notch at 1800 Hz.
18	TX(IN)	Transmit/Signal Input. Unfiltered signal input.
19	T(OUT)	Transmit uncommitted op amp output.
20	T+	Transmit uncommitted op amp non-inverting input.
21	T–	Transmit uncommitted op amp inverting input.
22	CLK2	Digital Clock 2. TTL/CMOS input clock at 153.6 kHz. If CLK1 is used, CLK2 should be left unconnected.
23	DGND	Digital Ground.
24	RX(OUT)	Receive Signal Output. This output is capable of driving a 20 k Ω load.

Functional Description

The MT35212A modem filter implements both the filtering and equalizing functions required in Bell 212A and CCITT V.22 Modems. For CCITT V.22 applications a notch filter is included. The MT35212A includes both the transmit signal shaping filter and the receive signal separation filter and features on-chip originate/answer mode selection. In addition, half-channel compromise amplitude and group delay equalizers are included giving full compromise equalization through the transmit and receive filter pair. For the Call Progress Mode provision is made to select the R_X (OUT) smoothing filter. See Call Progress Mode for details.

Figure 1 illustrates the functionality of the MT35212A modem filter. Selection between the call progress tone detection mode and the normal data transmission mode is made via Pin 1 (SEL2). For CCITT V.22 applications the notch filter can be programmed to provide rejection at 1800 Hz or 550 Hz via Pin 17 (NSEL). For maximum flexibility the MT35212A may be operated from a 2.4576 MHz, 1.2288 MHz, or 153.6 kHz clock. Refer to Table 2 for input clock selection.

CLOCK INPUT	SEL1	CLK1	CLK2
153.6 kHz	Don't care	Open	Input
1.2288 MHz	logic '0'	Input	Open
2.4576 MHz	logic '1'	Input	Open

Table 2 - Input Clock Selection

Two uncommitted operational amplifiers are provided which can be used for gain control or anti-aliasing filters.

Call Progress Mode Operation

A logic '1' on Pin 1 (SEL2) selects this mode. This will insert a divide by six factor in the clock frequency (f_c) causing the center frequencies of the filters to shift down to one-sixth of their original values. As a result, the 1200 Hz filter will be centered around 200 Hz and the 2400 Hz filter will be centered around 400 Hz. Refer to figure 2.

With the high group filter centered at 400 Hz, its passband will be approximately 300 Hz to 480 Hz. This allows the precision dial tone of 350/440 Hz to pass, as well as audible ringing at 440/480 Hz. Half of the busy or reorder tone of 480/620 Hz will also pass through the high group filter in this mode.

By using a suitable detector circuit combined with a method of timing determination it is possible to build a more intelligent modem that can communicate back to its terminal or computer the status of the phone call.

Diagnostic Mode

The MT35212A has Analog Loopback capability. A logic '0' on $\overline{\text{AL}}$ pin switches the transmit carrier output back through the receive smoothing filter for testing. For normal operation the $\overline{\text{AL}}$ pin should be connected to a High voltage level (+5 V).