PRELIMINARY DATA SHEET

# MSP 34x7G
# Multistandard
# Sound Processor Family

Edition March 5, 2001
6251-535-2PD

MICRONAS

**Contents**


| Page | Section | Title |
|---|---|---|
| **5** | **1.** | **Introduction** |
| 6 | 1.1. | Features of the MSP 34x7G Family and Differences to MSPD |
| 6 | 1.2. | MSP 34x7G Version List |
| 7 | 1.3. | MSP 34x7G Versions and their Application Fields |
| **8** | **2.** | **Functional Description** |
| 9 | 2.1. | Architecture of the MSP 34x7G Family |
| 9 | 2.2. | Sound IF Processing |
| 9 | 2.2.1. | Analog Sound IF Input |
| 9 | 2.2.2. | Demodulator: Standards and Features |
| 10 | 2.2.3. | Preprocessing of Demodulator Signals |
| 10 | 2.2.4. | Automatic Sound Select |
| 10 | 2.2.5. | Manual Mode |
| 12 | 2.3. | Preprocessing for SCART |
| 12 | 2.4. | Source Selection and Output Channel Matrix |
| 12 | 2.5. | Audio Baseband Processing |
| 12 | 2.5.1. | Automatic Volume Correction (AVC) |
| 12 | 2.5.2. | Quasi-Peak Detector |
| 13 | 2.6. | SCART Signal Routing |
| 13 | 2.6.1. | SCART DSP In and SCART Out Select |
| 13 | 2.6.2. | Stand-by Mode |
| 13 | 2.7. | Digital Control I/O Pins and Status Change Indication |
| 13 | 2.8. | Clock PLL Oscillator and Crystal Specifications |
| **14** | **3.** | **Control Interface** |
| 14 | 3.1. | $I^2C$ Bus Interface |
| 14 | 3.1.1. | Internal Hardware Error Handling |
| 15 | 3.1.2. | Description of CONTROL Register |
| 15 | 3.1.3. | Protocol Description |
| 16 | 3.1.4. | Proposals for General MSP 34x7G $I^2C$ Telegrams |
| 16 | 3.1.4.1. | Symbols |
| 16 | 3.1.4.2. | Write Telegrams |
| 16 | 3.1.4.3. | Read Telegrams |
| 16 | 3.1.4.4. | Examples |
| 16 | 3.2. | Start-Up Sequence: Power-Up and $I^2C$-Controlling |
| 16 | 3.3. | MSP 34x7G Programming Interface |
| 16 | 3.3.1. | User Registers Overview |
| 18 | 3.3.2. | Description of User Registers |
| 19 | 3.3.2.1. | STANDARD SELECT Register |
| 19 | 3.3.2.2. | Refresh of STANDARD SELECT Register |
| 19 | 3.3.2.3. | STANDARD RESULT Register |
| 21 | 3.3.2.4. | Write Registers on $I^2C$ Subaddress $10_{hex}$ |
| 22 | 3.3.2.5. | Read Registers on $I^2C$ Subaddress $11_{hex}$ |
| 23 | 3.3.2.6. | Write Registers on $I^2C$ Subaddress $12_{hex}$ |
| 29 | 3.3.2.7. | Read Registers on $I^2C$ Subaddress $13_{hex}$ |
| 30 | 3.4. | Programming Tips |
| 30 | 3.5. | Examples of Minimum Initialization Codes |

**Contents, continued**


| Page | Section | Title |
|---|---|---|
| 30 | 3.5.1. | B/G-FM (A2 or NICAM) |
| 30 | 3.5.2. | BTSC-Stereo |
| 30 | 3.5.3. | BTSC-SAP with SAP at Loudspeaker Channel |
| 31 | 3.5.4. | FM-Stereo Radio |
| 31 | 3.5.5. | Automatic Standard Detection |
| 31 | 3.5.6. | Software Flow for Interrupt driven STATUS Check |
| **33** | **4.** | **Specifications** |
| 33 | 4.1. | Outline Dimensions |
| 34 | 4.2. | Pin Connections and Short Descriptions |
| 36 | 4.3. | Pin Descriptions |
| 38 | 4.4. | Pin Configurations |
| 39 | 4.5. | Pin Circuits |
| 41 | 4.6. | Electrical Characteristics |
| 41 | 4.6.1. | Absolute Maximum Ratings |
| 42 | 4.6.2. | Recommended Operating Conditions |
| 42 | 4.6.2.1. | General Recommended Operating Conditions |
| 42 | 4.6.2.2. | Analog Input and Output Recommendations |
| 43 | 4.6.2.3. | Recommendations for Analog Sound IF Input Signal |
| 44 | 4.6.2.4. | Crystal Recommendations |
| 46 | 4.6.3. | Characteristics |
| 46 | 4.6.3.1. | General Characteristics |
| 47 | 4.6.3.2. | Digital Inputs, Digital Outputs |
| 48 | 4.6.3.3. | Reset Input and Power-Up |
| 49 | 4.6.3.4. | $I^2C$ Bus Characteristics |
| 50 | 4.6.3.5. | Analog Baseband Inputs and Outputs, AGNDC |
| 51 | 4.6.3.6. | Sound IF Input |
| 51 | 4.6.3.7. | Power Supply Rejection |
| 52 | 4.6.3.8. | Analog Performance |
| 53 | 4.6.3.9. | Sound Standard Dependent Characteristics |
| **57** | **5.** | **Appendix A: Overview of TV Sound Standards** |
| 57 | 5.1. | NICAM 728 |
| 58 | 5.2. | A2 Systems |
| 59 | 5.3. | BTSC-Sound System |
| 59 | 5.4. | Japanese FM Stereo System (EIA-J) |
| 60 | 5.5. | FM Satellite Sound |
| 60 | 5.6. | FM-Stereo Radio |
| **61** | **6.** | **Appendix B: Manual/Compatibility Mode** |
| 61 | 6.1. | Demodulator Write and Read Registers for Manual/Compatibility Mode |
| 62 | 6.2. | DSP Write and Read Registers for Manual/Compatibility Mode |
| 63 | 6.3. | Manual/Compatibility Mode: Description of Demodulator Write Registers |
| 63 | 6.3.1. | Automatic Switching between NICAM and Analog Sound |
| 63 | 6.3.1.1. | Function in Automatic Sound Select Mode |
| 63 | 6.3.1.2. | Function in Manual Mode |
| 65 | 6.3.2. | A2 Threshold |
| 65 | 6.3.3. | Carrier-Mute Threshold |

**Contents, continued**


| Page | Section | Title |
|---|---|---|
| 66 | 6.3.4. | Register AD_CV |
| 68 | 6.3.5. | Register MODE_REG |
| 69 | 6.3.6. | FIR-Parameter, Registers FIR1 and FIR2 |
| 69 | 6.3.7. | DCO-Registers |
| 71 | 6.4. | Manual/Compatibility Mode: Description of Demodulator Read Registers |
| 71 | 6.4.1. | NICAM Mode Control/Additional Data Bits Register |
| 71 | 6.4.2. | Additional Data Bits Register |
| 71 | 6.4.3. | CIB Bits Register |
| 72 | 6.4.4. | NICAM Error Rate Register |
| 72 | 6.4.5. | PLL_CAPS Readback Register |
| 72 | 6.4.6. | AGC_GAIN Readback Register |
| 72 | 6.4.7. | Automatic Search Function for FM-Carrier Detection in Satellite Mode |
| 73 | 6.5. | Manual/Compatibility Mode: Description of DSP Write Registers |
| 73 | 6.5.1. | Additional Channel Matrix Modes |
| 73 | 6.5.2. | Volume Modes of SCART1 Output |
| 73 | 6.5.3. | FM Fixed Deemphasis |
| 73 | 6.5.4. | FM Adaptive Deemphasis |
| 73 | 6.5.5. | NICAM Deemphasis |
| 74 | 6.5.6. | Identification Mode for A2 Stereo Systems |
| 74 | 6.5.7. | FM DC Notch |
| 74 | 6.6. | Manual/Compatibility Mode: Description of DSP Read Registers |
| 74 | 6.6.1. | Stereo Detection Register for A2 Stereo Systems |
| 74 | 6.6.2. | DC Level Register |
| 75 | 6.7. | Demodulator Source Channels in Manual Mode |
| 75 | 6.7.1. | Terrestric Sound Standards |
| 75 | 6.7.2. | SAT Sound Standards |
| 75 | 6.8. | Exclusions of Audio Baseband Features |
| 75 | 6.9. | Compatibility Restrictions to MSP 34x7D |
| **77** | **7.** | **Appendix D: Application Information** |
| 77 | 7.1. | Phase Relationship of Analog Outputs |
| 78 | 7.2. | Application Circuit |
| **80** | **8.** | **Appendix E: MSP 34x7G Version History** |
| **80** | **9.** | **Data Sheet History** |


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**Multistandard Sound Processor Family**

**Release Note: Revision bars indicate significant changes to the previous edition. The hardware and software description in this document is valid for the MSP 34x7G version B8 and following versions.**

## 1. Introduction

The MSP 34x7G family of single-chip Multistandard Sound Processors covers the sound processing of all analog TV standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed in a single chip. Figure 1–1 shows a simplified functional block diagram of the MSP 34x7G.

These TV sound processing ICs include versions for processing the multichannel television sound (MTS) signal conforming to the standard recommended by the Broadcast Television Systems Committee (BTSC). The DBX noise reduction, or alternatively, Micronas Noise Reduction (MNR) is performed alignment free.

Other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM-Stereo-Radio standard.

Current ICs have to perform adjustment procedures in order to achieve good stereo separation for BTSC and EIA-J. The MSP 34x7G has optimum stereo performance without any adjustments.

All MSP 34xxG versions are pin compatible to the MSP 34xxD. Only minor modifications are necessary to adapt a MSP 34xxD controlling software to the MSP 34xxG. The MSP 34x7G further simplifies controlling software. Standard selection requires a single $I^2C$ transmission only.

**Note:** The MSP 34x7G version has reduced control registers and less functional pins. The remaining registers are software-compatible to the MSP 34x0G. The pinning is compatible to the MSP 34x0G.

The MSP 34x7G has built-in automatic functions: The IC is able to detect the actual sound standard automatically (Automatic Standard Detection). Furthermore, pilot levels and identification signals can be evaluated internally with subsequent switching between mono/stereo/bilingual; no $I^2C$ interaction is necessary (Automatic Sound Selection).

The MSP 34x7G can handle very high FM deviations even in conjunction with NICAM processing. This is especially important for the introduction of NICAM in China.

The ICs are produced in submicron CMOS technology. The MSP 34x7G is available in the following packages: PSDIP52 and PMQFP44.

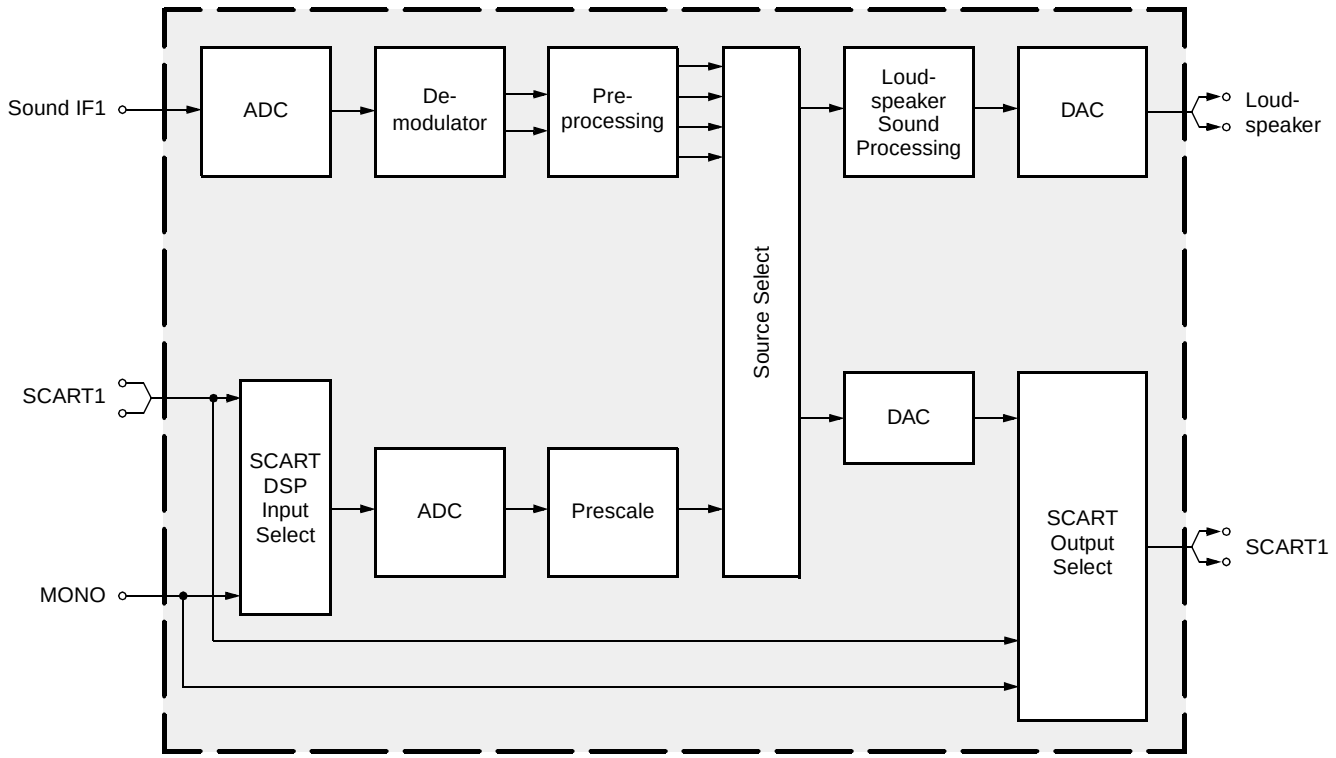



**Fig. 1–1:** Simplified functional block diagram of MSP 34x7G

## 1.1. Features of the MSP 34x7G Family and Differences to MSPD

| **Feature** (Features not available for MSPD are shaded gray.) | **3407** | **3417** | **3427** | **3447** | **3457** | **3467** |
|---|---|---|---|---|---|---|
| Standard Selection with single $I^2C$ transmission | X | X | X | X | X | X |
| Automatic Standard Detection of terrestrial TV standards | X | X | X | X | X | X |
| Automatic Sound Selection (mono/stereo/bilingual), new registers MODUS, STATUS | X | X | X | X | X | X |
| Automatic Carrier Mute function | X | X | X | X | X | X |
| Interrupt output programmable (indicating status change) | X | X | X | X | X | X |
| Loudspeaker channel with volume | X | X | X | X | X | X |
| AVC: Automatic Volume Correction | X | X | X | X | X | X |
| One Stereo SCART (line) input, one Mono input; one Stereo SCART output | X | X | X | X | X | X |
| Complete SCART in/out switching matrix | X | X | X | X | X | X |
| All analog Mono sound carriers including AM-SECAM L | X | X | X | X | X | X |
| All analog FM-Stereo A2 and satellite standards | X | X | | | X | |
| All NICAM standards | | X | | | X | |
| Simultaneous demodulation of (very) high-deviation FM-Mono and NICAM | | X | | | X | |
| Adaptive deemphasis for satellite (Wegener-Panda, acc. to ASTRA specification) | X | X | | | X | X |
| Demodulation of the BTSC multiplex signal and the SAP channel | | | X | X | X | |
| Alignment free digital DBX noise reduction for BTSC Stereo and SAP | | | | X | X | |
| Alignment free digital Micronas Noise Reduction (MNR) for BTSC Stereo and SAP | | | X | | | |
| BTSC stereo separation (MSP 3427/47G also EIA-J) significantly better than spec. | | | X | X | X | |
| SAP and stereo detection for BTSC system | | | X | X | X | |
| Korean FM-Stereo A2 standard | X | X | X | X | X | |
| Alignment-free Japanese standard EIA-J | | | X | X | X | |
| Demodulation of the FM-Radio multiplex signal | | | X | X | X | |

## 1.2. MSP 34x7G Version List

| **Version** | **Status** | **Description** |
|---|---|---|
| MSP 3407G | available | FM Stereo (A2) Version |
| MSP 3417G | available | NICAM and FM Stereo (A2) Version |
| MSP 3427G | not confirmed | NTSC Version (A2 Korea, BTSC with Micronas Noise Reduction (MNR), Japanese EIA-J system) |
| MSP 3447G | not confirmed | NTSC Version (A2 Korea, BTSC with DBX noise reduction, Japanese EIA-J system) |
| MSP 3457G | not confirmed | Global Stereo Version (all sound standards) |
| MSP 3467G | not confirmed | Global Mono Version (all sound standards) |

### 1.3. MSP 34x7G Versions and their Application Fields

Table 1–1 provides an overview of TV sound standards that can be processed by the MSP 34x7G family. In addition, the MSP 34x7G is able to handle the FM-Radio standard. With the MSP 34x7G, a complete multimedia receiver covering all TV sound standards together with terrestrial/cable and satellite radio sound can be built.

**Table 1–1:** TV Stereo Sound Standards covered by the MSP 34x7G IC Family (details see Appendix A)

| MSP Version | | | | TV-System | Position of Sound Carrier /MHz | Sound Modulation | Color System | Broadcast e.g. in: |
|---|---|---|---|---|---|---|---|---|
| 3407 | | | 3457 | B/G | 5.5/5.7421875 | FM-Stereo (A2) | PAL | Germany |
| | | | | | 5.5/5.85 | FM-Mono/NICAM | PAL | Scandinavia, Spain |
| | | | | L | 6.5/5.85 | AM-Mono/NICAM | SECAM-L | France |
| | | | | I | 6.0/6.552 | FM-Mono/NICAM | PAL | UK, Hong Kong |
| 3407 | | 3417 | | D/K | 6.5/6.2578125 | FM-Stereo (A2, D/K1) | SECAM-East | Slovak. Rep. |
| | | | | | 6.5/6.7421875 | FM-Stereo (A2, D/K2) | PAL | currently no broadcast |
| | | | | | 6.5/5.7421875 | FM-Stereo (A2, D/K3) | SECAM-East | Poland |
| | | | | | 6.5/5.85 | FM-Mono/NICAM (D/K, NICAM) | PAL | China, Hungary |
| 3407 | | | | Satellite | 6.5<br>7.02/7.2<br>7.38/7.56<br>etc. | FM-Mono<br>FM-Stereo | PAL | Europe Sat.<br>ASTRA |
| | 3427, 3447 | | | M/N | 4.5/4.724212 | FM-Stereo (A2) | NTSC | Korea |
| | | | | | 4.5 | FM-FM (EIA-J) | NTSC | Japan |
| | | | | | 4.5 | BTSC-Stereo + SAP | NTSC, PAL | USA, Argentina |
| | | | | FM-Radio | 10.7 | FM-Stereo Radio | | USA, Europe |
| 3467 | | | | All standards as above, but Mono demodulation only. | | | | |

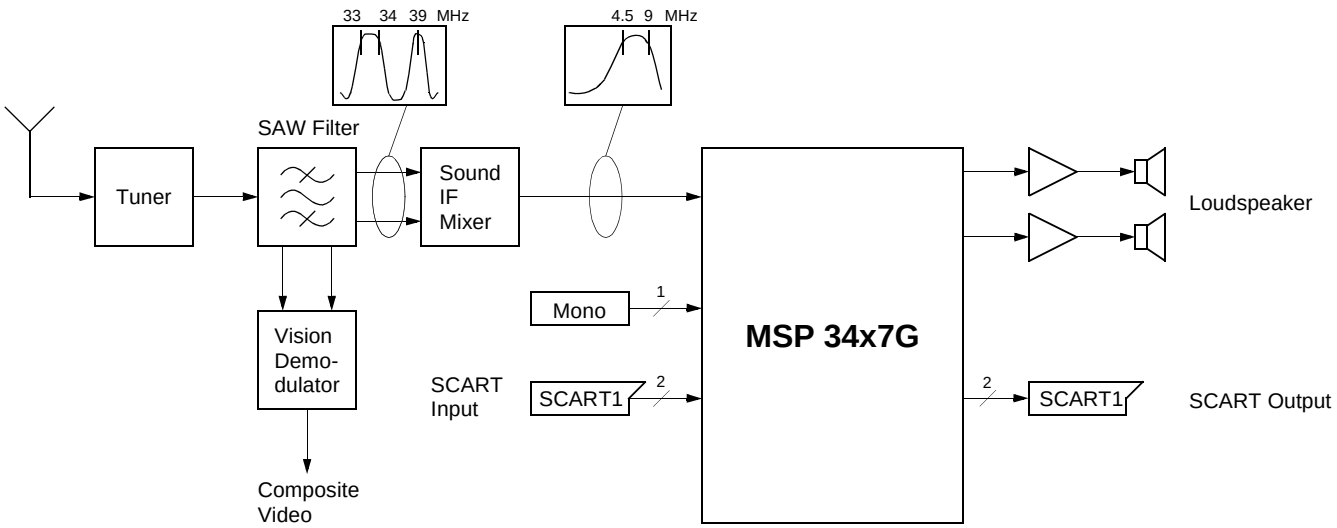



**Fig. 1–2:** Typical MSP 34x7G application

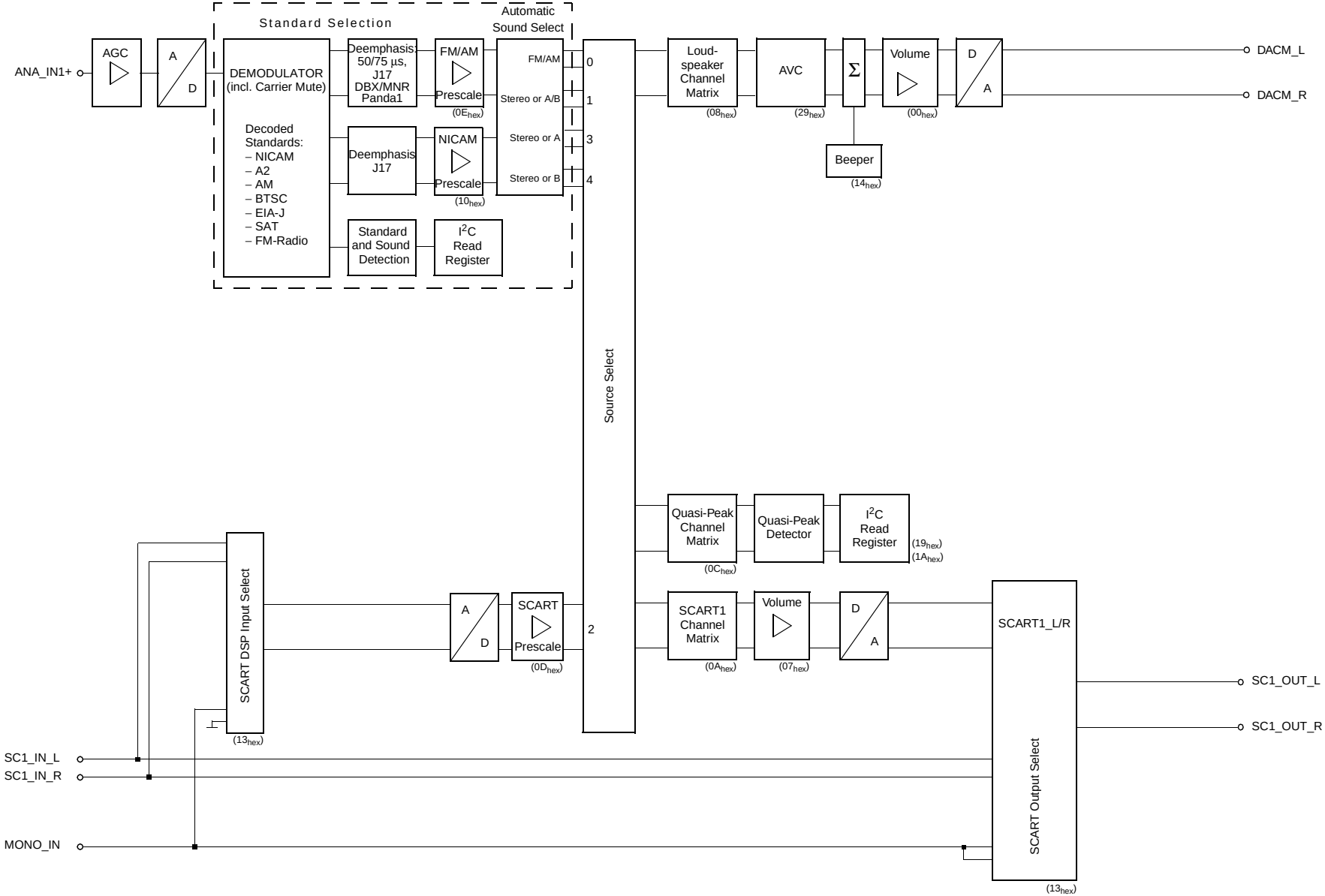



**Fig. 2–1:** Signal flow block diagram of the MSP 34x7G (input and output names correspond to pin names).

### 2.1. Architecture of the MSP 34x7G Family

Fig. 2–1 on page 8 shows a simplified block diagram of the IC. The block diagram contains all features of the MSP 3457G. Other members of the MSP 34x7G family do not have the complete set of features: The demodulator handles only a subset of the standards presented in the demodulator block; NICAM processing is only possible in the MSP 3417G and MSP 3457G (see dashed block in Fig. 2–1).

### 2.2. Sound IF Processing

#### 2.2.1. Analog Sound IF Input

The input pins ANA_IN1+ and ANA_IN– offer the possibility to connect sound IF (SIF) sources to the MSP 34x7G. The analog-to-digital conversion of the sound IF signal is done by an A/D-converter. An analog automatic gain circuit (AGC) allows a wide range of input levels. The high-pass filter formed by the coupling capacitor at pin ANA_IN1+ (see Section 7. “Appendix D: Application Information” on page 77) is sufficient in most cases to suppress video components. Some combinations of SAW filters and sound IF mixer ICs, however, show large picture components on their outputs. In this case, further filtering is recommended.

#### 2.2.2. Demodulator: Standards and Features

The MSP 34x7G is able to demodulate all TV sound standards worldwide including the digital NICAM system. Depending on the MSP 34x7G version, the following demodulation modes can be performed:

**A2-Systems:** Detection and demodulation of two separate FM carriers (FM1 and FM2), demodulation and evaluation of the identification signal of carrier FM2.

**NICAM-Systems:** Demodulation and decoding of the NICAM carrier, detection and demodulation of the analog (FM or AM) carrier. For D/K-NICAM, the FM carrier may have a maximum deviation of 384 kHz.

**Very high deviation FM-Mono:** Detection and robust demodulation of one FM carrier with a maximum deviation of 540 kHz.

**BTSC-Stereo:** Detection and FM demodulation of the aural carrier resulting in the MTS/MPX signal. Detection and evaluation of the pilot carrier, AM demodulation of the (L-R)-carrier and detection of the SAP subcarrier. Processing of the DBX noise reduction or Micronas Noise Reduction (MNR).

**BTSC-Mono + SAP:** Detection and FM demodulation of the aural carrier resulting in the MTS/MPX signal. Detection and evaluation of the pilot carrier, detection and FM demodulation of the SAP-subcarrier. Processing of the DBX noise reduction or Micronas Noise Reduction (MNR).

**Japan Stereo:** Detection and FM demodulation of the aural carrier resulting in the MPX signal. Demodulation and evaluation of the identification signal and FM demodulation of the (L-R)-carrier.

**FM-Satellite Sound:** Demodulation of one or two FM carriers. Processing of high-deviation mono or narrow bandwidth mono, stereo, or bilingual satellite sound according to the ASTRA specification.

**FM-Stereo-Radio:** Detection and FM demodulation of the aural carrier resulting in the MPX signal. Detection and evaluation of the pilot carrier and AM demodulation of the (L-R)-carrier.

The demodulator blocks of all MSP 34x7G versions have identical user interfaces. Even completely different systems like the BTSC and NICAM systems are controlled the same way. Standards are selected by means of MSP Standard Codes. Automatic processes handle standard detection and identification without controller interaction. The key features of the MSP 34x7G demodulator blocks are

**Standard Selection:** The controlling of the demodulator is minimized: All parameters, such as tuning frequencies or filter bandwidth, are adjusted automatically by transmitting one single value to the STANDARD SELECT register. For all standards, specific MSP standard codes are defined.

Automatic Standard Detection: If the TV sound standard is unknown, the MSP 34x7G can automatically detect the actual standard, switch to that standard, and respond the actual MSP standard code.

**Automatic Carrier Mute:** To prevent noise effects or FM identification problems in the absence of an FM carrier, the MSP 34x7G offers a configurable carrier mute feature, which is activated automatically if the TV sound standard is selected by means of the STANDARD SELECT register. If no FM carrier is detected at one of the two MSP demodulator channels, the corresponding demodulator output is muted. This is indicated in the STATUS register.

### 2.2.3. Preprocessing of Demodulator Signals

The NICAM signals must be processed by a deemphasis filter and adjusted in level. The analog demodulated signals must be processed by a deemphasis filter, adjusted in level, and dematrixed. The correct deemphasis filters are already selected by setting the standard in the STANDARD SELECT register. The level adjustment has to be done by means of the FM/AM and NICAM prescale registers. The necessary dematrix function depends on the selected sound standard and the actual broadcasted sound mode (mono, stereo, or bilingual). It can be manually set by the FM Matrix Mode register or automatically by the Automatic Sound Selection.

### 2.2.4. Automatic Sound Select

In the Automatic Sound Select mode, the dematrix function is automatically selected based on the identification information in the STATUS register. No $I^2C$ interaction is necessary when the broadcasted sound mode changes (e.g. from mono to stereo).

The demodulator supports the identification check by switching between mono-compatible standards (standards that have the same FM-Mono carrier) automatically and non-audible. If B/G-FM or B/G-NICAM is selected, the MSP will switch between these standards. The same action is performed for the standards: D/K1-FM, D/K2-FM, D/K3-FM and D/K-NICAM. Switching is only done in the absence of any stereo or bilingual identification. If identification is found, the MSP keeps the detected standard.

In case of high bit-error rates, the MSP 34x7G automatically falls back from digital NICAM sound to analog FM or AM mono.

Table 2–1 summarizes all actions that take place when Automatic Sound Select is switched on.

To provide more flexibility, the Automatic Sound Select block prepares four different source channels of demodulated sound (Fig. 2–2). By choosing one of the four demodulator channels, the preferred sound mode can be selected for each of the output channels (loudspeaker, headphone, etc.). This is done by means of the Source Select registers.

The following source channels of demodulated sound are defined:

- **“FM/AM” channel:** Analog mono sound, stereo if available. In case of NICAM, analog mono only (FM or AM mono).
- **“Stereo or A/B” channel:** Analog or digital mono sound, stereo if available. In case of bilingual broadcast, it contains both languages A (left) and B (right).
- **“Stereo or A” channel:** Analog or digital mono sound, stereo if available. In case of bilingual broadcast, it contains language A (on left and right).
- **“Stereo or B” channel:** Analog or digital mono sound, stereo if available. In case of bilingual broadcast, it contains language B (on left and right).

Fig. 2–2 and Table 2–2 show the source channel assignment of the demodulated signals in case of Automatic Sound Select mode for all sound standards.

**Note:** The analog primary input channel contains the signal of the mono FM/AM carrier or the L+R signal of the MPX carrier. The secondary input channel contains the signal of the 2nd FM carrier, the L-R signal of the MPX carrier, or the SAP signal.

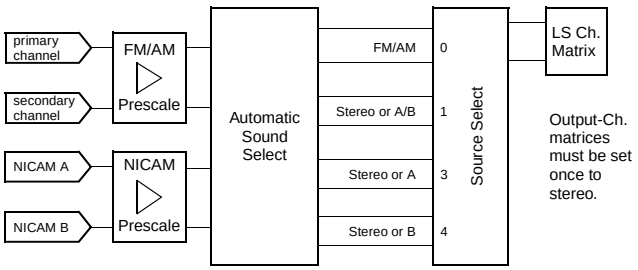



**Fig. 2–2:** Source channel assignment of demodulated signals in Automatic Sound Select Mode

### 2.2.5. Manual Mode

Fig. 2–3 shows the source channel assignment of demodulated signals in case of manual mode. If manual mode is required, more information can be found in Section 6.7. “Demodulator Source Channels in Manual Mode” on page 75.

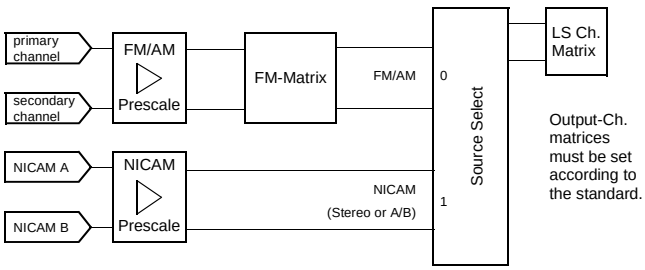



**Fig. 2–3:** Source channel assignment of demodulated signals in Manual Mode

**Table 2–1:** Performed actions of the Automatic Sound Selection

| Selected TV Sound Standard | Performed Actions |
|---|---|
| B/G-FM, D/K-FM, M-Korea, and M-Japan | Evaluation of the identification signal and automatic switching to mono, stereo, or bilingual. Preparing four demodulator source channels according to Table 2–2. |
| B/G-NICAM, L-NICAM, I-NICAM, D/K-NICAM | Evaluation of NICAM-C-bits and automatic switching to mono, stereo, or bilingual. Preparing four demodulator source channels according to Table 2–2. |
| | In case of bad or no NICAM reception, the MSP switches automatically to FM/AM mono and switches back to NICAM if possible. A hysteresis prevents periodical switching. |
| B/G-FM, B/G-NICAM<br>or<br>D/K1-FM, D/K2-FM, D/K3-FM, and D/K-NICAM | Automatic searching for stereo/bilingual-identification in case of mono transmission. Automatic and non-audible changes between Dual-FM and FM-NICAM standards while listening to the basic FM-mono sound carrier.<br>Example: If starting with B/G-FM-Stereo, there will be a periodical alternation to B/G-NICAM in the absence of FM-Stereo/Bilingual or NICAM-identification. Once an identification is detected, the MSP keeps the corresponding standard. |
| BTSC-STEREO, FM Radio | Evaluation of the pilot signal and automatic switching to mono or stereo. Preparing four demodulator source channels according to Table 2–2. Detection of the SAP carrier. |
| M-BTSC-SAP | In the absence of SAP, the MSP switches to BTSC-stereo if available. If SAP is detected, the MSP switches automatically to SAP (see Table 2–2). |

**Table 2–2:** Sound modes for the demodulator source channels with Automatic Sound Select

| | | | Source Channels in Automatic Sound Select Mode | | | |
|---|---|---|---|---|---|---|
| **Broadcasted Sound Standard** | **Selected MSP Standard Code**[3] | **Broadcasted Sound Mode** | **FM/AM** (source select: 0) | **Stereo or A/B** (source select: 1) | **Stereo or A** (source select: 3) | **Stereo or B** (source select: 4) |
| M-Korea<br>B/G-FM<br>D/K-FM<br>M-Japan | 02<br>03, 08[1]<br>04, 05, 07, 0B[1]<br>30 | MONO | Mono | Mono | Mono | Mono |
| | | STEREO | Stereo | Stereo | Stereo | Stereo |
| | | BILINGUAL:<br>Languages A and B | Right = B | Left = A<br>Right = B | A | B |
| B/G-NICAM<br>L-NICAM<br>I-NICAM<br>D/K-NICAM<br>D/K-NICAM (with high deviation FM) | 08, 03[2]<br>09<br>0A<br>0B, 04[2], 05[2]<br>0C, 0D | NICAM not available or error rate too high | analog Mono | analog Mono | analog Mono | analog Mono |
| | | MONO | analog Mono | NICAM Mono | NICAM Mono | NICAM Mono |
| | | STEREO | analog Mono | NICAM Stereo | NICAM Stereo | NICAM Stereo |
| | | BILINGUAL:<br>Languages A and B | analog Mono | Left = NICAM A<br>Right = NICAM B | NICAM A | NICAM B |
| BTSC | 20, 21 | MONO | Mono | Mono | Mono | Mono |
| | | STEREO | Stereo | Stereo | Stereo | Stereo |
| | 20 | MONO + SAP | Mono | Mono | Mono | Mono |
| | | STEREO + SAP | Stereo | Stereo | Stereo | Stereo |
| | 21 | MONO + SAP | Left = Mono<br>Right = SAP | Left = Mono<br>Right = SAP | Mono | SAP |
| | | STEREO + SAP | Left = Mono<br>Right = SAP | Left = Mono<br>Right = SAP | Mono | SAP |
| FM Radio | 40 | MONO | Mono | Mono | Mono | Mono |
| | | STEREO | Stereo | Stereo | Stereo | Stereo |

[1] The Automatic Sound Select process will automatically switch to the mono compatible analog standard.
[2] The Automatic Sound Select process will automatically switch to the mono compatible digital standard.
[3] The MSP Standard Codes are defined in Table 3–7 on page 18.

### 2.3. Preprocessing for SCART

The SCART input need only be adjusted in level by means of the SCART prescale register.

### 2.4. Source Selection and Output Channel Matrix

The Source Selector makes it possible to distribute all source signals (one of the demodulator source channels or SCART) to the desired output channels (loudspeaker, etc.). All input and output signals can be processed simultaneously. Each source channel is identified by a unique source address.

For each output channel, the sound mode can be set to sound A, sound B, stereo, or mono by means of the output channel matrix.

If Automatic Sound Select is on, the output channel matrix can stay fixed to stereo (transparent) for demodulated signals.

### 2.5. Audio Baseband Processing

#### 2.5.1. Automatic Volume Correction (AVC)

Different sound sources (e.g. terrestrial channels, SAT channels, or SCART) fairly often do not have the same volume level. Advertisements during movies usually have a higher volume level than the movie itself. This results in annoying volume changes. The AVC solves this problem by equalizing the volume level.

To prevent clipping, the AVC's gain decreases quickly in dynamic boost conditions. To suppress oscillation effects, the gain increases rather slowly for low level inputs. The decay time is programmable by means of the AVC register (see page 27).

For input signals ranging from –24 dBr to 0 dBr, the AVC maintains a fixed output level of –18 dBr. Fig. 2–4 shows the AVC output level versus its input level. For prescale and volume registers set to 0 dB, a level of 0 dBr corresponds to full scale input/output. This is

– SCART input/output 0 dBr = 2.0 $V_{rms}$

– Loudspeaker output 0 dBr = 1.4 $V_{rms}$

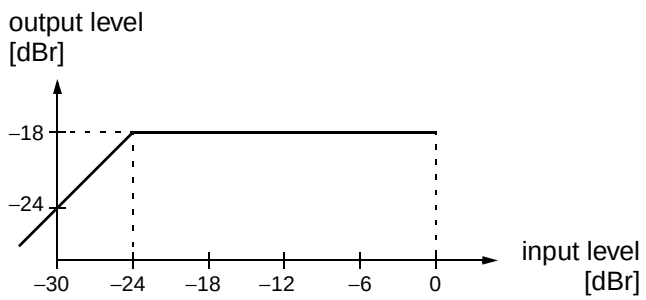



**Fig. 2–4:** Simplified AVC characteristics

#### 2.5.2. Quasi-Peak Detector

The quasi-peak readout register can be used to read out the quasi-peak level of any input source. The feature is based on following filter time constants:

attack time: 1.3 ms
decay time: 37 ms

## 2.6. SCART Signal Routing

### 2.6.1. SCART DSP In and SCART Out Select

The SCART DSP Input Select and SCART Output Select blocks include switching facilities. The switches are controlled by the ACB user register (see page 28).

### 2.6.2. Stand-by Mode

If the MSP 34x7G is switched off by first pulling STANDBYQ low and then (after >1 µs delay) switching off DVSUP and AVSUP, but keeping AHVSUP (**'Stand-by'-mode**), the SCART switches maintain their position and function. This allows the copying from SCART-input to SCART-output in the TV set's stand-by mode.

In case of power on or starting from stand-by (switching on the DVSUP and AVSUP, RESETQ going high 2 ms later), all internal registers except the ACB register (page 28) are reset to the default configuration (see Table 3–5 on page 17). The reset position of the ACB register becomes active after the first $I^2C$ transmission into the Baseband Processing part. By transmitting the ACB register first, the reset state can be redefined.

## 2.7. Digital Control I/O Pins and Status Change Indication

The static level of the digital input/output pins D_CTR_I/O_0/1 is switchable between HIGH and LOW via the $I^2C$-bus by means of the ACB register (see page 28). This enables the controlling of external hardware switches or other devices via $I^2C$-bus.

The digital input/output pins can be set to high impedance by means of the MODUS register (see page 21). In this mode, the pins can be used as input. The current state can be read out of the STATUS register (see page 22).

Optionally, the pin D_CTR_I/O_1 can be used as an interrupt request signal to the controller, indicating any changes in the read register STATUS. This makes polling unnecessary; $I^2C$-bus interactions are reduced to a minimum (see STATUS register on page 22 and MODUS register on page 21).

## 2.8. Clock PLL Oscillator and Crystal Specifications

The MSP 34x7G derives all internal system clocks from the 18.432-MHz oscillator. In NICAM mode, the clock is phase-locked to the corresponding source.

For proper performance, the MSP clock oscillator requires a 18.432-MHz crystal. Note, that for the phase-locked mode (NICAM), crystals with tighter tolerance are required.

## 3. Control Interface

### 3.1. I²C Bus Interface

The MSP 34x7G is controlled via the I²C bus slave interface.

The IC is selected by transmitting one of the MSP 34x7G device addresses. In order to allow up to three MSP ICs to be connected to a single bus, an address select pin (ADR_SEL) has been implemented. With ADR_SEL pulled to high, low, or left open, the MSP 34x7G responds to different device addresses. A device address pair is defined as a write address and a read address (see Table 3–1).

**Writing** is done by sending the write device address, followed by the subaddress byte, two address bytes, and two data bytes.

**Reading** is done by sending the write device address, followed by the subaddress byte and two address bytes. Without sending a stop condition, reading of the addressed data is completed by sending the device read address and reading two bytes of data.

Refer to Section 3.1.3. for the I²C bus protocol and to Section 3.4. “Programming Tips” on page 30 for proposals of MSP 34x7G I²C telegrams. See Table 3–2 for a list of available subaddresses.

Besides the possibility of hardware reset, the MSP can also be reset by means of the RESET bit in the CONTROL register by the controller via I²C bus.

Due to the architecture of the MSP 34x7G, the IC cannot react immediately to an I²C request. The typical response time is about 0.3 ms. If the MSP cannot accept another byte of data (e.g. while servicing an internal interrupt), it holds the clock line I2C_CL low to force the transmitter into a wait state. The I²C Bus Master must read back the clock line to detect when the MSP is ready to receive the next I²C transmission. The positions within a transmission where this may happen are indicated by ’Wait’ in Section 3.1.3. The maximum wait period of the MSP during normal operation mode is less than 1 ms.

#### 3.1.1. Internal Hardware Error Handling

In case of any hardware problems (e.g. interruption of the power supply of the MSP), the MSP’s wait period is extended to 1.8 ms. After this time period elapses, the MSP releases data and clock lines.

**Indication and solving the error status:**

To indicate the error status, the remaining acknowledge bits of the actual I²C-protocol will be left high. Additionally, bit[14] of CONTROL is set to one. The MSP can then be reset via the I²C bus by transmitting the RESET condition to CONTROL.

**Indication of reset:**

Any reset, even caused by an unstable reset line etc., is indicated in bit[15] of CONTROL.

A general timing diagram of the I²C bus is shown in Fig. 4–21 on page 49.

**Table 3–1:** I²C Bus Device Addresses

| ADR_SEL | Low (connected to DVSS) | | High (connected to DVSUP) | | Left Open | |
|---|---|---|---|---|---|---|
| **Mode** | **Write** | **Read** | **Write** | **Read** | **Write** | **Read** |
| MSP device address | $80_{hex}$ | $81_{hex}$ | $84_{hex}$ | $85_{hex}$ | $88_{hex}$ | $89_{hex}$ |

**Table 3–2:** I²C Bus Subaddresses

| Name | Binary Value | Hex Value | Mode | Function |
|---|---|---|---|---|
| CONTROL | 0000 0000 | 00 | Read/Write | Write: Software reset of MSP (see Table 3–3)<br>Read: Hardware error status of MSP |
| WR_DEM | 0001 0000 | 10 | Write | write address demodulator |
| RD_DEM | 0001 0001 | 11 | Write | read address demodulator |
| WR_DSP | 0001 0010 | 12 | Write | write address DSP |
| RD_DSP | 0001 0011 | 13 | Write | read address DSP |

### 3.1.2. Description of CONTROL Register

**Table 3–3:** CONTROL as a Write Register

| Name | Subaddress | Bit[15] (MSB) | Bits[14:0] |
|---|---|---|---|
| CONTROL | $00_{hex}$ | 1 : RESET<br>0 : normal | 0 |

**Table 3–4:** CONTROL as a Read Register

| Name | Subaddress | Bit[15] (MSB) | Bit[14] | Bits[13:0] |
|---|---|---|---|---|
| CONTROL | $00_{hex}$ | RESET status after last reading of CONTROL:<br>0 : no reset occured<br>1 : reset occured | Internal hardware status:<br>0 : no error occured<br>1 : internal error occured | not of interest |
| Reading of CONTROL will reset the bits[15,14] of CONTROL. After Power-on, bit[15] of CONTROL will be set; it must be read once to be reset. | | | | |

### 3.1.3. Protocol Description

Write to DSP or Demodulator

| | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S | write device address | Wait | ACK | sub-addr | ACK | addr-byte high | ACK | addr-byte low | ACK | data-byte high | ACK | data-byte low | ACK | P |

Read from DSP or Demodulator

| | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S | write device address | Wait | ACK | sub-addr | ACK | addr-byte high | ACK | addr-byte low | ACK | S | read device address | Wait | ACK | data-byte-high | ACK | data-byte low | NAK | P |

Write to Control Register

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| S | write device address | Wait | ACK | sub-addr | ACK | data-byte high | ACK | data-byte low | ACK | P |

Read from Control Register

| | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S | write device address | Wait | ACK | 00hex | ACK | S | read device address | Wait | ACK | data-byte-high | ACK | data-byte low | NAK | P |

**Note:** S = $I^2C$-Bus Start Condition from master
P = $I^2C$-Bus Stop Condition from master
ACK = Acknowledge-Bit: LOW on I2C_DA from slave (= MSP, light gray) or master (= controller, dark gray)
NAK = Not Acknowledge-Bit: HIGH on I2C_DA from master (dark gray) to indicate ‘End of Read’ or from MSP indicating internal error state
Wait = $I^2C$-Clock line is held low, while the MSP is processing the $I^2C$ command. This waiting time is max. 1 ms

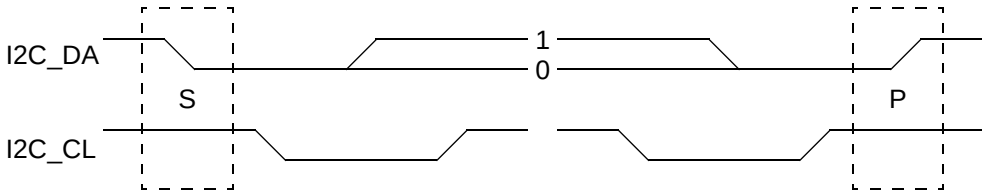



**Fig. 3–1:** $I^2C$ bus protocol (MSB first; data must be stable while clock is high)

### 3.1.4. Proposals for General MSP 34x7G $I^2C$ Telegrams

#### 3.1.4.1. Symbols

| | |
|---|---|
| daw | write device address ($80_{hex}$, $84_{hex}$ or $88_{hex}$) |
| dar | read device address ($81_{hex}$, $85_{hex}$ or $89_{hex}$) |
| < | Start Condition |
| > | Stop Condition |
| aa | Address Byte |
| dd | Data Byte |

#### 3.1.4.2. Write Telegrams

| | |
|---|---|
| `<daw 00 d0 00>` | write to CONTROL register |
| `<daw 10 aa aa dd dd>` | write data into demodulator |
| `<daw 12 aa aa dd dd>` | write data into DSP |

#### 3.1.4.3. Read Telegrams

| | |
|---|---|
| `<daw 00 <dar dd dd>` | read data from CONTROL register |
| `<daw 11 aa aa <dar dd dd>` | read data from demodulator |
| `<daw 13 aa aa <dar dd dd>` | read data from DSP |

#### 3.1.4.4. Examples

| | |
|---|---|
| `<80 00 80 00>` | RESET MSP statically |
| `<80 00 00 00>` | Clear RESET |
| `<80 10 00 20 00 03>` | Set demodulator to stand. $03_{hex}$ |
| `<80 11 02 00 <81 dd dd>` | Read STATUS |
| `<80 12 00 08 01 20>` | Set loudspeaker channel source to NICAM and Matrix to STEREO |

More examples of typical application protocols are listed in Section 3.4. “Programming Tips” on page 30.

## 3.2. Start-Up Sequence: Power-Up and $I^2C$-Controlling

After POWER-ON or RESET (see Fig. 4–20), the IC is in an inactive state. All registers are in the Reset position (see Table 3–5 and Table 3–6), the analog outputs are muted. The controller has to initialize all registers for which a non-default setting is necessary.

## 3.3. MSP 34x7G Programming Interface

### 3.3.1. User Registers Overview

The MSP 34x7G is controlled by means of user registers. The complete list of all user registers are given in Table 3–5 and Table 3–6. The registers are partitioned into the Demodulator section (Subaddress $10_{hex}$ for writing, $11_{hex}$ for reading) and the Baseband Processing sections (Subaddress $12_{hex}$ for writing, $13_{hex}$ for reading).

Write and read registers are 16 bit wide, whereby the MSB is denoted bit[15]. Transmissions via $I^2C$ bus have to take place in 16-bit words (two byte transfers, with the most significant byte transferred first). All write registers, except the demodulator write registers are readable.

Unused parts of the 16-bit write registers must be zero. **Addresses not given in this table must not be accessed.**

For reasons of software compatibility to the MSP 34xxD, a Manual/Compatibility Mode is available. More read and write registers together with a detailed description can be found in “Appendix B: Manual/Compatibility Mode” on page 61.

**Table 3–5:** List of MSP 34x7G Write Registers

| Write Register | Address (hex) | Bits | Description and Adjustable Range | Reset | See Page |
|---|---|---|---|---|---|
| **$I^2C$ Sub-Address = $10_{hex}$ ; Registers are *not* readable** | | | | | |
| STANDARD SELECT | 00 20 | [15:0] | Initial Programming of the Demodulator | 00 00 | 19 |
| MODUS | 00 30 | [15:0] | Demodulator, Automatic options | 00 00 | 21 |
| **$I^2C$ Sub-Address = $12_{hex}$ ; Registers are *all* readable by using $I^2C$ Sub-Address = $13_{hex}$** | | | | | |
| Volume loudspeaker channel | 00 00 | [15:8] | [+12 dB ... −114 dB, MUTE] | MUTE | 26 |
| Volume / Mode loudspeaker channel | | [7:0] | 1/8 dB Steps,<br>Reduce Volume / Tone Control / Compromise / Dynamic | $00_{hex}$ | |
| Volume SCART1 output channel | 00 07 | [15:8] | [+12 dB ... −114 dB, MUTE] | MUTE | 27 |
| Loudspeaker source select | 00 08 | [15:8] | [FM/AM, NICAM, SCART, $I^2S1$, $I^2S2$] | FM/AM | 25 |
| Loudspeaker channel matrix | | [7:0] | [SOUNDA, SOUNDB, STEREO, MONO...] | SOUNDA | 25 |
| SCART1 source select | 00 0A | [15:8] | [FM/AM, NICAM, SCART, $I^2S1$, $I^2S2$] | FM/AM | 25 |
| SCART1 channel matrix | | [7:0] | [SOUNDA, SOUNDB, STEREO, MONO...] | SOUNDA | 25 |
| Quasi-peak detector source select | 00 0C | [15:8] | [FM/AM, NICAM, SCART, $I^2S1$, $I^2S2$] | FM/AM | 25 |
| Quasi-peak detector matrix | | [7:0] | [SOUNDA, SOUNDB, STEREO, MONO...] | SOUNDA | 25 |
| Prescale SCART input | 00 0D | [15:8] | [$00_{hex}$ ... $7F_{hex}$] | $00_{hex}$ | 24 |
| Prescale FM/AM | 00 0E | [15:8] | [$00_{hex}$ ... $7F_{hex}$] | $00_{hex}$ | 23 |
| FM matrix | | [7:0] | [NO_MAT, GSTERERO, KSTEREO] | NO_MAT | 24 |
| Prescale NICAM | 00 10 | [15:8] | [$00_{hex}$ ... $7F_{hex}$] (MSP 3417G, MSP 3457G only) | $00_{hex}$ | 24 |
| ACB : SCART Switches a. D_CTR_I/O | 00 13 | [15:0] | Bits[15:0] | $00_{hex}$ | 28 |
| Beeper | 00 14 | [15:0] | [$00_{hex}$ ... $7F_{hex}$]/[$00_{hex}$ ... $7F_{hex}$] | 0/0 | 28 |
| Automatic Volume Correction | 00 29 | [15:8] | [off, on, decay time] | off | 27 |

**Table 3–6:** List of MSP 34x7G Read Registers

| Read Register | Address (hex) | Bits | Description and Adjustable Range | See Page |
|---|---|---|---|---|
| **$I^2C$ Sub-Address = $11_{hex}$ ; Registers are *not* writable** | | | | |
| STANDARD RESULT | 00 7E | [15:0] | Result of Automatic Standard Detection (see Table 3–8) | 22 |
| STATUS | 02 00 | [15:0] | Monitoring of internal settings e.g. Stereo, Mono, Mute etc. | 22 |
| **$I^2C$ Sub-Address = $13_{hex}$ ; Registers are *not* writable** | | | | |
| Quasi-peak readout left | 00 19 | [15:0] | [$00_{hex}$ ... $7FFF_{hex}$] 16 bit two's complement | 29 |
| Quasi-peak readout right | 00 1A | [15:0] | [$00_{hex}$ ... $7FFF_{hex}$] 16 bit two's complement | 29 |
| MSP hardware version code | 00 1E | [15:8] | [$00_{hex}$ ... $FF_{hex}$] | 29 |
| MSP major revision code | | [7:0] | [$00_{hex}$ ... $FF_{hex}$] | 29 |
| MSP product code | 00 1F | [15:8] | [$00_{hex}$ ... $FF_{hex}$] | 29 |
| MSP ROM version code | | [7:0] | [$00_{hex}$ ... $FF_{hex}$] | 29 |

### 3.3.2. Description of User Registers

**Table 3–7:** Standard Codes for STANDARD SELECT register

| MSP Standard Code (Data in hex) | TV Sound Standard | Sound Carrier Frequencies in MHz | MSP 34x7G Version |
|---|---|---|---|
| **Automatic Standard Detection** | | | |
| 00 01 | Starts Automatic Standard Detection and sets detected standard | | all |
| **Standard Selection** | | | |
| 00 02 | M-Dual FM-Stereo | 4.5/4.724212 | 3407, -17, -27, -47, -57 |
| 00 03 | B/G-Dual FM-Stereo[1)] | 5.5/5.7421875 | 3407, -17, -57 |
| 00 04 | D/K1-Dual FM-Stereo[2)] | 6.5/6.2578125 | |
| 00 05 | D/K2-Dual FM-Stereo[2)] | 6.5/6.7421875 | |
| 00 06 | D/K -FM-Mono with HDEV3[3)], not detectable by Automatic Standard Detection, for China<br>HDEV3[3)] SAT-Mono (i.e. Eutelsat, s. Table 6–18) | 6.5 | |
| 00 07 | D/K3-Dual FM-Stereo | 6.5/5.7421875 | |
| 00 08 | B/G-NICAM-FM[1)] | 5.5/5.85 | 3417, -57 |
| 00 09 | L-NICAM-AM | 6.5/5.85 | |
| 00 0A | I-NICAM-FM | 6.0/6.552 | |
| 00 0B | D/K-NICAM-FM[2)] | 6.5/5.85 | |
| 00 0C | D/K-NICAM-FM with HDEV2[4)], not detectable by Automatic Standard Detection, for China | 6.5/5.85 | |
| 00 0D | D/K-NICAM-FM with HDEV3[3)], not detectable by Automatic Standard Detection, for China | 6.5/5.85 | |
| 00 20 | BTSC-Stereo | 4.5 | 3427, -47, -57 |
| 00 21 | BTSC-Mono + SAP | | |
| 00 30 | M-EIA-J Japan Stereo | 4.5 | 3427, -47, -57 |
| 00 40 | FM-Stereo Radio with 75 µs Deemphasis | 10.7 | 3427, -47, -57 |
| 00 50 | SAT-Mono (see Table 6–18) | 6.5 | 3407, -17, -57 |
| 00 51 | SAT-Stereo (see Table 6–18) | 7.02/7.20 | |

[1)] In case of Automatic Sound Select, the B/G-codes $3_{hex}$ and $8_{hex}$ are equivalent.
[2)] In case of Automatic Sound Select, the D/K-codes $4_{hex}$, $5_{hex}$, $7_{hex}$, and $B_{hex}$ are equivalent.
[3)] HDEV3: Max. FM deviation must not exceed 540 kHz
[4)] HDEV2: Max. FM deviation must not exceed 360 kHz

#### 3.3.2.1. STANDARD SELECT Register

The TV sound standard of the MSP 34x7G demodulator is determined by the STANDARD SELECT register. There are two ways to use the STANDARD SELECT register:

– Setting up the demodulator for a TV sound standard by sending the corresponding standard code with a single $I^2C$ bus transmission.

– Starting the Automatic Standard Detection for terrestrial TV standards. This is the most comfortable way to set up the demodulator. Within 0.5 s, the detection and setup of the actual TV sound standard is performed. The detected standard can be read out of the STANDARD RESULT register by the control processor. This feature is recommended for the primary setup of a TV set. Outputs should be muted during Automatic Standard Detection.

The Standard Codes are listed in Table 3–7.

Selecting a TV sound standard via the STANDARD SELECT register initializes the demodulator. This includes: AGC-settings and carrier mute, tuning frequencies, FIR-filter settings, demodulation mode (FM, AM, NICAM), deemphasis and identification mode.

TV stereo sound standards that are unavailable for a specific MSP version are processed in analog mono sound of the standard. In that case, stereo or bilingual processing will not be possible.

For a complete setup of the TV sound processing from analog IF input to the source selection, the transmissions as shown in Section 3.5. are necessary.

For reasons of software compatibility to the MSP 34x7D, a Manual/Compatibility mode is available. A detailed description of this mode can be found on page 61.

#### 3.3.2.2. Refresh of STANDARD SELECT Register

A general refresh of the STANDARD SELECT register is not allowed. However, the following method enables watching the MSP 34x7G “alive” status and detection of accidental resets (only versions B6 and later):

– After Power-on, bit[15] of CONTROL will be set; it must be read once to enable the reset-detection feature.

– Reading of the CONTROL register and checking the reset indicator bit[15] .

– If bit[15] is “0”, any refresh of the STANDARD SELECT register **is not allowed.**

– If bit[15] is “1”, indicating a reset, a refresh of the STANDARD SELECT register and all other MSPG registers is required.

#### 3.3.2.3. STANDARD RESULT Register

If Automatic Standard Detection is selected in the STANDARD SELECT register, status and result of the Automatic Standard Detection process can be read out of the STANDARD RESULT register. The possible results are based on the mentioned Standard Code and are listed in Table 3–8.

In cases where no sound standard has been detected (no standard present, too much noise, strong interferers, etc.) the STANDARD RESULT register contains $00\ 00_{hex}$. In that case, the controller has to start further actions (for example set the standard according to a preference list or by manual input).

As long as the STANDARD RESULT register contains a value greater than $07\ FF_{hex}$, the Automatic Standard Detection is still active. During this period, the MODUS and STANDARD SELECT register must not be written. The STATUS register will be updated when the Automatic Standard Detection has finished.

If a present sound standard is unavailable for a specific MSP-version, it detects and switches to the analog mono sound of this standard.

Example:
The MSPs 3427G and 3447G will detect a B/G-NICAM signal as standard 3 and will switch to the analog FM-Mono sound.

**Table 3–8:** Results of the Automatic Standard Detection

| **Broadcasted Sound Standard** | **STANDARD RESULT Register** Read $007E_{hex}$ |
|---|---|
| Automatic Standard Detection could not find a sound standard | $0000_{hex}$ |
| B/G-FM | $0003_{hex}$ |
| B/G-NICAM | $0008_{hex}$ |
| I | $000A_{hex}$ |
| FM-Radio | $0040_{hex}$ |
| M-Korea<br>M-Japan<br>M-BTSC | $0002_{hex}$ (if MODUS[14,13]=00) |
| | $0020_{hex}$ (if MODUS[14,13]=01) |
| | $0030_{hex}$ (if MODUS[14,13]=10) |
| L-AM<br>D/K1<br>D/K2<br>D/K3 | $0009_{hex}$ (if MODUS[12]=0) |
| | $0004_{hex}$ (if MODUS[12]=1) |
| L-NICAM<br>D/K-NICAM | $0009_{hex}$ (if MODUS[12]=0) |
| | $000B_{hex}$ (if MODUS[12]=1) |
| Automatic Standard Detection still active | $>07FF_{hex}$ |

### 3.3.2.4. Write Registers on $I^2C$ Subaddress $10_{hex}$

**Table 3–9:** Write registers on $I^2C$ subaddress $10_{hex}$

| Register Address | Function | Name |
|---|---|---|
| $00\ 20_{hex}$ | **STANDARD SELECTION Register**<br>Defines TV-Sound or FM-Radio Standard<br>bit[15:0] $00\ 01_{hex}$ start Automatic Standard Detection<br>$00\ 02_{hex}$ MSP Standard Codes (see Table 3–7)<br>...<br>$00\ 51_{hex}$ | STANDARD_SEL |
| $00\ 30_{hex}$ | **MODUS Register**<br>Preference in Automatic Standard Detection:<br>bit[15] 0 undefined, must be 0<br>bit[14:13] detected 4.5 MHz carrier is interpreted as:[1)]<br>0 standard M (Korea)<br>1 standard M (BTSC)<br>2 standard M (Japan)<br>3 chroma carrier (M/N standards are ignored)<br>bit[12] detected 6.5 MHz carrier is interpreted as:[1)]<br>0 standard L (SECAM)<br>1 standard D/K1, D/K2, D/K3, or D/K NICAM<br>General MSP 34x7G Options<br>bit[11:4] 0 undefined, must be 0<br>bit[3] state of digital output pins D_CTR_I/O_0 and _1<br>0 active: D_CTR_I/O_0 and _1 are output pins (can be set by means of the ACB register. see also: MODUS[1])<br>1 tristate: D_CTR_I/O_0 and _1 are input pins (level can be read out of STATUS[4,3])<br>bit[2] 0 undefined, must be 0<br>bit[1] 0/1 disable/enable STATUS change indication by means of the digital I/O pin D_CTR_I/O_1 Necessary condition: MODUS[3] = 0 (active)<br>bit[0] 0/1 off/on: Automatic Sound Select | MODUS |

[1)] Valid at the next start of Automatic Standard Detection.

### 3.3.2.5. Read Registers on $I^2C$ Subaddress $11_{hex}$

**Table 3–10:** Read Registers on $I^2C$ Subaddress $11_{hex}$

| Register Address | Function | Name |
|---|---|---|
| $00\ 7E_{hex}$ | **STANDARD RESULT Register**<br><br>Readback of the detected TV sound or FM-Radio Standard<br><br>bit[15:0] $00\ 00_{hex}$ Automatic Standard Detection could not find a sound standard<br>$00\ 02_{hex}$ MSP Standard Codes (see Table 3–8)<br>...<br>$00\ 40_{hex}$<br>$>07\ FF_{hex}$ Automatic Standard Detection still active | STANDARD_RES |
| $02\ 00_{hex}$ | **STATUS Register**<br><br>Contains all user relevant internal information about the status of the MSP<br><br>bit[15:10] undefined<br><br>bit[8] 0/1 “1” indicates bilingual sound mode or SAP present (internally evaluated from received analog or digital identification signals)<br><br>bit[7] 0/1 “1” indicates independent mono sound (only for NICAM)<br><br>bit[6] 0/1 mono/stereo indication (internally evaluated from received analog or digital identification signals)<br><br>bit[5,9] 00 analog sound standard (FM or AM) active<br>01 this pattern will not occur<br>10 digital sound (NICAM) available<br>11 bad reception condition of digital sound (NICAM) due to:<br>a. high error rate<br>b. unimplemented sound code<br>c. data transmission only<br><br>bit[4] 0/1 low/high level of digital I/O pin D_CTR_I/O_1<br><br>bit[3] 0/1 low/high level of digital I/O pin D_CTR_I/O_0<br><br>bit[2] 0 detected secondary carrier (2nd A2 or SAP sub-carrier)<br>1 no secondary carrier detected<br><br>bit[1] 0 detected primary carrier (Mono or MPX carrier)<br>1 no primary carrier detected<br><br>bit[0] undefined<br><br>If STATUS change indication is activated by means of MODUS[1]: Each change in the STATUS register sets the digital I/O pin D_CTR_I/O_1 to high level. Reading the STATUS register resets D_CTR_I/O_1. | STATUS |

### 3.3.2.6. Write Registers on $I^2C$ Subaddress $12_{hex}$

**Table 3–11:** Write Registers on $I^2C$ Subaddress $12_{hex}$

| Register Address | Function | Name |
|---|---|---|
| **PREPROCESSING** | | |
| 00 $0E_{hex}$ | **FM/AM Prescale**<br>bit[15:8] $00_{hex}$ Defines the input prescale gain for the demodulated<br>... FM or AM signal<br>$7F_{hex}$<br>$00_{hex}$ off (RESET condition)<br>For all FM modes except satellite FM and AM-mode, the combinations of prescale value and FM deviation listed below lead to internal full scale.<br>FM mode<br>bit[15:8] $7F_{hex}$ 28 kHz FM deviation<br>$48_{hex}$ 50 kHz FM deviation<br>$30_{hex}$ 75 kHz FM deviation<br>$24_{hex}$ 100 kHz FM deviation<br>$18_{hex}$ 150 kHz FM deviation<br>$13_{hex}$ 180 kHz FM deviation (limit)<br>FM high deviation mode (HDEV2, MSP Standard Code = $C_{hex}$)<br>bit[15:8] $30_{hex}$ 150 kHz FM deviation<br>$14_{hex}$ 360 kHz FM deviation (limit)<br>FM very high deviation mode (HDEV3, MSP Standard Code = $6_{hex}$ and $D_{hex}$)<br>bit[15:8] $20_{hex}$ 450 kHz FM deviation<br>$1A_{hex}$ 540 kHz FM deviation (limit)<br>Satellite FM with adaptive deemphasis<br>bit[15:8] $10_{hex}$ recommendation<br>AM mode (MSP Standard Code = $9_{hex}$)<br>bit[15:8] $7C_{hex}$ recommendation for SIF input levels from 0.1 $V_{pp}$ to 0.8 $V_{pp}$<br>(Due to the AGC being switched on, the AM-output level remains stable and independent of the actual SIF-level in the mentioned input range) | PRE_FM |

**Table 3–11:** Write Registers on $I^2C$ Subaddress $12_{hex}$, continued

| Register Address | Function | Name |
|---|---|---|
| (continued)<br><br>00 $0E_{hex}$ | **FM Matrix Modes**<br><br>Defines the dematrix function for the demodulated FM signal<br><br>bit[7:0] $00_{hex}$ no matrix (used for bilingual and unmatrixed stereo sound)<br>$01_{hex}$ German stereo (Standard B/G)<br>$02_{hex}$ Korean stereo (also used for BTSC, EIA-J and FM Radio)<br>$03_{hex}$ sound A mono (left and right channel contain the mono sound of the FM/AM mono carrier)<br>$04_{hex}$ sound B mono<br><br>In case of **Automatic Sound Select = on**, the FM Matrix Mode is set automatically. Writing to the FM/AM prescale register (00 $0E_{hex}$ high part) is still allowed. In order not to disturb the automatic process, the low part of any $I^2C$ transmission to this register is ignored. Therefore, any FM-Matrix readback values may differ from data written previously.<br><br>In case of **Automatic Sound Select = off**, the FM Matrix Mode must be set as shown in Table 6–17 of Appendix B.<br><br>To enable a **Forced Mono Mode** set A2 THRESHOLD as described in Section 6.3.2.on page 65 | FM_MATRIX |
| 00 $10_{hex}$ | **NICAM Prescale**<br><br>Defines the input prescale value for the digital NICAM signal<br><br>bit[15:8] $00_{hex}$ ... $7F_{hex}$ prescale gain<br><br>examples:<br>$00_{hex}$ off<br>$20_{hex}$ 0 dB gain<br>$5A_{hex}$ 9 dB gain (recommendation)<br>$7F_{hex}$ +12 dB gain (maximum gain) | PRE_NICAM |
| 00 $0D_{hex}$ | **SCART Input Prescale**<br><br>Defines the input prescale value for the analog SCART input signal<br><br>bit[15:8] $00_{hex}$ ... $7F_{hex}$ prescale gain<br><br>examples:<br>$00_{hex}$ off (RESET condition)<br>$19_{hex}$ 0 dB gain (2 $V_{RMS}$ input leads to digital full scale)<br>$7F_{hex}$ +14 dB gain (400 $mV_{RMS}$ input leads to digital full scale) | PRE_SCART |

**Table 3–11:** Write Registers on $I^2C$ Subaddress $12_{hex}$, continued

| Register Address | Function | Name |
|---|---|---|
| **SOURCE SELECT AND OUTPUT CHANNEL MATRIX** | | |
| 00 $08_{hex}$<br>00 $0A_{hex}$<br>00 $0C_{hex}$ | **Source for:**<br>**Loudspeaker Output**<br>**SCART1 DA Output**<br>**Quasi-Peak Detector**<br><br>bit[15:8] 0 “FM/AM”: demodulated FM or AM mono signal<br>1 “Stereo or A/B”: demodulator Stereo or A/B signal (in manual mode, this source is identical to the NICAM source in the MSP 3417D)<br>3 “Stereo or A”: demodulator Stereo Sound or Language A (only defined for Automatic Sound Select)<br>4 “Stereo or B”: demodulator Stereo Sound or Language B (only defined for Automatic Sound Select)<br>2 SCART input<br>For demodulator sources, see Table 2–2. | SRC_MAIN<br>SRC_SCART1<br>SRC_QPEAK |
| 00 $08_{hex}$<br>00 $0A_{hex}$<br>00 $0C_{hex}$ | **Matrix Mode for:**<br>**Loudspeaker Output**<br>**SCART1 DA Output**<br>**Quasi-Peak Detector**<br><br>bit[7:0] $00_{hex}$ Sound A Mono (or Left Mono) (RESET condition)<br>$10_{hex}$ Sound B Mono (or Right Mono)<br>$20_{hex}$ Stereo (transparent mode)<br>$30_{hex}$ Mono (sum of left and right inputs divided by 2)<br>special modes are available (see Section 6.5.1. on page 73)<br><br>In Automatic Sound Select mode, the demodulator source channels are set according to Table 2–2. Therefore, the matrix modes of the corresponding output channels should be set to “Stereo” (transparent). | MAT_MAIN<br>MAT_SCART1<br>MAT_QPEAK |

**Table 3–11:** Write Registers on $I^2C$ Subaddress $12_{hex}$, continued

| Register Address | Function | Name |
|---|---|---|
| **LOUDSPEAKER PROCESSING** | | |
| 00 $00_{hex}$ | **Volume Loudspeaker**<br><br>bit[15:8] volume table with 1 dB step size<br>$7F_{hex}$ +12 dB (maximum volume)<br>$7E_{hex}$ +11 dB<br>...<br>$74_{hex}$ +1 dB<br>$73_{hex}$ 0 dB<br>$72_{hex}$ –1 dB<br>...<br>$02_{hex}$ –113 dB<br>$01_{hex}$ –114 dB<br>$00_{hex}$ Mute (RESET condition)<br>$FF_{hex}$ Fast Mute (needs about 75 ms until the signal is completely ramped down)<br><br>bit[7:5] higher resolution volume table<br>0 +0 dB<br>1 +0.125 dB increase in addition to the volume table<br>...<br>7 +0.875 dB increase in addition to the volume table<br><br>bit[4] 0 must be set to 0<br><br>bit[3:0] clipping mode<br>0 reduce volume<br>1 reduce tone control<br>2 compromise<br>3 dynamic<br><br>With large scale input signals, positive volume settings may lead to signal clipping.<br><br>The MSP 34x7G loudspeaker and headphone volume function is divided into a digital and an analog section. With Fast Mute, volume is reduced to mute position by digital volume only. Analog volume is not changed. This reduces any audible DC plops. To turn volume on again, the volume step that has been used before Fast Mute was activated must be transmitted.<br><br>If the clipping mode is set to “**reduce volume**”, the following rule is used: To prevent severe clipping effects with bass, treble, or equalizer boosts, the internal volume is automatically limited to a level where, in combination with either bass, treble, or equalizer setting, the amplification does not exceed 12 dB.<br><br>If the clipping mode is “**reduce tone control**”, the bass or treble value is reduced if amplification exceeds 12 dB. If the equalizer is switched on, the gain of those bands is reduced, where amplification together with volume exceeds 12 dB.<br><br>If the clipping mode is “**compromise**”**,** the bass or treble value and volume are reduced half and half if amplification exceeds 12 dB. If the equalizer is switched on, the gain of those bands is reduced half and half, where amplification together with volume exceeds 12 dB.<br><br>If the clipping mode is “**dynamic**”, volume is reduced automatically if the signal amplitudes would exceed –2 dBFS within the IC. | VOL_MAIN |

**Table 3–11:** Write Registers on I$^2$C Subaddress $12_{hex}$, continued

| Register Address | Function | Name |
|---|---|---|
| 00 $29_{hex}$ | **Automatic Volume Correction (AVC) Loudspeaker Channel**<br><br>bit[15:12] $00_{hex}$ AVC off (and reset internal variables)<br>$08_{hex}$ AVC on<br><br>bit[11:8] $08_{hex}$ 8 sec decay time<br>$04_{hex}$ 4 sec decay time (recommended)<br>$02_{hex}$ 2 sec decay time<br>$01_{hex}$ 20 ms decay time (should be used for approx. 100 ms after channel change) | <br><br>AVC<br><br><br>AVC_DECAY |
| **SCART OUTPUT CHANNEL** | | |
| 00 $07_{hex}$ | **Volume SCART1 Output Channel**<br><br>bit[15:8] volume table with 1 dB step size<br>$7F_{hex}$ +12 dB (maximum volume)<br>$7E_{hex}$ +11 dB<br>...<br>$74_{hex}$ +1 dB<br>$73_{hex}$ 0 dB<br>$72_{hex}$ –1 dB<br>...<br>$02_{hex}$ –113 dB<br>$01_{hex}$ –114 dB<br>$00_{hex}$ Mute (RESET condition)<br><br>bit[7:5] higher resolution volume table<br>0 +0 dB<br>1 +0.125 dB increase in addition to the volume table<br>...<br>7 +0.875 dB increase in addition to the volume table<br><br>bit[4:0] $01_{hex}$ this must be $01_{hex}$ | VOL_SCART1 |

**Table 3–11:** Write Registers on $I^2C$ Subaddress $12_{hex}$, continued

| Register Address | Function | Name |
|---|---|---|
| **SCART SWITCHES AND DIGITAL I/O PINS** | | |
| 00 $13_{hex}$ | **ACB Register**<br><br>Defines the level of the digital output pins and the position of the SCART switches<br>bit[15] 0/1 low/high of digital output pin D_CTR_I/O_1 (MODUS[3]=0)<br>bit[14] 0/1 low/high of digital output pin D_CTR_I/O_0 (MODUS[3]=0)<br>bit[13:5] SCART DSP Input Select<br>xxxx00xx0 SCART1 to DSP input (RESET position)<br>xxxx01xx0 MONO to DSP input (Sound A Mono must be selected in the channel matrix mode for the corresponding output channels)<br>xxxx11xx1 mute DSP input<br>bit[13:5] SCART1 Output Select<br>xx00xxx0x undefined (RESET position)<br>xx10xxx0x MONO input to SCART1 output<br>xx11xxx0x SCART1 DA to SCART1 output<br>xx01xxx1x SCART1 input to SCART1 output<br>xx11xxx1x mute SCART1 output<br><br>The RESET position becomes active at the time of the first write transmission on the control bus to the audio processing part. By writing to the ACB register first, the RESET state can be redefined. | ACB_REG |
| **BEEPER** | | |
| 00 $14_{hex}$ | **Beeper Volume and Frequency**<br><br>bit[15:8] Beeper Volume<br>$00_{hex}$ off<br>$7F_{hex}$ maximum volume<br>bit[7:0] Beeper Frequency<br>$01_{hex}$ 16 Hz (lowest)<br>$40_{hex}$ 1 kHz<br>$FF_{hex}$ 4 kHz | BEEPER |

### 3.3.2.7. Read Registers on $I^2C$ Subaddress $13_{hex}$

**Table 3–12:** Read Registers on $I^2C$ Subaddress $13_{hex}$

| Register Address | Function | Name |
|---|---|---|
| **QUASI-PEAK DETECTOR READOUT** | | |
| 00 $19_{hex}$<br>00 $1A_{hex}$ | **Quasi-Peak Detector Readout Left**<br>**Quasi-Peak Detector Readout Right**<br><br>bit[15:0] $0_{hex}$ ... $7FFF_{hex}$ values are 16 bit two's complement (only positive) | QPEAK_L<br>QPEAK_R |
| **MSP 34x7G VERSION READOUT REGISTERS** | | |
| 00 $1E_{hex}$ | **MSP Hardware Version Code**<br><br>bit[15:8] $02_{hex}$ MSP 34x7G - B8<br>A change in the hardware version code defines hardware optimizations that may have influence on the chip's behavior. The readout of this register is identical to the hardware version code in the chip's imprint.<br><br>**MSP Major Revision Code**<br><br>bit[7:0] $07_{hex}$ MSP 34x7G - B8 | MSP_HARD<br><br><br><br><br><br>MSP_REVISION |
| 00 $1F_{hex}$ | **MSP Product Code**<br><br>bit[15:8] $07_{hex}$ MSP 3407G - B8<br>$11_{hex}$ MSP 3417G - B8<br>$1B_{hex}$ MSP 3427G - B8<br>$2F_{hex}$ MSP 3447G - B8<br>$39_{hex}$ MSP 3457G - B8<br>$43_{hex}$ MSP 3467G - B8<br>By means of the MSP product code, the control processor is able to decide which TV sound standards have to be considered.<br><br>**MSP ROM Version Code**<br><br>bit[7:0] $46_{hex}$ MSP 34x7G - B6<br>$48_{hex}$ MSP 34x7G - B8<br>A change in the ROM version code defines internal software optimizations, that may have influence on the chip's behavior, e.g. new features may have been included. While a software change is intended to create no compatibility problems, customers that want to use the new functions can identify new MSP 34x7G versions according to this number.<br>To avoid compatibility problems with MSP 3410B and MSP 34x7D, an offset of $40_{hex}$ is added to the ROM version code of the chip's imprint. | MSP_PRODUCT<br><br><br><br><br><br><br><br><br><br><br><br><br>MSP_ROM |

### 3.4. Programming Tips

This section describes the preferred method for initializing the MSP 34x7G. The initialization is grouped into three sections:

– SCART Signal Path (analog signal path)

– Demodulator

– Output Channels

See Fig. 2–1 on page 8 for a complete signal flow.

#### SCART Signal Path

1. Select analog input for the SCART baseband processing (SCART DSP Input Select) by means of the ACB register.

2. Set preferred prescale for SCART.

3. Select the source for the analog SCART output by means of the ACB register.

#### Demodulator

For a complete setup of the TV sound processing from analog IF input to the source selection, the following steps must be performed:

1. Set MODUS register to the preferred mode and Sound IF input.

2. Set preferred prescale (FM and NICAM) values.

3. Write STANDARD SELECT register.

4. If Automatic Sound Select is not active:
   Choose FM matrix repeatedly according to the sound mode indicated in the STATUS register.

#### Output Channels

1. Select the source channel and matrix for each output channel.

2. Select volume for each output channel.

### 3.5. Examples of Minimum Initialization Codes

Initialization of the MSP 34x7G according to these listings reproduces sound of the selected standard on the loudspeaker output. All numbers are hexadecimal. The examples have the following structure:

1. Perform an $I^2C$ controlled reset of the IC.

2. Write MODUS register
   (with Automatic Sound Select).

3. Set Source Selection for loudspeaker channel
   (with matrix set to STEREO).

4. Set Prescale
   (FM and/or NICAM and dummy FM matrix).

5. Write STANDARD SELECT register.

6. Set Volume loudspeaker channel to 0 dB.

#### 3.5.1. B/G-FM (A2 or NICAM)

| | |
|---|---|
| *<80 00 80 00>* | // Softreset |
| *<80 00 00 00>* | |
| *<80 10 00 30 20 03>* | // MODUS-Register: Automatic = on |
| *<80 12 00 08 03 20>* | // Source Sel. = (St or A) & Ch. Matr. = St |
| *<80 12 00 0E 24 03>* | // FM/AM-Prescale = $24_{hex}$, FM-Matrix = MONO/SOUNDA |
| *<80 12 00 10 5A 00>* | // NICAM-Prescale = $5A_{hex}$ |
| *<80 10 00 20 00 03>* | // Standard Select: A2 B/G or NICAM B/G |
| ***or*** | |
| *<80 10 00 20 00 08>* | |
| *<80 12 00 00 73 00>* | // Loudspeaker Volume 0 dB |

#### 3.5.2. BTSC-Stereo

| | |
|---|---|
| *<80 00 80 00>* | // Softreset |
| *<80 00 00 00>* | |
| *<80 10 00 30 20 03>* | // MODUS-Register: Automatic = on |
| *<80 12 00 08 03 20>* | // Source Sel. = (St or A) & Ch. Matr. = St |
| *<80 12 00 0E 24 03>* | // FM/AM-Prescale = $24_{hex}$, FM-Matrix = Sound A Mono |
| *<80 10 00 20 00 20>* | // Standard Select: BTSC-STEREO |
| *<80 12 00 00 73 00>* | // Loudspeaker Volume 0 dB |

#### 3.5.3. BTSC-SAP with SAP at Loudspeaker Channel

| | |
|---|---|
| *<80 00 80 00>* | // Softreset |
| *<80 00 00 00>* | |
| *<80 10 00 30 20 03>* | // MODUS-Register: Automatic = on |
| *<80 12 00 08 03 20>* | // Source Sel. = (St or A) & Ch. Matr. = St |
| *<80 12 00 0E 24 03>* | // FM/AM-Prescale = $24_{hex}$, FM-Matrix = Sound A Mono |
| *<80 10 00 20 00 21>* | // Standard Select: BTSC-SAP |
| *<80 12 00 00 73 00>* | // Loudspeaker Volume 0 dB |

### 3.5.4. FM-Stereo Radio

*<80 00 80 00>* // Softreset

*<80 00 00 00>*

*<80 10 00 30 20 03>* // MODUS-Register: Automatic = on

*<80 12 00 08 03 20>* // Source Sel. = (St or A) & Ch. Matr. = St

*<80 12 00 0E 24 03>* // FM/AM-Prescale = $24_{hex}$,
FM-Matrix = Sound A Mono

*<80 10 00 20 00 40>* // Standard Select: FM-STEREO-RADIO

*<80 12 00 00 73 00>* // Loudspeaker Volume 0 dB

### 3.5.5. Automatic Standard Detection

A detailed software flow diagram is shown in Fig. 3–2 on page 32.

*<80 00 80 00>* // Softreset

*<80 00 00 00>*

*<80 10 00 30 20 03>* // MODUS-Register: Automatic = on

*<80 12 00 08 03 20>* // Source Sel. = (St or A) & Ch. Matr. = St

*<80 12 00 0E 24 03>* // FM/AM-Prescale = $24_{hex}$,
FM-Matrix = Sound A Mono

*<80 12 00 10 5A 00>* // NICAM-Prescale = $5A_{hex}$

*<80 10 00 20 00 01>* // Standard Select:
Automatic Standard Detection

// Wait till STANDARD RESULT contains a value ≤ 07FF

// IF STANDARD RESULT contains 0000

// do some error handling

// ELSE

*<80 12 00 00 73 00>* // Loudspeaker Volume 0 dB

### 3.5.6. Software Flow for Interrupt driven STATUS Check

A detailed software flow diagram is shown in Fig. 3–2 on page 32.

If the D_CTR_I/O_1 pin of the MSP 34x7G is connected to an interrupt input pin of the controller, the following interrupt handler can be applied to be automatically called with each status change of the MSP 34x7G. The interrupt handler may adjust the TV display according to the new status information.

Interrupt Handler:

*<80 11 02 00 <81 dd dd>* // Read STATUS

// adjust TV-display with given status information

// Return from Interrupt

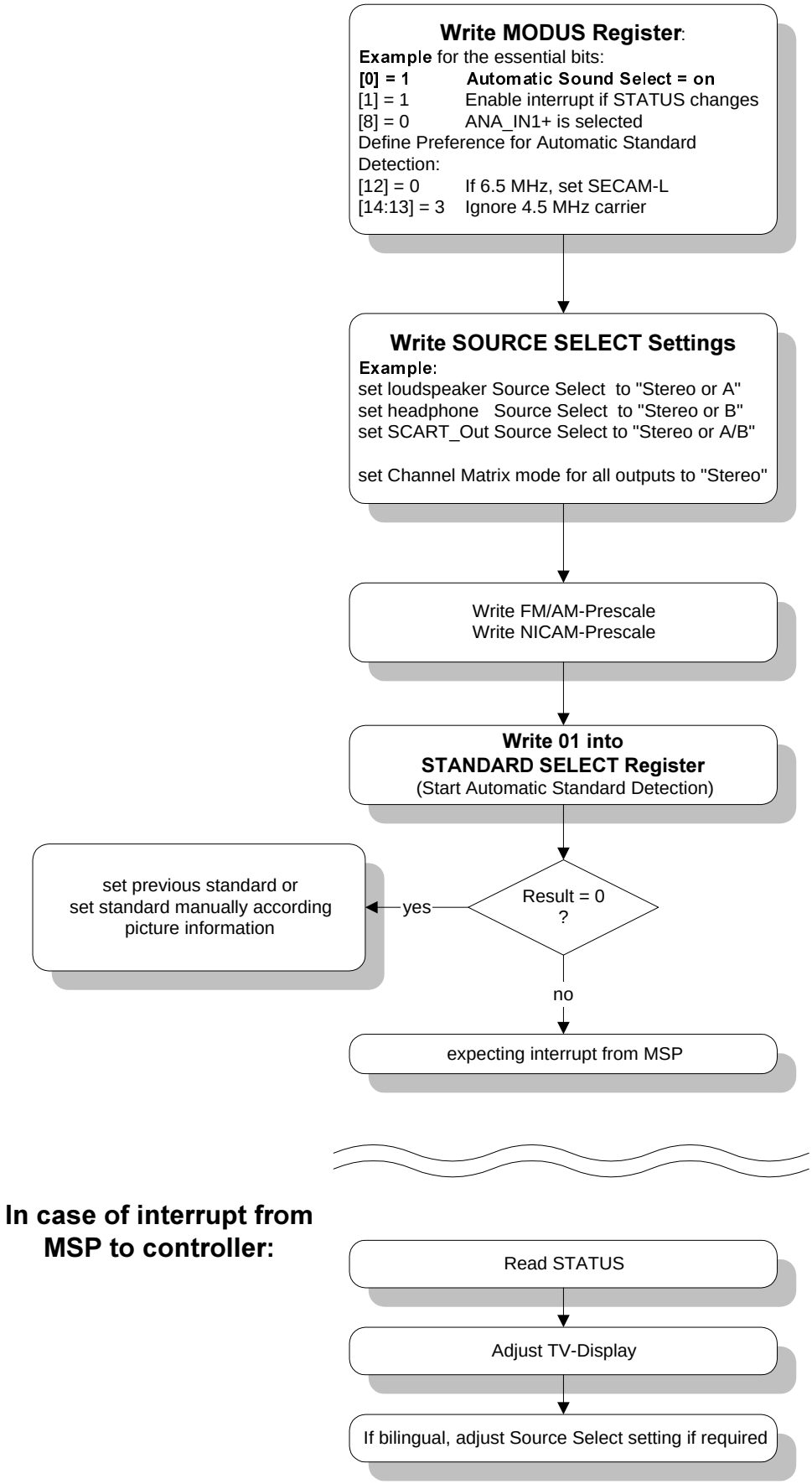



**Fig. 3–2:** Software flow diagram for a minimum demodulator setup for a European multistandard set applying the Automatic Sound Select feature

## 4. Specifications

### 4.1. Outline Dimensions

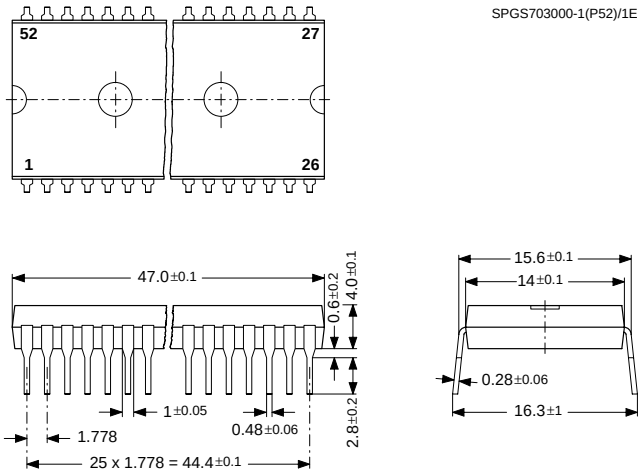



**Fig. 4–1:**
52-Pin Plastic Shrink Dual Inline Package
**(PSDIP52)**
Weight approximately 5.5 g
Dimensions in mm

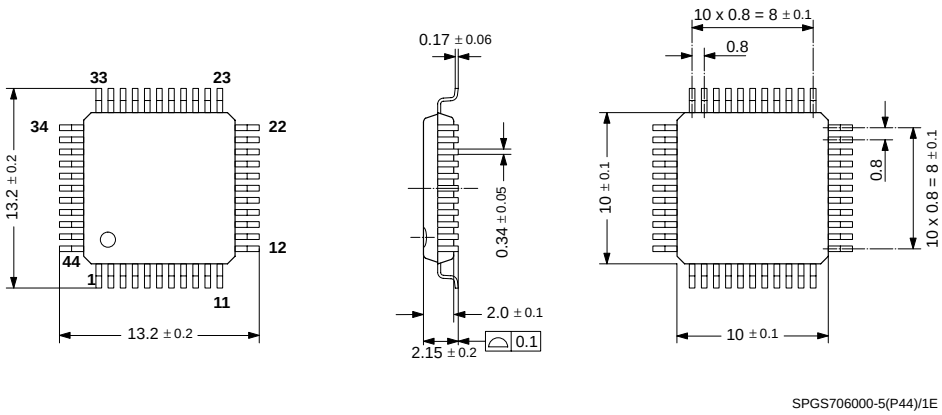



**Fig. 4–2:**
44-Pin Plastic Metric Quad Flat Pack
**(PMQFP44)**
Weight approximately 0.4 g
Dimensions in mm

### 4.2. Pin Connections and Short Descriptions

NC = not connected; leave vacant
LV = if not used, leave vacant
DVSS: if not used, connect to DVSS
X = obligatory; connect as described in circuit diagram
AHVSS: connect to AHVSS

| Pin No. PSDIP 52-pin | Pin No. PMQFP 44-pin | Pin Name | Type | Connection (if not used) | Short Description |
|---|---|---|---|---|---|
| 1 | 7 | TP | | LV | Test pin |
| 2 | – | NC | | LV | Not connected |
| 3 | 8 | D_CTR_I/O_1 | IN/OUT | LV | D_CTR_I/O_1 |
| 4 | 9 | D_CTR_I/O_0 | IN/OUT | LV | D_CTR_I/O_0 |
| 5 | 10 | ADR_SEL | IN | X | $I^2C$ Bus address select |
| 6 | 11 | STANDBYQ | IN | X | Standby (low-active) |
| 7 | 12 | I2C_CL | IN/OUT | X | $I^2C$ clock |
| 8 | 13 | I2C_DA | IN/OUT | X | $I^2C$ data |
| 9 | 14 | TP | | LV | Test pin |
| 10 | 15 | TP | | LV | Test pin |
| 11 | 16 | TP | | LV | Test pin |
| 12 | 17 | TP | | LV | Test pin |
| 13 | – | TP | | LV | Test pin |
| 14 | – | TP | | LV | Test pin |
| 15 | 18 | TP_CO | OUT | LV | Test pin[1)] |
| 16 | 19 | DVSUP | | X | Digital power supply +5 V |
| 17 | – | DVSS | | X | Digital ground |
| – | 20 | DVSS | | X | Digital ground |
| 18 | 21 | TP | | LV | Test pin |
| 19 | – | NC | | LV | Not connected |
| 20 | 22 | RESETQ | IN | X | Power-on-reset |
| 21 | 23 | NC | | LV | Not connected |
| 22 | 24 | NC | | LV | Not connected |
| 23 | 25 | VREF2 | | X | Reference ground 2 high-voltage part |
| 24 | 26 | DACM_R | OUT | LV | Loudspeaker out, right |

1) Use this pin to define the capacitor size at the crystal oscillator (see Section 4.6.2.4. on page 44).

| Pin No. PSDIP 52-pin | Pin No. PMQFP 44-pin | Pin Name | Type | Connection (if not used) | Short Description |
|---|---|---|---|---|---|
| 25 | 27 | DACM_L | OUT | LV | Loudspeaker out, left |
| 26 | – | NC | | LV | Not connected |
| 27 | – | NC | | LV | Not connected |
| 28 | 28 | NC | | LV | Not connected |
| 29 | 29 | VREF1 | | X | Reference ground 1 high-voltage part |
| 30 | 30 | SC1_OUT_R | OUT | LV | SCART 1 output, right |
| 31 | 31 | SC1_OUT_L | OUT | LV | SCART 1 output, left |
| 32 | 32 | NC | | LV | Not connected |
| 33 | 33 | AHVSUP | | X | Analog power supply +8.0 V |
| 34 | 34 | CAPL_M | | X | Volume capacitor MAIN |
| 35 | 35 | AHVSS | | X | Analog ground |
| 36 | 36 | AGNDC | | X | Analog reference voltage high-voltage part |
| 37 | – | NC | | LV | Not connected |
| 38 | – | NC | | LV | Not connected |
| 39 | 37 | NC | | LV | Not connected |
| 40 | 38 | NC | | LV | Not connected |
| – | 39 | NC | | LV | Not connected |
| 41 | 40 | SC1_IN_L | IN | LV | SCART 1 input, left |
| 42 | 41 | SC1_IN_R | IN | LV | SCART 1 input, right |
| 43 | 42 | VREFTOP | | X | Reference voltage IF A/D converter |
| 44 | 43 | MONO_IN | IN | LV | Mono input |
| 45 | 44 | AVSS | | X | Analog ground |
| 46 | 1 | AVSUP | | X | Analog power supply +5 V |
| 47 | 2 | ANA_IN1+ | IN | LV | IF input 1 |
| 48 | 3 | ANA_IN– | IN | LV | IF common |
| 49 | – | NC | | LV | Not connected |
| 50 | 4 | TESTEN | IN | X | Test pin |
| 51 | 5 | XTAL_IN | IN | X | Crystal oscillator |
| 52 | 6 | XTAL_OUT | OUT | X | Crystal oscillator |

### 4.3. Pin Descriptions

**NC** – Pin not connected

**I2C_CL** – $I^2C$ Clock Input/Output (Fig. 4–12)
Via this pin the $I^2C$ bus clock signal has to be supplied. The signal can be pulled down by the MSP in case of wait conditions.

**I2C_DA** – $I^2C$ Data Input/Output (Fig. 4–12)
Via this pin the $I^2C$ bus data is written to or read from the MSP.

**TP_CO** – Clock Output
Output of clock signal used in order to define capacitors at the crystal oscillator (see Section 4.6.2.4. on page 44).

**DVSUP*** – Digital Supply Voltage
Power supply for the digital circuitry of the MSP. Must be connected to a power supply.

**DVSS*** – Digital Ground
Ground connection for the digital circuitry of the MSP

**RESETQ** – Reset Input (Fig. 4–5)
In the steady state, high level is required. A low level resets the MSP 34x7G.

**VREF2** – Reference Ground 2
Reference analog ground. This pin must be connected separately to ground (AHVSS). VREF2 serves as a clean ground and should be used as the reference for analog connections to the loudspeaker outputs.

**DACM_R/L** – Loudspeaker Outputs (Fig. 4–15)
Output of the loudspeaker signal. A 1nF capacitor to AHVSS must be connected to these pins. The DC offset on these pins depends on the selected volume.

**VREF1** – Reference Ground 1
Reference analog ground. This pin must be connected separately to ground (AHVSS). VREF1 serves as a clean ground and should be used as the reference for analog connections to the SCART output.

**SC1_OUT_R/L** – SCART1 Outputs (Fig. 4–16)
Output of the SCART1 signal. Connections to these pins must use a 100 ohm series resistor and are intended to be AC coupled.

**AHVSUP*** – Analog Power Supply High Voltage
Power is supplied via this pin for the analog circuitry of the MSP (except IF input). This pin must be connected to the +8 V supply.

**CAPLM** – Volume Capacitor Loudspeakers (Fig. 4–18)
A 10µF capacitor to AHVSUP must be connected to this pin. It serves as smoothing filter for volume changes in order to suppress audible plops. The value of the capacitor can be lowered to 1µF if faster response is required. The area encircled by the trace lines should be minimized, keep traces as short as possible. This input is sensitive for magnetic induction.

**AHVSS*** – Ground for Analog Power Supply High Voltage
Ground connection for the analog circuitry of the MSP (except IF input).

**AGNDC** – Internal Analog Reference Voltage
This pin serves as the internal ground connection for the analog circuitry (except IF input). It must be connected to the VREF pins with a 3.3 µF and a 100 nF capacitor in parallel. This pins shows a DC level of typically 3.73 V.

**SC1_IN_L/R** – SCART1 Inputs (Fig. 4–8)
The analog input signal for SCART1 is fed to this pin. Analog input connection must be AC coupled.

**VREFTOP** – Reference Voltage IF AD Converter (Fig. 4–10)
Via this pin, the reference voltage for the IF AD converter is decoupled. It must be connected to AVSS pins with a 10µF and a 100nF capacitor in parallel. Traces must be kept short.

**MONO_IN** – Mono Input (Fig. 4–8)
The analog mono input signal is fed to this pin. Analog input connection must be AC coupled.

**AVSS*** – Ground for Analog Power Supply Voltage
Ground connection for the analog IF input circuitry of the MSP.

**AVSUP*** – Analog Power Supply Voltage
Power is supplied via this pin for the analog IF input circuitry of the MSP. This pin must be connected to the +5 V supply.

**ANA_IN1+** – IF Input 1 (Fig. 4–10)
The analog sound if signal is supplied to this pin. Inputs must be AC coupled. This pin is designed as symmetrical input: ANA_IN1+ is internally connected to one input of a symmetrical op amp, ANA_IN– to the other.

**ANA_IN**– – IF Common (Fig. 4–10)
This pin serves as a common reference for ANA_IN1+ input.

**TESTEN** – Test Enable Pin (Fig. 4–6)
This pin enables factory test modes. For normal operation it must be connected to ground.

**XTAL_IN, XTAL_OUT** – Crystal Input and Output Pins (Fig. 4–14)
These pins are connected to an 18.432 MHz crystal oscillator which is digitally tuned by integrated shunt capacitances. An external clock can be fed into XTAL_IN. External capacitors at each crystal pin to ground (AVSS) are required. It should be verified by layout, that no supply current for the digital circuitry is flowing through the ground connection point. To adjust capacitors see Crystal Recommendations on page 44.

**D_CTR_I/O_1/0** – Digital Control Input/Output Pins (Fig. 4–13)
General purpose input/output pins. Pin D_CTR_I/O_1 can be used as an interrupt request pin to the controller.

**ADR_SEL** – $I^2C$ Bus Address Select (Fig. 4–11)
This pin selects the device address for the MSP (see Table 3–1 on page 14).

**STANDBYQ** – Standby
In normal operation, this pin must be high. If the MSP 34x7G is switched to (**'Standby'-mode**), the SCART switches maintain their position and function (see Section 2.6.2.on page 13).

*** Application Note:**
All ground pins should be connected to one low-resistive ground plane. All supply pins should be connected separately with short and low-resistive lines to the power supply. Decoupling capacitors from DVSUP to DVSS, AVSUP to AVSS, and AHVSUP to AHVSS are recommended as closely as possible to these pins. Decoupling of DVSUP and DVSS is most important. We recommend using more than one capacitor. By choosing different values, the frequency range of active decoupling can be extended. In our application boards we use: 220 pF, 470 pF, 1.5 nF, and 10 µF. The capacitor with the lowest value should be placed nearest to the DVSUP and DVSS pins.

## 4.4. Pin Configurations

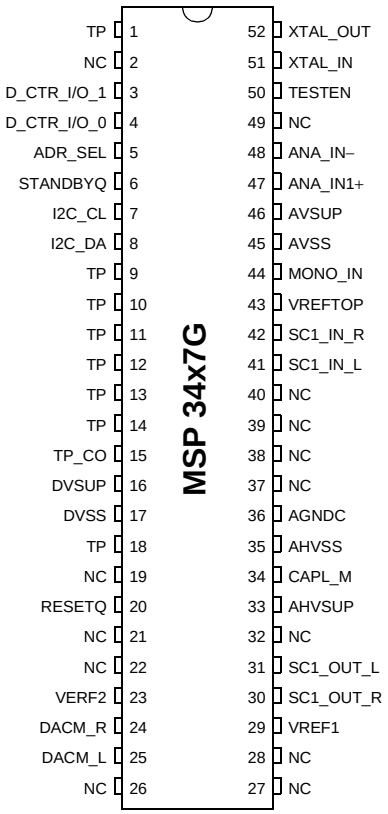



**Fig. 4–3:** PSDIP52 package

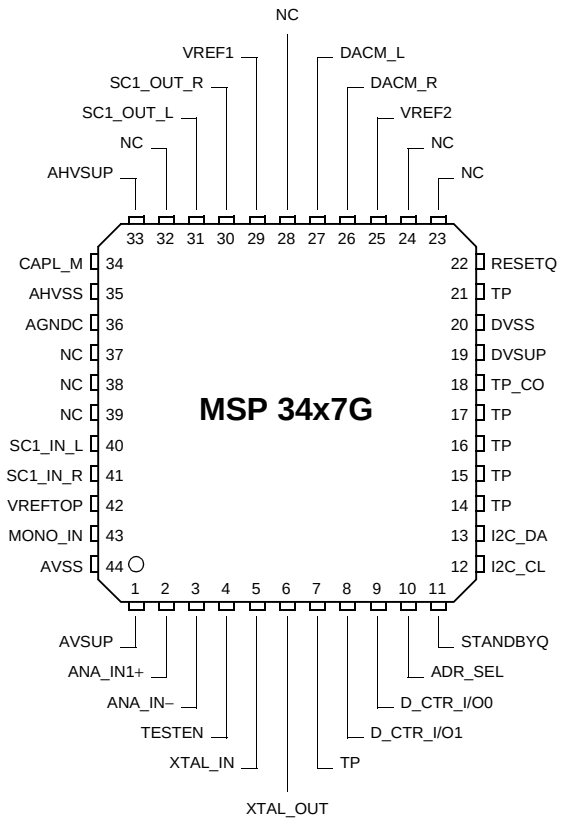



**Fig. 4–4:** PMQFP44 package

### 4.5. Pin Circuits

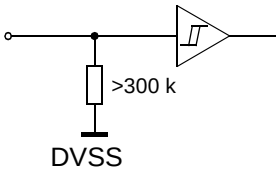



**Fig. 4–5:** Input Pin: **RESETQ**

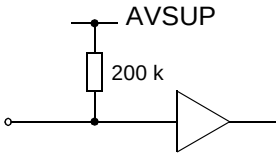



**Fig. 4–6:** Input Pin **TESTEN**

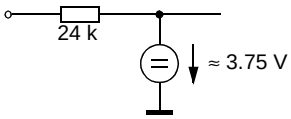



**Fig. 4–7:** Input Pin: **MONO_IN**

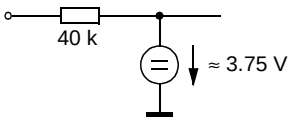



**Fig. 4–8:** Input Pins: **SC1_IN_L/R**

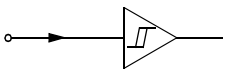


**Fig. 4–9:** Input Pin: **STANDBYQ**

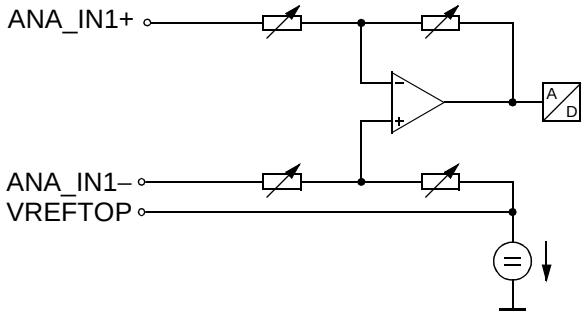



**Fig. 4–10:** Input Pins:
**VREFTOP, ANA_IN1+, ANA_IN–**

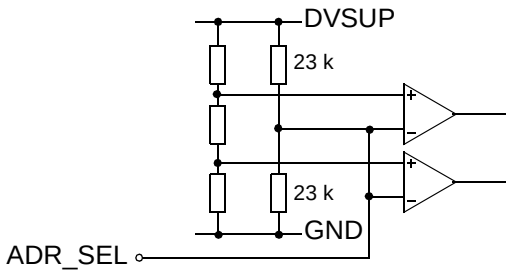



**Fig. 4–11:** Input Pin: **ADR_SEL**

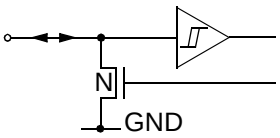



**Fig. 4–12:** Input/Output Pins: **I2C_CL, I2C_DA**

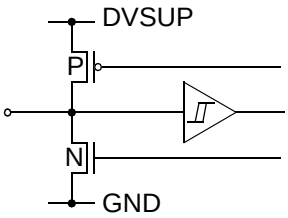



**Fig. 4–13:** Input/Output Pins:
**D_CTR_I/O_1, D_CTR_I/O_0**

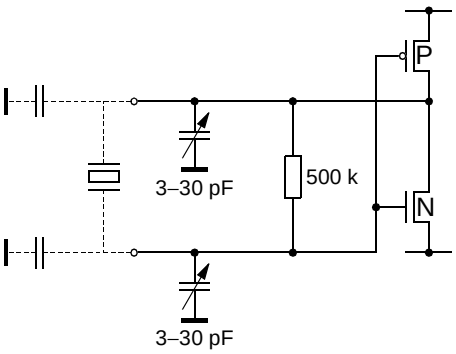



**Fig. 4–14:** Output/Input Pins: **XTAL_IN, XTAL_OUT**

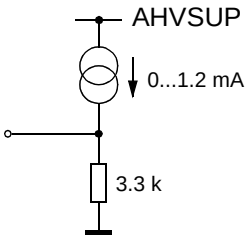



**Fig. 4–15:** Output Pins: **DACM_R/L**

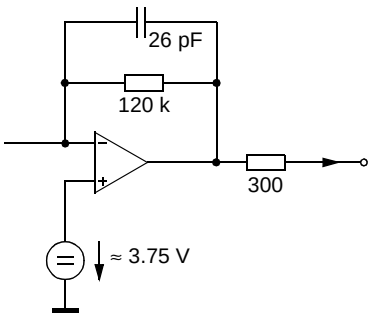



**Fig. 4–16:** Output Pins: **SC1_OUT_R/L**

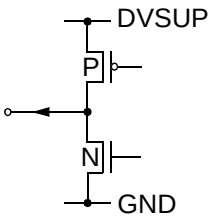



**Fig. 4–17:** Output Pin: **TP_CO**

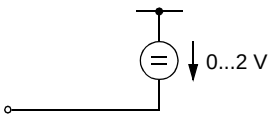



**Fig. 4–18:** Capacitor Pin: **CAPL_M**

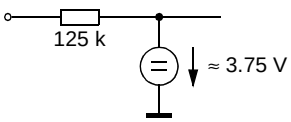



**Fig. 4–19: AGNDC**

## 4.6. Electrical Characteristics

### 4.6.1. Absolute Maximum Ratings

| Symbol | Parameter | Pin Name | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $T_A$ | Ambient Operating Temperature | – | 0 | 70 | °C |
| $T_S$ | Storage Temperature | – | –40 | 125 | °C |
| $V_{SUP1}$ | First Supply Voltage | AHVSUP | –0.3 | 9.0 | V |
| $V_{SUP2}$ | Second Supply Voltage | DVSUP | –0.3 | 6.0 | V |
| $V_{SUP3}$ | Third Supply Voltage | AVSUP | –0.3 | 6.0 | V |
| $dV_{SUP23}$ | Voltage between AVSUP and DVSUP | AVSUP, DVSUP | –0.5 | 0.5 | V |
| $P_{TOT}$ | Package Power Dissipation<br>PSDIP52<br>PMQFP44 | AHVSUP, DVSUP, AVSUP | | <br>1200<br>960 | <br>mW<br>mW |
| $V_{Idig}$ | Input Voltage, all Digital Inputs | | –0.3 | $V_{SUP2}$+0.3 | V |
| $I_{Idig}$ | Input Current, all Digital Pins | – | –20 | +20 | mA[1] |
| $V_{Iana}$ | Input Voltage, all Analog Inputs | SC1_IN_s,[2]<br>MONO_IN | –0.3 | $V_{SUP1}$+0.3 | V |
| $I_{Iana}$ | Input Current, all Analog Inputs | SC1_IN_s,[2]<br>MONO_IN | –5 | +5 | mA[1] |
| $I_{Oana}$ | Output Current, all SCART Outputs | SC1_OUT_s[2] | [3], [4] | [3], [4] | |
| $I_{Oana}$ | Output Current, all Analog Outputs except SCART Outputs | DACM_s[2] | [3] | [3] | |
| $I_{Cana}$ | Output Current, other pins connected to capacitors | CAPL_M, AGNDC | [3] | [3] | |

[1] positive value means current flowing into the circuit
[2] “s” means “L” or “R”
[3] The Analog Outputs are short-circuit proof with respect to First Supply Voltage and Ground.
[4] Total chip power dissipation must not exceed absolute maximum rating.

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

### 4.6.2. Recommended Operating Conditions

at $T_A$ = 0 to 70 °C

#### 4.6.2.1. General Recommended Operating Conditions

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{SUP1}$ | First Supply Voltage (AHVSUP = 8 V) | AHVSUP | 7.6 | 8.0 | 8.7 | V |
| | First Supply Voltage (AHVSUP = 5V) | | 4.75 | 5.0 | 5.25 | V |
| $V_{SUP2}$ | Second Supply Voltage | DVSUP | 4.75 | 5.0 | 5.25 | V |
| $V_{SUP3}$ | Third Supply Voltage | AVSUP | 4.75 | 5.0 | 5.25 | V |
| $t_{STBYQ1}$ | STANDBYQ Setup Time before Turn-off of Second Supply Voltage | STANDBYQ, DVSUP | 1 | | | µs |

#### 4.6.2.2. Analog Input and Output Recommendations

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{AGNDC}$ | AGNDC-Filter-Capacitor | AGNDC | –20% | 3.3 | | µF |
| | Ceramic Capacitor in Parallel | | –20% | 100 | | nF |
| $C_{inSC}$ | DC-Decoupling Capacitor in front of SCART Inputs | SC1_IN_s[1)] | –20% | 330 | | nF |
| $V_{inSC}$ | SCART Input Level | | | | 2.0 | $V_{RMS}$ |
| $V_{inMONO}$ | Input Level, Mono Input | MONO_IN | | | 2.0 | $V_{RMS}$ |
| $R_{LSC}$ | SCART Load Resistance | SC1_OUT_s[1)] | 10 | | | kΩ |
| $C_{LSC}$ | SCART Load Capacitance | | | | 6.0 | nF |
| $C_{VMA}$ | Main Volume Capacitor | CAPL_M | | 10 | | µF |
| $C_{FMA}$ | Main Filter Capacitor | DACM_s[1)] | –10% | 1 | +10% | nF |

1) “s” means “L” or “R”

#### 4.6.2.3. Recommendations for Analog Sound IF Input Signal

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{VREFTOP}$ | VREFTOP-Filter-Capacitor | VREFTOP | –20% | 10 | | µF |
| | Ceramic Capacitor in Parallel | | –20% | 100 | | nF |
| $F_{IF_FMTV}$ | Analog Input Frequency Range for TV applications | ANA_IN1+, ANA_IN– | 0 | | 9 | MHz |
| $F_{IF_FMRADIO}$ | Analog Input Frequency for FM-Radio Applications | | | 10.7 | | MHz |
| $V_{IF_FM}$ | Analog Input Range FM/NICAM | | 0.1 | 0.8 | 3 | $V_{pp}$ |
| $V_{IF_AM}$ | Analog Input Range AM/NICAM | | 0.1 | 0.45 | 0.8 | $V_{pp}$ |
| $R_{FMNI}$ | Ratio: NICAM Carrier/FM Carrier (unmodulated carriers)<br>BG:<br>I: | | <br><br>–20<br>–23 | <br><br>–7<br>–10 | <br><br>0<br>0 | <br><br>dB<br>dB |
| $R_{AMNI}$ | Ratio: NICAM Carrier/AM Carrier (unmodulated carriers) | | –25 | –11 | 0 | dB |
| $R_{FM}$ | Ratio: FM-Main/FM-Sub Satellite | | | 7 | | dB |
| $R_{FM1/FM2}$ | Ratio: FM1/FM2 German FM-System | | | 7 | | dB |
| $R_{FC}$ | Ratio: Main FM Carrier/ Color Carrier | | 15 | – | – | dB |
| $R_{FV}$ | Ratio: Main FM Carrier/ Luma Components | | 15 | – | – | dB |
| $PR_{IF}$ | Passband Ripple | | – | – | ±2 | dB |
| $SUP_{HF}$ | Suppression of Spectrum above 9.0 MHz (not for FM Radio) | | 15 | | – | dB |
| $FM_{MAX}$ | Maximum FM-Deviation (approx.)<br>normal mode<br>HDEV2: high deviation mode<br>HDEV3: very high deviation mode | | | | <br>±180<br>±360<br>±540 | <br>kHz<br>kHz<br>kHz |

#### 4.6.2.4. Crystal Recommendations

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **General Crystal Recommendations** | | | | | | |
| $f_P$ | Crystal Parallel Resonance Frequency at 12 pF Load Capacitance | | | 18.432 | | MHz |
| $R_R$ | Crystal Series Resistance | | | 8 | 25 | Ω |
| $C_0$ | Crystal Shunt (Parallel) Capacitance | | | 6.2 | 7.0 | pF |
| $C_L$ | External Load Capacitance[1)] | XTAL_IN, XTAL_OUT | PSDIP<br>PMQFP | approx. 1.5<br>approx. 3.3 | | pF<br>pF |
| **Crystal Recommendations for FM / NICAM Applications** | | | | | | |
| $f_{TOL}$ | Accuracy of Adjustment | | –30 | | +30 | ppm |
| $D_{TEM}$ | Frequency Variation versus Temperature | | –30 | | +30 | ppm |
| $C_1$ | Motional (Dynamic) Capacitance | | 15 | | | fF |
| $f_{CL}$ | Required Open Loop Clock Frequency ($T_{amb}$ = 25 °C) | | 18.4305 | | 18.4335 | MHz |

[1)] External capacitors at each crystal pin to ground are required. They are necessary to tune the open-loop frequency of the internal PLL and to stabilize the frequency in closed-loop operation. Due to different layouts, the accurate capacitor value should be determined with the customer PCB. The suggested values (1.5...3.3 pF) are figures based on experience and should serve as “start value”.

To adjust the capacitor value, reset the MSP and transfer only the following I²C-protocol:
<80 10 00 20 00 60>.

Measure the frequency at pin TP_CO. Measurement at XTAL_IN/OUT pins is not possible. Change the capacitor value until the frequency matches 18.432/3 = 6.144 MHz as closely as possible. The higher the capacity, the lower the resulting clock frequency.

**Note:** To minimize adjustment tolerances for all MSP-generations, it is strongly recommended to use the so-called MSP-XTAL-REF ICs (available in all packages) for the capacitor adjustment. Since all MSP-XTAL-REF ICs do have an AUD_CL_OUT-pin with the 18.432 MHz signal, this pin should be used for the capacitor adjustment instead of the TP_CO-pin. After the reset, no I²C-protocol should be transmitted. The AUD_CL_OUT-signal is available at the following pins:

| PLCC68 | PSDIP64 | PSDIP52 | PQFP80 | PLQFP64 | PMQFP44[2)] |
|---|---|---|---|---|---|
| pin 18 | pin 1 | pin 2 | pin 74 | pin 57 | pin 8 |

[2)] For the MSP-XTAL-REF IC, the PMQFP44 pin functionality of the D_CTR_I/O1-pin has been changed to the Audio_Clock_Out signal. If D_CTR_I/O1 is used in the customer application, this pin must be left open for the adjustment procedure.

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Crystal Recommendations for all analog FM/AM Applications** | | | | | | |
| $f_{TOL}$ | Accuracy of Adjustment | | –100 | | +100 | ppm |
| $D_{TEM}$ | Frequency Variation versus Temperature | | –50 | | +50 | ppm |
| $f_{CL}$ | Required Open Loop Clock Frequency ($T_{amb}$ = 25 °C) | | 18.429 | | 18.435 | MHz |
| **Amplitude Recommendation for Operation with External Clock Input** ($C_{load}$ after reset typ. 22 pF) | | | | | | |
| $V_{XCA}$ | External Clock Amplitude | XTAL_IN | 0.7 | | | $V_{pp}$ |

### 4.6.3. Characteristics

at $T_A$ = 0 to 70 °C, $f_{CLOCK}$ = 18.432 MHz, $V_{SUP1}$ = 7.6 to 8.7 V, $V_{SUP2}$ = 4.75 to 5.25 V for min./max. values
at $T_A$ = 60 °C, $f_{CLOCK}$ = 18.432 MHz, $V_{SUP1}$ = 8 V, $V_{SUP2}$ = 5 V for typical values,
$T_J$ = Junction Temperature
MAIN (M) = Loudspeaker Channel

#### 4.6.3.1. General Characteristics

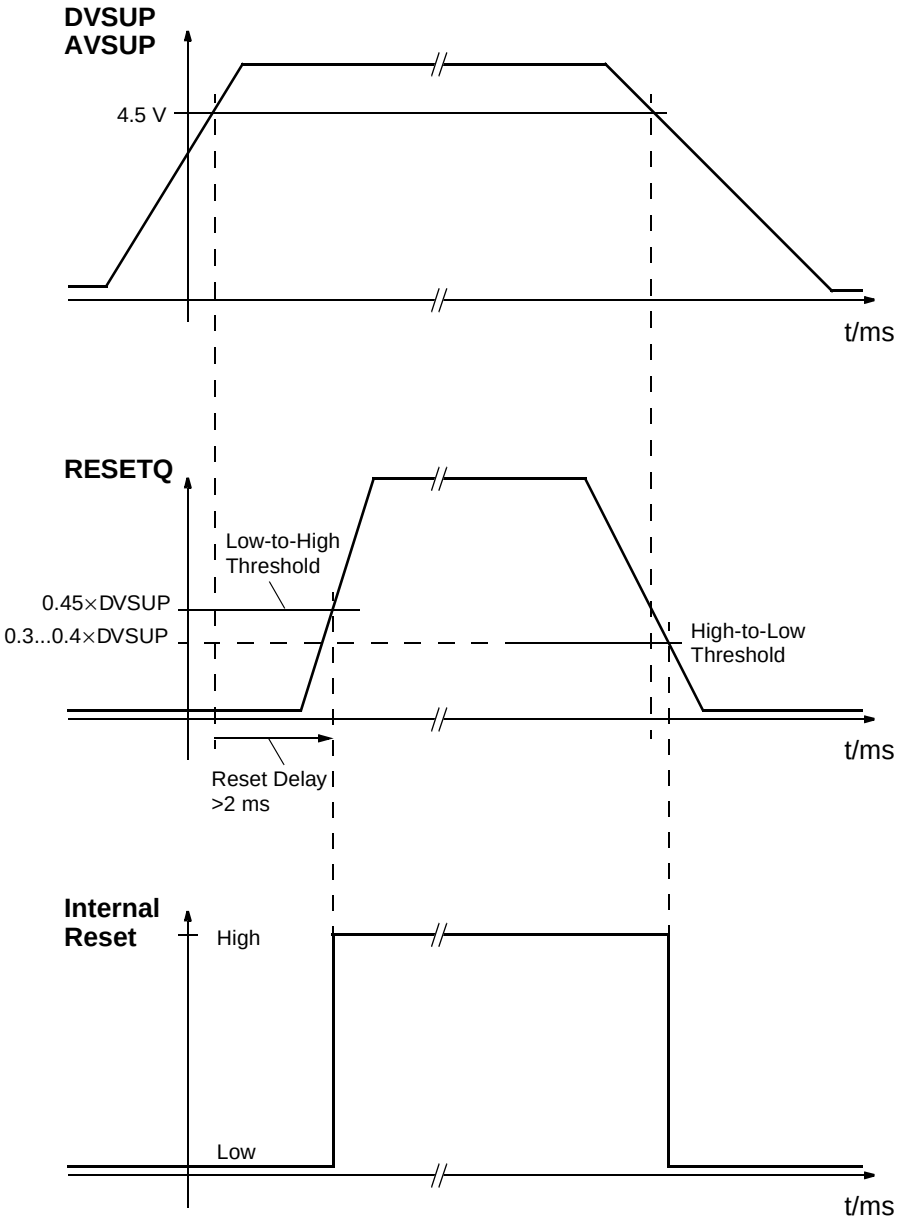
| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| **Supply** | | | | | | | |
| $I_{SUP1A}$ | First Supply Current (active) (AHVSUP = 8 V) | AHVSUP | | 14<br>10 | 22<br>16 | mA<br>mA | Volume Main = 0 dB<br>Volume Main = –30 dB |
| | First Supply Current (active) (AHVSUP = 5 V) | | | 11<br>8 | 16<br>11 | mA<br>mA | Volume Main = 0 dB<br>Volume Main = –30 dB |
| $I_{SUP2A}$ | Second Supply Current (active) | DVSUP | | 55 | 70 | mA | |
| $I_{SUP3A}$ | Third Supply Current (active) | AVSUP | | 30 | 38 | mA | |
| $I_{SUP1S}$ | First Supply Current (AHVSUP = 8 V) | AHVSUP | | 5.6 | 7.7 | mA | STANDBYQ = low |
| | First Supply Current (AHVSUP = 5 V) | | | 3.7 | 5.1 | mA | STANDBYQ = low |
| **Clock** | | | | | | | |
| $f_{CLOCK}$ | Clock Input Frequency | XTAL_IN | | 18.432 | | MHz | |
| $D_{CLOCK}$ | Clock High to Low Ratio | | 45 | | 55 | % | |
| $t_{JITTER}$ | Clock Jitter (verification not provided in production test) | | | | 50 | ps | |
| $V_{xtalDC}$ | DC-Voltage Oscillator | | | 2.5 | | V | |
| $t_{Startup}$ | Oscillator Startup Time at VDD Slew-rate of 1 V/1 µs | XTAL_IN, XTAL_OUT | | 0.4 | 2 | ms | |

### 4.6.3.2. Digital Inputs, Digital Outputs

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| **Digital Input Levels** | | | | | | | |
| $V_{DIGIL}$ | Digital Input Low Voltage | STANDBYQ | | | 0.2 | $V_{SUP2}$ | |
| $V_{DIGIH}$ | Digital Input High Voltage | | 0.5 | | | $V_{SUP2}$ | |
| $Z_{DIGI}$ | Input Impedance | | | | 5 | pF | |
| $I_{DLEAK}$ | Digital Input Leakage Current | | –1 | | 1 | µA | 0 V < $U_{INPUT}$< DVSUP<br>D_CTR_I/O_0/1: tri-state |
| $V_{DIGIL}$ | Digital Input Low Voltage | ADR_SEL | | | 0.2 | $V_{SUP2}$ | |
| $V_{DIGIH}$ | Digital Input High Voltage | | 0.8 | | | $V_{SUP2}$ | |
| $I_{ADRSEL}$ | Input Current Address Select Pin | | –500 | –220 | | µA | $U_{ADR_SEL}$ = DVSS |
| | | | | 220 | 500 | µA | $U_{ADR_SEL}$ = DVSUP |
| $Z_{TESTEN}$ | Input Capacitance | TESTEN | | | 5 | pF | |
| $I_{TESTEN}$ | Input Low Current | | –30 | | | µA | $U_{TESTEN}$ = AVSS |
| **Digital Output Levels** | | | | | | | |
| $V_{DCTROL}$ | Digital Output Low Voltage | D_CTR_I/O_0<br>D_CTR_I/O_1 | | | 0.4 | V | IDDCTR = 1 mA |
| $V_{DCTROH}$ | Digital Output High Voltage | | $V_{SUP2}$ –0.3 | | | V | IDDCTR = –1 mA |

### 4.6.3.3. Reset Input and Power-Up

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| **RESETQ Input Levels** | | | | | | | |
| $V_{RHL}$ | Reset High-Low Transition Voltage | RESETQ | 0.3 | | 0.4 | $V_{SUP2}$ | |
| $V_{RLH}$ | Reset Low-High Transition Voltage | | 0.45 | | 0.55 | $V_{SUP2}$ | |
| $Z_{RES}$ | Input Capacitance | | | | 5 | pF | |
| $I_{RES}$ | Input High Current | | | | 20 | µA | $U_{RESETQ}$ = DVSUP |




**Note:** The reset should not reach high level before the oscillator has started. This requires a reset delay of >2 ms

0.45 x DVSUP means 2.25 Volt with DVSUP = 5.0 V

**Fig. 4–20:** Power-up sequence

### 4.6.3.4. I²C Bus Characteristics

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| $V_{I2CIL}$ | I²C-Bus Input Low Voltage | I2C_CL, I2C_DA | | | 0.3 | $V_{SUP2}$ | |
| $V_{I2CIH}$ | I²C-Bus Input High Voltage | | 0.6 | | | $V_{SUP2}$ | |
| $t_{I2C1}$ | I²C Start Condition Setup Time | | 120 | | | ns | |
| $t_{I2C2}$ | I²C Stop Condition Setup Time | | 120 | | | ns | |
| $t_{I2C5}$ | I²C-Data Setup Time before Rising Edge of Clock | | 55 | | | ns | |
| $t_{I2C6}$ | I²C-Data Hold Time after Falling Edge of Clock | | 55 | | | ns | |
| $t_{I2C3}$ | I²C-Clock Low Pulse Time | I2C_CL | 500 | | | ns | |
| $t_{I2C4}$ | I²C-Clock High Pulse Time | | 500 | | | ns | |
| $f_{I2C}$ | I²C-BUS Frequency | | | | 1.0 | MHz | |
| $V_{I2COL}$ | I²C-Data Output Low Voltage | I2C_CL, I2C_DA | | | 0.4 | V | $I_{I2COL}$ = 3 mA |
| $I_{I2COH}$ | I²C-Data Output High Leakage Current | | | | 1.0 | µA | $V_{I2COH}$ = 5 V |
| $t_{I2COL1}$ | I²C-Data Output Hold Time after Falling Edge of Clock | | 15 | | | ns | |
| $t_{I2COL2}$ | I²C-Data Output Setup Time before Rising Edge of Clock | | 100 | | | ns | $f_{I2C}$ = 1 MHz |

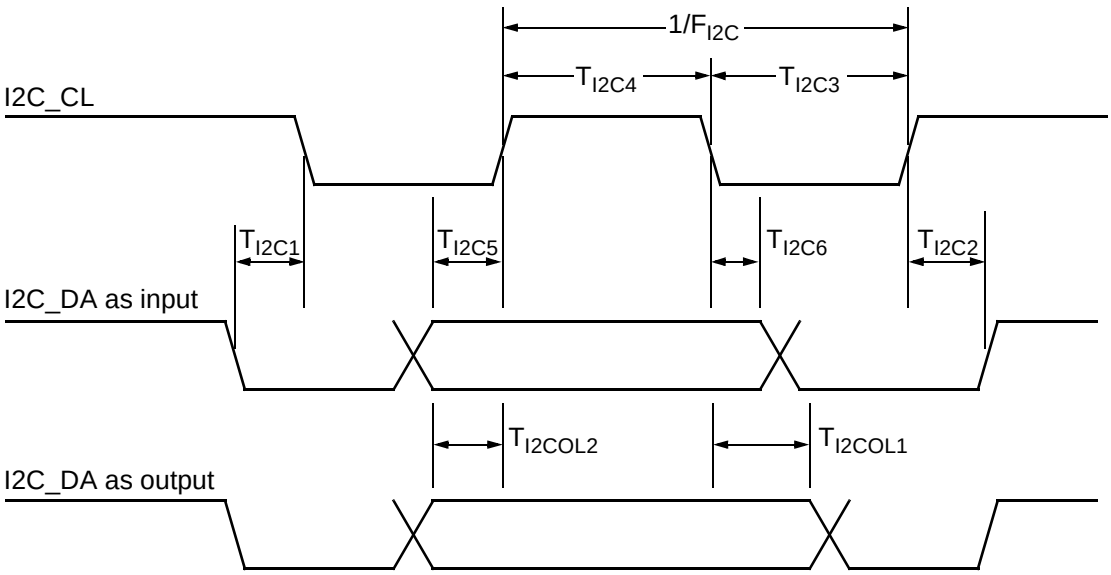



**Fig. 4–21:** I²C bus timing diagram

### 4.6.3.5. Analog Baseband Inputs and Outputs, AGNDC

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| **Analog Ground** | | | | | | | |
| $V_{AGNDC0}$ | AGNDC Open Circuit Voltage (AHVSUP = 8 V) | AGNDC | | 3.77 | | V | $R_{load}$ ≥10 MΩ |
| | AGNDC Open Circuit Voltage (AHVSUP = 5 V) | | | 2.51 | | V | |
| $R_{outAGN}$ | AGNDC Output Resistance (AHVSUP = 8 V) | | 70 | 125 | 180 | kΩ | 3 V ≤ $V_{AGNDC}$ ≤ 4 V |
| | AGNDC Output Resistance (AHVSUP = 5 V) | | 47 | 83 | 120 | kΩ | |
| **Analog Input Resistance** | | | | | | | |
| $R_{inSC}$ | SCART Input Resistance from $T_A$ = 0 to 70 °C | SC1_IN_s[1)] | 25 | 40 | 58 | kΩ | $f_{signal}$ = 1 kHz, I = 0.05 mA |
| $R_{inMONO}$ | MONO Input Resistance from $T_A$ = 0 to 70 °C | MONO_IN | 15 | 24 | 35 | kΩ | $f_{signal}$ = 1 kHz, I = 0.1 mA |
| **Audio Analog-to-Digital-Converter** | | | | | | | |
| $V_{AICL}$ | Analog Input Clipping Level for Analog-to-Digital-Conversion (AHVSUP = 8 V) | SC1_IN_s,[1)] MONO_IN | 2.00 | | 2.25 | $V_{RMS}$ | $f_{signal}$ = 1 kHz |
| | Analog Input Clipping Level for Analog-to-Digital-Conversion (AHVSUP = 5 V) | | 1.13 | | 1.51 | $V_{RMS}$ | |
| **SCART Output** | | | | | | | |
| $R_{outSC}$ | SCART Output Resistance | SC1_OUT_s[1)] | 200<br>200 | 330 | 460<br>500 | Ω<br>Ω | $f_{signal}$ = 1 kHz, I = 0.1 mA<br>$T_j$ = 27 °C<br>$T_A$ = 0 to 70 °C |
| $dV_{OUTSC}$ | Deviation of DC-Level at SCART Output from AGNDC Voltage | | –70 | | +70 | mV | |
| $A_{SCtoSC}$ | Gain from Analog Input to SCART Output | SCn_IN_s,[1)] MONO_IN → SC1_OUT_s[1)] | –1.0 | | +0.5 | dB | $f_{signal}$ = 1 kHz |
| $f_{rSCtoSC}$ | Frequency Response from Analog Input to SCART Output | | –0.5 | | +0.5 | dB | with resp. to 1 kHz<br>Bandwidth: 0 to 20000 Hz |
| $V_{outSC}$ | Signal Level at SCART Output (AHVSUP = 8 V) | SC1_OUT_s[1)] | 1.8 | 1.9 | 2.0 | $V_{RMS}$ | $f_{signal}$ = 1 kHz<br>Volume 0 dB<br>Full Scale input from $I^2S$ |
| | Signal Level at SCART Output (AHVSUP = 5V) | | 1.17 | 1.27 | 1.37 | $V_{RMS}$ | |

1) "s" means "L" or "R"

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| **Main Output** | | | | | | | |
| $R_{outMA}$ | Main Output Resistance | DACM_s[1]) | 2.1<br>2.1 | 3.3 | 4.6<br>5.0 | kΩ<br>kΩ | $f_{signal}$ = 1 kHz, I = 0.1 mA,<br>$T_j$ = 27 °C<br>$T_A$ = 0 to 70 °C |
| $V_{outDCMA}$ | DC-Level at Main-Output (AHVSUP = 8 V) | | 1.80 | 2.04<br>61 | 2.28 | V<br>mV | Volume Main = 0 dB<br>Volume Main = –30 dB |
| | DC-Level at Main-Output (AHVSUP = 5 V) | | 1.12 | 1.36<br>40 | 1.60 | V<br>mV | Volume Main = 0 dB<br>Volume Main = –30 dB |
| $V_{outMA}$ | Signal Level at Main-Output (AHVSUP = 8 V) | | 1.23 | 1.37 | 1.51 | $V_{RMS}$ | $f_{signal}$ = 1 kHz, full scale,<br>Volume Main = 0 dB |
| | Signal Level at Main-Output (AHVSUP = 5 V) | | 0.76 | 0.90 | 1.04 | $V_{RMS}$ | |

1) “s” means “L” or “R”

### 4.6.3.6. Sound IF Input

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| $R_{IFIN}$ | Input Impedance | ANA_IN1+,<br>ANA_IN– | 1.5<br>6.8 | 2<br>9.1 | 2.5<br>11.4 | kΩ<br>kΩ | Gain AGC = 20 dB<br>Gain AGC = 3 dB |
| $DC_{VREFTOP}$ | DC Voltage at VREFTOP | VREFTOP | 2.4 | 2.65 | 2.75 | V | |
| $DC_{ANA_IN}$ | DC Voltage on IF Inputs | ANA_IN1+,<br>ANA_IN– | 1.3 | 1.5 | 1.7 | V | |
| $XTALK_{IF}$ | Crosstalk Attenuation | ANA_IN1+,<br>ANA_IN– | 40 | | | dB | $f_{signal}$ = 1 MHz<br>Input Level = –2 dBr |
| $BW_{IF}$ | 3 dB Bandwidth | | 10 | | | MHz | |
| AGC | AGC Step Width | | | 0.85 | | dB | |

### 4.6.3.7. Power Supply Rejection

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| **PSRR: Rejection of Noise on AHVSUP at 1 kHz** | | | | | | | |
| PSRR | AGNDC | AGNDC | | 80 | | dB | |
| | From Analog Input to SCART Output | MONO_IN,<br>SC1_IN_s[1)]<br>SC1_OUT_s[1)] | | 70 | | dB | |

1) “s” means “L” or “R”

### 4.6.3.8. Analog Performance

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| **Specifications for AHVSUP = 8 V** | | | | | | | |
| SNR | Signal-to-Noise Ratio | | | | | | |
| | from Analog Input to SCART Output | MONO_IN, SC1_IN_s[1)] → SC1_OUT_s[1)] | 93 | 96 | | dB | Input Level = –20 dB, $f_{sig}$ = 1 kHz, unweighted 20 Hz…20 kHz |
| THD | Total Harmonic Distortion | | | | | | |
| | from Analog Input to SCART Output | MONO_IN, SC1_IN_s → SC1_OUT_s[1)] | | 0.01 | 0.03 | % | Input Level = –3 dBr, $f_{sig}$ = 1 kHz, unweighted 20 Hz…20 kHz |
| **Specifications for AHVSUP = 5 V** | | | | | | | |
| SNR | Signal-to-Noise Ratio | | | | | | |
| | from Analog Input to SCART Output | MONO_IN, SC1_IN_s[1)] → SC1_OUT_s[1)] | 90 | 93 | | dB | Input Level = –20 dB, $f_{sig}$ = 1 kHz, unweighted 20 Hz…20 kHz |
| THD | Total Harmonic Distortion | | | | | | |
| | from Analog Input to SCART Output | MONO_IN, SC1_IN_s → SC1_OUT_s[1)] | | | 0.1 | % | Input Level = –3 dBr, $f_{sig}$ = 1 kHz, unweighted 20 Hz…20 kHz |
| **CROSSTALK Specifications for AHVSUP = 8 V and 5 V** | | | | | | | |
| XTALK | Crosstalk Attenuation | | | | | | Input Level = –3 dB, $f_{sig}$ = 1 kHz, unused analog inputs connected to ground by Z < 1 kΩ |
| | between left and right channel within SCART Input/Output pair (L→R, R→L) SC1_IN → SC1_OUT | | 80 | | | dB | unweighted 20 Hz…20 kHz |
| | between MONO Input and SCART Input | | 95 | | | dB | unweighted 20 Hz…20 kHz |

1) “s” means “L” or “R”

### 4.6.3.9. Sound Standard Dependent Characteristics

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| **NICAM Characteristics (MSP Standard Code = 8)** | | | | | | | |
| $dV_{NICAMOUT}$ | Tolerance of Output Voltage of NICAM Baseband Signal | DACM_s, SC1_OUT_s[1)] | –1.5 | | +1.5 | dB | 2.12 kHz, Modulator input level = 0 dBref |
| $S/N_{NICAM}$ | S/N of NICAM Baseband Signal | | 72 | | | dB | NICAM: –6 dB, 1 kHz, RMS unweighted 0 to 15 kHz, Vol = 9 dB NIC_Presc = $7F_{hex}$ Output level 1 $V_{RMS}$ at DACM_s |
| $THD_{NICAM}$ | Total Harmonic Distortion + Noise of NICAM Baseband Signal | | | | 0.1 | % | 2.12 kHz, Modulator input level = 0 dBref |
| $BER_{NICAM}$ | NICAM: Bit Error Rate | | | | 1 | $10^{-7}$ | FM+NICAM, norm conditions |
| $fR_{NICAM}$ | NICAM Frequency Response, 20...15000 Hz | | –1.0 | | +1.0 | dB | Modulator input level = –12 dB dBref; RMS |
| $XTALK_{NICAM}$ | NICAM Crosstalk Attenuation (Dual) | | 80 | | | dB | |
| $SEP_{NICAM}$ | NICAM Channel Separation (Stereo) | | 80 | | | dB | |
| **FM Characteristics (MSP Standard Code = 3)** | | | | | | | |
| $dV_{FMOUT}$ | Tolerance of Output Voltage of FM Demodulated Signal | DACM_s, SC1_OUT_s[1)] | –1.5 | | +1.5 | dB | 1 FM-carrier, 50 µs, 1 kHz, 40 kHz deviation; RMS |
| $S/N_{FM}$ | S/N of FM Demodulated Signal | | 73 | | | dB | 1 FM-carrier 5.5 MHz, 50 µs, 1 kHz, 40 kHz deviation; RMS, unweighted 0 to 15 kHz (for S/N); full input range, FM-Prescale = $46_{hex}$, Vol = 0 dB → Output Level 1 $V_{RMS}$ at DACM_s |
| $THD_{FM}$ | Total Harmonic Distortion + Noise of FM Demodulated Signal | | | | 0.1 | % | |
| $fR_{FM}$ | FM Frequency Responses, 20...15000 Hz | | –1.0 | | +1.0 | dB | 1 FM-carrier 5.5 MHz, 50 µs, Modulator input level = –14.6 dBref; RMS |
| $XTALK_{FM}$ | FM Crosstalk Attenuation (Dual) | | 80 | | | dB | 2 FM-carriers 5.5/5.74 MHz, 50 µs, 1 kHz, 40 kHz deviation; Bandpass 1 kHz |
| $SEP_{FM}$ | FM Channel Separation (Stereo) | | 50 | | | dB | 2 FM-carriers 5.5/5.74 MHz, 50 µs, 1 kHz, 40 kHz deviation; RMS |
| **AM Characteristics (MSP Standard Code = 9)** | | | | | | | |
| $S/N_{AM(1)}$ | S/N of AM Demodulated Signal measurement condition: RMS/Flat | DACM_s, SC1_OUT_s[1)] | 55 | | | dB | SIF level: 0.1–0.8 $V_{pp}$ AM-carrier 54% at 6.5 MHz Vol = 0 dB, FM/AM prescaler set for output = 0.5 $V_{RMS}$ at Loudspeaker out; Standard Code = $09_{hex}$ no video/chroma components |
| $S/N_{AM(2)}$ | S/N of AM Demodulated Signal measurement condition: QP/CCIR | | 45 | | | dB | |
| $THD_{AM}$ | Total Harmonic Distortion + Noise of AM Demodulated Signal | | | | 0.6 | % | |
| $fR_{AM}$ | AM Frequency Response 50...12000 Hz | | –2.5 | | +1.0 | dB | |

1) “s” means “L” or “R”

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| **BTSC Characteristics (MSP Standard Code = $20_{hex}$, $21_{hex}$)** | | | | | | | |
| $S/N_{BTSC}$ | S/N of BTSC Stereo Signal<br>S/N of BTSC-SAP Signal | DACM_s, SC1_OUT_s[1)] | 68<br>57 | | | dB<br>dB | 1 kHz L or R or SAP, 100% modulation, 75 µs deemphasis, RMS unweighted 0 to 15 kHz |
| $THD_{BTSC}$ | THD+N of BTSC Stereo Signal<br>THD+N of BTSC SAP Signal | | | | 0.1<br>0.5 | %<br>% | 1 kHz L or R or SAP, 100% 75 µs EIM[2)], DBX NR or MNR, RMS unweighted 0 to 15 kHz |
| $fR_{DBX}$ | Frequency Response of BTSC Stereo, 50 Hz...12 kHz<br>Frequency Response of BTSC-SAP, 50 Hz...9 kHz | | –1.0<br>–1.0 | | 1.0<br>1.0 | dB<br>dB | L or R or SAP, 1%...66% EIM[2)], DBX NR |
| $fR_{MNR}$ | Frequency Response of BTSC Stereo, 50 Hz...12 kHz | | –2.0 | | 2.0 | dB | L or R 5%...66% EIM[2)], MNR |
| | Frequency Response of BTSC-SAP, 50 Hz...9 kHz | | –2.0 | | 2.0 | dB | SAP, white noise, 10% Modulation, MNR |
| $XTALK_{BTSC}$ | Stereo → SAP<br>SAP → Stereo | | 76<br>80 | | | dB<br>dB | 1 kHz L or R or SAP, 100% modulation, 75 µs deemphasis, Bandpass 1 kHz |
| $SEP_{DBX}$ | Stereo Separation DBX NR<br>50 Hz...10 kHz<br>50 Hz...12 kHz | | <br>35<br>30 | | | <br>dB<br>dB | L or R 1%...66% EIM[2)], DBX NR |
| $SEP_{MNR}$ | Stereo Separation MNR | | 30 | | | dB | L = 300 Hz, R = 3.1 kHz 14% Modulation, MNR |
| $FM_{pil}$ | Pilot deviation threshold<br>Stereo off → on<br>Stereo on → off | ANA_IN1+ | <br>3.2<br>1.2 | | <br>3.5<br>1.5 | <br>kHz<br>kHz | 4.5 MHz carrier modulated with $f_h$ = 15.734 kHz SIF level = 100 $mV_{pp}$ indication: STATUS Bit[6] |
| $f_{Pilot}$ | Pilot Frequency Range | | 15.563 | | 15.843 | kHz | standard BTSC stereo signal, sound carrier only |

1) "s" means "L" or "R"
2) EIM refers to 75-µs Equivalent Input Modulation. It is defined as the audio-signal level which results in a stated percentage modulation, when the DBX encoding process is replaced by a 75-µs preemphasis network.

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| **BTSC Characteristics (MSP Standard Code = $20_{hex}$, $21_{hex}$) with a minimum IF input signal level of 70 mVpp (measured without any video/chroma signal components)** | | | | | | | |
| $S/N_{BTSC}$ | S/N of BTSC Stereo Signal<br>S/N of BTSC-SAP Signal | DACM_s, SC1_OUT_s[1)] | 64<br>55 | | | dB<br>dB | 1 kHz L or R or SAP, 100% modulation, 75 µs deemphasis, RMS unweighted 0 to 15 kHz |
| $THD_{BTSC}$ | THD+N of BTSC Stereo Signal<br>THD+N of BTSC SAP Signal | | | | 0.15<br>0.8 | %<br>% | 1 kHz L or R or SAP, 100% 75 µs EIM[2)], DBX NR or MNR, RMS unweighted 0 to 15 kHz |
| $fR_{DBX}$ | Frequency Response of BTSC Stereo, 50 Hz...12 kHz<br>Frequency Response of BTSC-SAP, 50 Hz...9 kHz | | –1.0<br>–1.0 | | 1.0<br>1.0 | dB<br>dB | L or R or SAP, 1%...66% EIM[2)], DBX NR |
| $fR_{MNR}$ | Frequency Response of BTSC Stereo, 50 Hz...12 kHz | | –2.0 | | 2.0 | dB | L or R 5%...66% EIM[2)], MNR |
| | Frequency Response of BTSC-SAP, 50 Hz...9 kHz | | –2.0 | | 2.0 | dB | SAP, white noise, 10% Modulation, MNR |
| $XTALK_{BTSC}$ | Stereo → SAP<br>SAP → Stereo | | 75<br>75 | | | dB<br>dB | 1 kHz L or R or SAP, 100% modulation, 75 µs deemphasis, Bandpass 1 kHz |
| $SEP_{DBX}$ | Stereo Separation DBX NR<br>50 Hz...10 kHz<br>50 Hz...12 kHz | | <br>35<br>30 | | | <br>dB<br>dB | L or R 1%...66% EIM[2)], DBX NR |
| $SEP_{MNR}$ | Stereo Separation MNR | | 30 | | | dB | L = 300 Hz, R = 3.1 kHz 14% Modulation, MNR |

1) "s" means "L" or "R"
2) EIM refers to 75-µs Equivalent Input Modulation. It is defined as the audio-signal level which results in a stated percentage modulation, when the DBX encoding process is replaced by a 75-µs preemphasis network.

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| **EIA-J Characteristics (MSP Standard Code = $30_{hex}$)** | | | | | | | |
| $S/N_{EIAJ}$ | S/N of EIA-J Stereo Signal<br>S/N of EIA-J Sub-Channel | DACM_s, SC1_OUT_s[1)] | 60<br>60 | | | dB<br>dB | 1 kHz L or R, 100% modulation, 75 µs deemphasis, RMS unweighted 0 to 15 kHz |
| $THD_{EIAJ}$ | THD+N of EIA-J Stereo Signal<br>THD+N of EIA-J Sub-Channel | | | | 0.2<br>0.3 | %<br>% | |
| $fR_{EIAJ}$ | Frequency Response of EIA-J Stereo, 50 Hz...12 kHz<br>Frequency Response of EIA-J Sub-Channel, 50 Hz...12 kHz | | –1.0<br>–1.0 | | 1.0<br>1.0 | dB<br>dB | 100% modulation, 75 µs deemphasis |
| $XTALK_{EIAJ}$ | Main → SUB<br>Sub → MAIN | | 66<br>80 | | | dB<br>dB | 1 kHz L or R, 100% modulation, 75 µs deemphasis, Bandpass 1 kHz |
| $SEP_{EIAJ}$ | Stereo Separation<br>50 Hz...5 kHz<br>50 Hz...10 kHz | | <br>35<br>28 | | | <br>dB<br>dB | EIA-J Stereo Signal, L or R 100% modulation |
| **FM-Radio Characteristics (MSP Standard Code = $40_{hex}$)** | | | | | | | |
| $S/N_{UKW}$ | S/N of FM-Radio Stereo Signal | DACM_s, SC1_OUT_s[1)] | 68 | | | dB | 1 kHz L or R, 100% modulation, 75 µs deemphasis, RMS unweighted 0 to 15 kHz |
| $THD_{UKW}$ | THD+N of FM-Radio Stereo Signal | | | | 0.1 | % | |
| $fR_{UKW}$ | Frequency Response of FM-Radio Stereo 50 Hz...15 kHz | | –1.0 | | +1.0 | dB | L or R, 1%...100% modulation, 75 µs deemphasis |
| $SEP_{UKW}$ | Stereo Separation 50 Hz...15 kHz | | 45 | | | dB | |
| $f_{Pilot}$ | Pilot Frequency Range | ANA_IN1+ | 18.844 | | 19.125 | kHz | standard FM radio stereo signal |

[1)] “s” means “L” or “R”

# 5. Appendix A: Overview of TV Sound Standards

## 5.1. NICAM 728

**Table 5–1:** Summary of NICAM 728 sound modulation parameters

| Specification | I | B/G | L | | D/K | |
|---|---|---|---|---|---|---|
| Carrier frequency of digital sound | 6.552 MHz | 5.85 MHz | 5.85 MHz | | 5.85 MHz | |
| Transmission rate | 728 kbit/s | | | | | |
| Type of modulation | Differentially encoded quadrature phase shift keying (DQPSK) | | | | | |
| Spectrum shaping Roll-off factor | by means of Roll-off filters | | | | | |
| | 1.0 | 0.4 | 0.4 | | 0.4 | |
| Carrier frequency of analog sound component | 6.0 MHz FM mono | 5.5 MHz FM mono | 6.5 MHz AM mono | | 6.5 MHz FM mono | |
| | | | terrestrial | cable | | |
| Power ratio between vision carrier and analog sound carrier | 10 dB | 13 dB | 10 dB | 16 dB | 13 dB | |
| Power ratio between analog and modulated digital sound carrier | 10 dB | 7 dB | 17 dB | 11 dB | China/ Hungary | Poland |
| | | | | | 12 dB | 7 dB |

**Table 5–2:** Summary of NICAM 728 sound coding characteristics

| Characteristics | Values |
|---|---|
| Audio sampling frequency | 32 kHz |
| Number of channels | 2 |
| Initial resolution | 14 bit/sample |
| Companding characteristics | near instantaneous, with compression to 10 bits/sample in 32-samples (1 ms) blocks |
| Coding for compressed samples | 2’s complement |
| Preemphasis | CCITT Recommendation J.17 (6.5 dB attenuation at 800 Hz) |
| Audio overload level | +12 dBm measured at the unity gain frequency of the preemphasis network (2 kHz) |

### 5.2. A2 Systems

**Table 5–3:** Key parameters for A2 Systems of Standards B/G, D/K, and M

| **Characteristics** | **Sound Carrier FM1** | | | **Sound Carrier FM2** | | |
|---|---|---|---|---|---|---|
| TV-Sound Standard | **B/G** | **D/K** | **M** | **B/G** | **D/K** | **M** |
| Carrier frequency in MHz | 5.5 | 6.5 | 4.5 | 5.7421875 | 6.2578125<br>6.7421875<br>5.7421875 | 4.724212 |
| Vision/sound power difference | 13 dB | | | 20 dB | | |
| Sound bandwidth | 40 Hz to 15 kHz | | | | | |
| Preemphasis | 50 µs | | 75 µs | 50 µs | | 75 µs |
| Frequency deviation (nom/max) | ±27/±50 kHz | | ±17/±25 kHz | ±27/±50 kHz | | ±15/±25 kHz |
| **Transmission Modes** | | | | | | |
| Mono transmission | mono | | | mono | | |
| Stereo transmission | (L+R)/2 | | (L+R)/2 | R | | (L–R)/2 |
| Dual sound transmission | language A | | | language B | | |
| **Identification of Transmission Mode** | | | | | | |
| Pilot carrier frequency | | | | 54.6875 kHz | | 55.0699 kHz |
| Max. deviation portion | | | | ±2.5 kHz | | |
| Type of modulation / modulation depth | | | | AM / 50% | | |
| Modulation frequency | | | | mono: unmodulated<br>stereo: 117.5 Hz<br>dual: 274.1 Hz | | <br>149.9 Hz<br>276.0 Hz |

### 5.3. BTSC-Sound System

**Table 5–4:** Key parameters for BTSC-Sound Systems

| | Aural Carrier | BTSC-MPX-Components | | | | |
|---|---|---|---|---|---|---|
| | | (L+R) | Pilot | (L–R) | SAP | Prof. Ch. |
| Carrier frequency ($f_{hNTSC}$ = 15.734 kHz) ($f_{hPAL}$ = 15.625 kHz) | 4.5 MHz | Baseband | $f_h$ | 2 $f_h$ | 5 $f_h$ | 6.5 $f_h$ |
| Sound bandwidth in kHz | | 0.05 - 15 | | 0.05 - 15 | 0.05 - 12 | 0.05 - 3.4 |
| Preemphasis | | 75 µs | | DBX | DBX | 150 µs |
| Max. deviation to Aural Carrier | 73 kHz (total) | 25 kHz[1)] | 5 kHz | 50 kHz[1)] | 15 kHz | 3 kHz |
| Max. Freq. Deviation of Subcarrier Modulation Type | | | | AM | 10 kHz FM | 3 kHz FM |
| [1)] Sum does not exceed 50 kHz due to interleaving effects | | | | | | |

### 5.4. Japanese FM Stereo System (EIA-J)

**Table 5–5:** Key parameters for Japanese FM-Stereo Sound System EIA-J

| | Aural Carrier FM | EIA-J-MPX-Components | | |
|---|---|---|---|---|
| | | (L+R) | (L–R) | Identification |
| Carrier frequency ($f_h$ = 15.734 kHz) | 4.5 MHz | Baseband | 2 $f_h$ | 3.5 $f_h$ |
| Sound bandwidth | | 0.05 - 15 kHz | 0.05 - 15 kHz | – |
| Preemphasis | | 75 µs | 75 µs | none |
| Max. deviation portion to Aural Carrier | 47 kHz | 25 kHz | 20 kHz | 2 kHz |
| Max. Freq. Deviation of Subcarrier Modulation Type | | | 10 kHz FM | 60% AM |
| Transmitter-sided delay | | 20 µs | 0 µs | 0 µs |
| Mono transmission | | L+R | – | unmodulated |
| Stereo transmission | | L+R | L–R | 982.5 Hz |
| Bilingual transmission | | Language A | Language B | 922.5 Hz |

### 5.5. FM Satellite Sound

**Table 5–6:** Key parameters for FM Satellite Sound

| Carrier Frequency | Maximum FM Deviation | Sound Mode | Bandwidth | Deemphasis |
|---|---|---|---|---|
| 6.5 MHz | 85 kHz | Mono | 15 kHz | 50 µs |
| 7.02/7.20 MHz | 50 kHz | Mono/Stereo/Bilingual | 15 kHz | adaptive |
| 7.38/7.56 MHz | 50 kHz | Mono/Stereo/Bilingual | 15 kHz | adaptive |
| 7.74/7.92 MHz | 50 kHz | Mono/Stereo/Bilingual | 15 kHz | adaptive |

### 5.6. FM-Stereo Radio

**Table 5–7:** Key parameters for FM-Stereo Radio Systems

| | Aural Carrier | FM-Radio-MPX-Components | | | |
|---|---|---|---|---|---|
| | | (L+R) | Pilot | (L–R) | RDS/ARI |
| Carrier frequency ($f_p$ = 19 kHz) | 10.7 MHz | Baseband | $f_p$ | 2 $f_p$ | 3 $f_h$ |
| Sound bandwidth in kHz | | 0.05 - 15 | | 0.05 - 15 | |
| Preemphasis:<br>– USA<br>– Europe | | <br>75 µs<br>50 µs | | <br>75 µs<br>50 µs | |
| Max. deviation to Aural Carrier | 75 kHz (100%) | 90%[1)] | 10% | 90%[1)] | 5% |
| [1)] Sum does not exceed 90% due to interleaving effects. | | | | | |

## 6. Appendix B: Manual/Compatibility Mode

To adapt the modes of the STANDARD SELECT register to individual requirements and for reasons of **compatibility to the MSP 34x7D,** the MSP 34x7G offers an Manual/Compatibility Mode, which provides sophisticated programming of the MSP 34x7G.

Using the STANDARD SELECT register generally provides a more economic way to program the MSP 34x7G and will result in optimal behavior. **Therefore, it is not recommend to use the Manual/Compatibility mode.** In those cases, where the MSP 34x7D is to be substituted by the MSP 34x7G, the tips given in Section 6.9. on page 75 have to be obeyed by the controller software.

### 6.1. Demodulator Write and Read Registers for Manual/Compatibility Mode

**Table 6–1:** Demodulator Write Registers; Subaddress: $10_{hex}$; these registers are not readable!

| Demodulator Write Registers | Address (hex) | MSP-Version | Description | Reset Mode | Page |
|---|---|---|---|---|---|
| AUTO_FM/AM | 00 21 | 3417, 3457 | **1. MODUS[0]=1 (Automatic Sound Select):** Switching Level threshold of Automatic Switching between NICAM and FM/AM in case of bad NICAM reception<br>**2. MODUS[0]=0 (Manual Mode):** Activation and configuration of Automatic Switching between NICAM and FM/AM in case of bad NICAM reception | 00 00 | 63 |
| A2_Threshold | 00 22 | all | A2 Stereo Identification Threshold | 00 $19_{hex}$ | 65 |
| CM_Threshold | 00 24 | all | Carrier-Mute Threshold | 00 $2A_{hex}$ | 65 |
| AD_CV | 00 BB | all | SIF-input selection, configuration of AGC, and Carrier-Mute Function | 00 00 | 66 |
| MODE_REG | 00 83 | 3417, 3457 | Controlling of MSP-Demodulator and Interface options. As soon as this register is applied, the MSP 34x7G works in the **MSP 34x7D compatibility mode.**<br>**Warning: In this mode, BTSC, EIA-J, and FM-Radio are disabled.** Only MSP 34x7D features are available; the use of MODUS and STATUS register is not allowed.<br>The MSP 34x7G is reset to the normal mode by first programming the MODUS register followed by transmitting a valid standard code to the STANDARD SELECTION register. | 00 00 | 68 |
| FIR1<br>FIR2 | 00 01<br>00 05 | | FIR1-filter coefficients channel 1 (6 · 8 bit)<br>FIR2-filter coefficients channel 2 (6 · 8 bit), + 3 · 8 bit offset (total 72 bit) | 00 00 | 69 |
| DCO1_LO<br>DCO1_HI<br>DCO2_LO<br>DCO2_HI | 00 93<br>00 9B<br>00 A3<br>00 AB | | Increment channel 1 Low Part<br>Increment channel 1 High Part<br>Increment channel 2 Low Part<br>Increment channel 2 High Part | 00 00 | 69 |
| **Note:** All registers except AUTO_FM/AM, A2_Threshold, and CM_Threshold are initialized during STANDARD SELECTION and are automatically updated when Automatic Sound Select (MODUS[0]=1) is on. | | | | | |

**Table 6–2:** Demodulator Read Registers; Subaddress: $11_{hex}$; these registers are not writable!

| Demodulator Read Registers | Address (hex) | MSP-Version | Description | Page |
|---|---|---|---|---|
| C_AD_BITS | 00 23 | 3417, 3457 | NICAM-Sync bit, NICAM-C-Bits, and three LSBs of additional data bits | 71 |
| ADD_BITS | 00 38 | | NICAM: bit [10:3] of additional data bits | 71 |
| CIB_BITS | 00 3E | | NICAM: CIB1 and CIB2 control bits | 71 |
| ERROR_RATE | 00 57 | | NICAM error rate, updated with 182 ms | 72 |
| PLL_CAPS | 02 1F | | Not for customer use. | 72 |
| AGC_GAIN | 02 1E | | Not for customer use. | 72 |

## 6.2. DSP Write and Read Registers for Manual/Compatibility Mode

**Table 6–3:** DSP-Write Registers; Subaddress: $12_{hex}$, all registers are readable as well

| Write Register | Address (hex) | Bits | Operational Modes and Adjustable Range | Reset Mode | Page |
|---|---|---|---|---|---|
| Volume SCART1 channel: Ctrl. mode | 00 07 | [7:0] | [Linear mode / logarithmic mode] | $00_{hex}$ | 73 |
| FM Fixed Deemphasis | 00 0F | [15:8] | [50 µs, 75 µs, J17, OFF] | 50 µs | 73 |
| FM Adaptive Deemphasis | | [7:0] | [OFF, WP1] | OFF | 73 |
| Identification Mode | 00 15 | [7:0] | [B/G, M] | B/G | 74 |
| FM DC Notch | 00 17 | [7:0] | [ON, OFF] | ON | 74 |

**Table 6–4:** DSP Read Registers; Subaddress: $13_{hex}$, all registers are not writable

| Additional Read Registers | Address (hex) | Bits | Output Range | Page |
|---|---|---|---|---|
| Stereo detection register for A2 Stereo Systems | 00 18 | [15:8] | [$80_{hex}$ ... $7F_{hex}$] 8 bit two's complement | 74 |
| DC level readout FM1/Ch2-L | 00 1B | [15:0] | [$8000_{hex}$ ... $7FFF_{hex}$] 16 bit two's complement | 74 |
| DC level readout FM2/Ch1-R | 00 1C | [15:0] | [$8000_{hex}$ ... $7FFF_{hex}$] 16 bit two's complement | 74 |

## 6.3. Manual/Compatibility Mode: Description of Demodulator Write Registers

### 6.3.1. Automatic Switching between NICAM and Analog Sound

In case of bad NICAM reception or loss of the NICAM-carrier, the MSP 34x7G offers an Automatic Switching (fall back) to the analog sound (FM/AM-mono), without the necessity for the controller of reading and evaluating any parameters. If a proper NICAM signal returns, switching back to this source is performed automatically as well. The feature evaluates the NICAM ERROR_RATE and switches, if necessary, all output channels which are assigned to the NICAM-source, to the analog source, and vice versa.

An appropriate hysteresis algorithm avoids oscillating effects (see Fig. 6–1). STATUS[9] and C_AD_BITS[11] (Addr: 0023 hex) provide information about the actual NICAM-FM/AM-status.

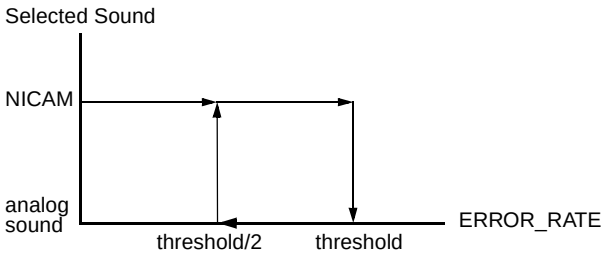



**Fig. 6–1:** Hysteresis for Automatic Switching

#### 6.3.1.1. Function in Automatic Sound Select Mode

The Automatic Sound Select feature (MODUS[0]=1) includes the procedure mentioned above. By default, the internal ERROR_RATE threshold is set to $700_{dec}$. i.e.:

– NICAM → analog Sound if ERROR_RATE > 700

– analog Sound → NICAM if ERROR_RATE < 700/2

The ERROR_RATE value of 700 corresponds to a BER of approximately $5.46*10^{-3}$ /s.

Individual configuration of the threshold can be done using Table 6–5. We recommend to use the internal setting used by the standard selection.

The optimum NICAM sound can be assigned to the MSP output channels by selecting one of the “Stereo or A/B”, “Stereo or A”, or “Stereo or B” source channels

#### 6.3.1.2. Function in Manual Mode

If the manual mode (MODUS[0]=0) is required, the activation and configuration of the Automatic Switching feature has to be done as described in Table 6–6. Note, that the channel matrix of the corresponding output-channels must be set according to the NICAM-mode and need not to be changed in the FM/AM-fallback case.

**Example:**
Required threshold = 500: bits[10:1] = 00 1111 1010

**Table 6–5:** Coding of Automatic NICAM/Analog Sound Switching; **Automatic Sound Select is on (MODUS[0] = 1)**

| Mode | Description | AUTO_FM [11:0] Addr. = 00 $21_{hex}$ | ERROR_RATE-Threshold/dec | Source Select: Input at NICAM Path[1)] |
|---|---|---|---|---|
| 1 Default | Automatic Switching with **internal** threshold | bit[11:0] = 0 | 700 | NICAM or FM/AM, depending on ERROR_RATE |
| 2 | Automatic Switching with **external** threshold (Customizing of Automatic Sound Select) | bit[11] = 0<br>bit[10:1] = 25...1000<br>= threshold/2<br>bit[0] = 1 | set by customer; recommended range: 50...2000 | |
| 3 | Forced Analog Mono | bit[11] = 1<br>bit[10:1] = ignored<br>bit[0] = 1 | | always FM/AM |

[1)] The NICAM path may be assigned to “Stereo or A/B”, “Stereo or A”, or “Stereo or B” source channels (see Table 2–2 on page 11).

**Table 6–6:** Coding of Automatic NICAM/Analog Sound Switching;
**Automatic Sound Select is off (MODUS[0] = 0)**

| Mode | Description | AUTO_FM [11:0]<br>Addr. = 00 $21_{hex}$ | ERROR_RATE-<br>Threshold/dec | Source Select:<br>Input at NICAM Path |
|---|---|---|---|---|
| 0<br>reset status | Forced NICAM<br>(Automatic Switching disabled) | bit[11] = 0<br>bit[10:1] = 0<br>bit[0] = 0 | none | always NICAM; Mute in case of no NICAM available |
| 1 | Automatic Switching with **internal** threshold<br>(Default, if Automatic Sound Select is on) | bit[11] = 0<br>bit[10:1] = 0<br>bit[0] = 1 | 700 | NICAM or FM/AM, depending on ERROR_RATE |
| 2 | Automatic Switching with **external** threshold<br>(Customizing of Automatic Sound Select) | bit[11] = 0<br>bit[10:1] = 25...1000<br>= threshold/2<br>bit[0] = 1 | set by customer; recommended range: 50...2000 | |
| 3 | Forced Analog Mono<br>(Automatic Switching disabled) | bit[11] = 1<br>bit[10:1] = 0<br>bit[0] = 1 | none | always FM/AM |

### 6.3.2. A2 Threshold

The threshold between Stereo/Bilingual and Mono Identification for the A2 Standard has been made programmable according to the user's preferences. An internal hysteresis ensures robustness and stability.

**Table 6–7:** Write Register on $I^2C$ Subaddress $10_{hex}$ : A2 Threshold

| Register Address | Function | Name |
|---|---|---|
| **THRESHOLDS** | | |
| 00 $22_{hex}$ (write) | **A2 THRESHOLD Register**<br>Defines threshold of all A2 and EIA_J standards for Stereo and Bilingual detection<br>bit[15:0] $07F0_{hex}$ force Mono Identification<br>...<br>$0190_{hex}$ default setting after reset<br>...<br>$00A0_{hex}$ minimum Threshold for stable detection<br>recommended range : $00A0_{hex}$...$03C0_{hex}$ | A2_THRESH |

### 6.3.3. Carrier-Mute Threshold

The Carrier-Mute threshold has been made programmable according to the user's preferences. An internal hysteresis ensures stable behavior.

**Table 6–8:** Write Register on $I^2C$ Subaddress $10_{hex}$ : Carrier-Mute Threshold

| Register Address | Function | Name |
|---|---|---|
| **THRESHOLDS** | | |
| 00 $24_{hex}$ (write) | **Carrier-Mute THRESHOLD Register**<br>Defines threshold for the carrier mute feature<br>bit[15:0] $0000_{hex}$ Carrier-Mute always ON (both channels muted)<br>...<br>$002A_{hex}$ default setting after reset<br>...<br>$07FF_{hex}$ Carrier-Mute always OFF (both channels forced on)<br>recommended range : $0014_{hex}$...$0050_{hex}$ | CM_THRESH |

### 6.3.4. Register AD_CV

The use of this register is no longer recommended. Use it only in cases where compatibility to the MSP 34x7D is required. Using the STANDARD SELECTION register together with the MODUS register provides a more economic way to program the MSP 34x7G

**Table 6–9:** AD_CV Register; reset status: all bits are “0”

| **AD_CV** (00 $BB_{hex}$) | | | **Automatic setting by STANDARD SELECT Register** | |
|---|---|---|---|---|
| **Bit** | **Function** | **Settings** | **2-8, 0A-51$_{hex}$** | **9** |
| [0] | not used | must be set to 0 | 0 | 0 |
| [1:6] | Reference level in case of Automatic Gain Control = on (see Table 6–10). Constant gain factor when Automatic Gain Control = off (see Table 6–11). | | 101000 | 100011 |
| [7] | Determination of Automatic Gain or Constant Gain | 0 = constant gain<br>1 = automatic gain | 1 | 1 |
| [8] | not used | must be set to 0 | 0 | 0 |
| [9] | MSP-Carrier-Mute Feature | 0 = off: no mute<br>1 = on: mute as described in Section 2.2.2. | 1 | 1 |
| [10:15] | not used | must be set to 0 | 0 | 0 |
| X: not affected while choosing the TV sound standard by means of the STANDARD SELECT Register | | | | |

**Note:** This register is initialized during STANDARD SELECTION and is automatically updated when Automatic Sound Select (MODUS[0]=1) is on.

**Table 6–10:** Reference values for active AGC (AD_CV[7] = 1)

| **Application** | **Input Signal Contains** | **AD_CV [6:1] Ref. Value** | **AD_CV [6:1] in decimal** | **Range of Input Signal at pin ANA_IN1+** |
|---|---|---|---|---|
| Terrestrial TV | | | | |
| – Dual Carrier FM | 2 FM Carriers | 101000 | 40 | 0.10 – 3 $V_{pp}$ [1)] |
| – NICAM/FM | 1 FM and 1 NICAM Carrier | 101000 | 40 | 0.10 – 3 $V_{pp}$ [1)] |
| – NICAM/AM | 1 AM and 1 NICAM Carrier | 100011 | 35 | 0.10 – 1.4 $V_{pp}$ (recommended: 0.10 – 0.8 $V_{pp}$) |
| – NICAM only | 1 NICAM Carrier only | 010100 | 20 | 0.05 – 1.0 $V_{pp}$ |
| SAT | 1 or more FM Carriers | 100011 | 35 | 0.10 – 3 $V_{pp}$ [1)] |

[1)] For signals above 1.4 Vpp, the minimum gain of 3 dB is switched, and overflow of the A/D converter may result. Due to the robustness of the internal processing, the IC works up to and even more than 3 Vpp, if norm conditions of FM/NICAM or FM1/FM2 ratio are supposed. In this overflow case, a loss of FM-S/N-ratio of about 10 dB may appear.

**Table 6–11:** AD_CV parameters for constant input gain (AD_CV[7]=0)

| Step | AD_CV [6:1] Constant Gain | Gain | Input Level at pin ANA_IN1+ and ANA_IN2+ |
|---|---|---|---|
| 0 | 000000 | 3.00 dB | maximum input level: 3 $V_{pp}$ (FM) or 1 $V_{pp}$ (NICAM)[1)] |
| 1 | 000001 | 3.85 dB | |
| 2 | 000010 | 4.70 dB | |
| 3 | 000011 | 5.55 dB | |
| 4 | 000100 | 6.40 dB | |
| 5 | 000101 | 7.25 dB | |
| 6 | 000110 | 8.10 dB | |
| 7 | 000111 | 8.95 dB | |
| 8 | 001000 | 9.80 dB | |
| 9 | 001001 | 10.65 dB | |
| 10 | 001010 | 11.50 dB | |
| 11 | 001011 | 12.35 dB | |
| 12 | 001100 | 13.20 dB | |
| 13 | 001101 | 14.05 dB | |
| 14 | 001110 | 14.90 dB | |
| 15 | 001111 | 15.75 dB | |
| 16 | 010000 | 16.60 dB | |
| 17 | 010001 | 17.45 dB | |
| 18 | 010010 | 18.30 dB | |
| 19 | 010011 | 19.15 dB | |
| 20 | 010100 | 20.00 dB | maximum input level: 0.14 $V_{pp}$ |

[1)] For signals above 1.4 Vpp, the minimum gain of 3 dB is switched, and overflow of the A/D converter may result. Due to the robustness of the internal processing, the IC works up to and even more than 3 Vpp, if norm conditions of FM/NICAM or FM1/FM2 ratio are supposed. In this overflow case, a loss of FM-S/N-ratio of about 10 dB may appear.

### 6.3.5. Register MODE_REG

**Note:** The use of this register is no longer recommended. It should be used only in cases where software compatibility to the MSP 34x7D is required. Using the STANDARD SELECTION register together with the MODUS register provides a more economic way to program the MSP 34x7G.

As soon as this register is applied, the MSP 34x7G works in the **MSP 34x7D Manual/Compatibility Mode**. In this mode, **BTSC, EIA-J, and FM-Radio are disabled**. Only MSP 34x7D features are available; the use of MODUS and STATUS register is not allowed. The MSP 34x7G is reset to the normal mode by first programming the MODUS register, followed by transmitting a valid standard code to the STANDARD SELECTION register.

The register 'MODE_REG' contains the control bits determining the operation mode of the MSP 34x7G in the MSP 34x7D Manual/Compatibility Mode; Table 6–12 explains all bit positions.

**Table 6–12:** Control word 'MODE_REG'; reset status: all bits are "0"

| **MODE_REG 00 83$_{hex}$** | | | | **Automatic setting by STANDARD SELECT Register** | | |
|---|---|---|---|---|---|---|
| **Bit** | **Function** | **Comment** | **Definition** | **2 - 5** | **8,A,B** | **9** |
| [0] | not used | | 0 : must be used | 0 | 0 | 0 |
| [1] | DCTR_TRI | Digital control out 0/1 tri-state | 0 : active<br>1 : tri-state | X | X | X |
| [2] | not used | | 1 : recommended | X | X | X |
| [3] | not used | | 0 : must be used | X | X | X |
| [4] | not used | | 0 : must be used | X | X | X |
| [5] | not used | | 1 : recommended | X | X | X |
| [6] | NICAM | Mode of MSP-Ch1 | 0 : FM<br>1 : Nicam | 0 | 1 | 1 |
| [7] | not used | | 0 : must be used | 0 | 0 | 0 |
| [8] | FM AM | Mode of MSP-Ch2 | 0 : FM<br>1 : AM | 0 | 0 | 1 |
| [9] | HDEV | High Deviation Mode (channel matrix must be sound A) | 0 : normal<br>1 : high deviation mode | 0 | 0 | 0 |
| [11:10] | not used | | 0 : must be used | 0 | 0 | 0 |
| [12] | MSP-Ch1 Gain | see also Table 6–14 | 0 : Gain = 6 dB<br>1 : Gain = 0 dB | 0 | 0 | 0 |
| [13] | FIR1-Filter Coeff. Set | see also Table 6–14 | 0 : use FIR1<br>1 : use FIR2 | 1 | 0 | 0 |
| [14] | not used | | 0 : recommended | 0 | 0 | 0 |
| [15] | AM-Gain | Gain for AM Demodulation | 0 : 0 dB (default. of MSPB)<br>1 : 12 dB (recommended) | 1 | 1 | 1 |
| | | | | X: not affected by STANDARD SELECT Register | | |

**Table 6–13:** Loading sequence for FIR-coefficients

| **FIR1 00 $01_{hex}$ (MSP-Ch1: NICAM/FM2)** | | | |
|---|---|---|---|
| **No.** | **Symbol Name** | **Bits** | **Value** |
| 1 | NICAM/FM2_Coeff. (5) | 8 | see Table 6–14 |
| 2 | NICAM/FM2_Coeff. (4) | 8 | |
| 3 | NICAM/FM2_Coeff. (3) | 8 | |
| 4 | NICAM/FM2_Coeff. (2) | 8 | |
| 5 | NICAM/FM2_Coeff. (1) | 8 | |
| 6 | NICAM/FM2_Coeff. (0) | 8 | |
| **FIR2 00 $05_{hex}$ (MSP-Ch2: FM1/AM)** | | | |
| No. | Symbol Name | Bits | Value |
| 1 | IMREG1 | 8 | $04_{hex}$ |
| 2 | IMREG1 / IMREG2 | 8 | $40_{hex}$ |
| 3 | IMREG2 | 8 | $00_{hex}$ |
| 4 | FM/AM_Coef (5) | 8 | see Table 6–14 |
| 5 | FM/AM_Coef (4) | 8 | |
| 6 | FM/AM_Coef (3) | 8 | |
| 7 | FM/AM_Coef (2) | 8 | |
| 8 | FM/AM_Coef (1) | 8 | |
| 9 | FM/AM_Coef (0) | 8 | |

### 6.3.6. FIR-Parameter, Registers FIR1 and FIR2

**Note:** The use of this register is no longer recommended. Use it only in cases where software compatibility to the MSP 34x7D is required. Using the STANDARD SELECTION register together with the MODUS register provides a more economic way to program the MSP 34x7G.

Data shaping and/or FM/AM bandwidth limitation is performed by a pair of linear phase Finite Impulse Response filters (FIR-filter). The filter coefficients are programmable and either are configured automatically by the STANDARD SELECT register or written manually by the control processor via the control bus. Two not necessarily different sets of coefficients are required: one for MSP-Ch1 (NICAM or FM2) and one for MSP-Ch2 (FM1 = FM-mono). In Table 6–14 several coefficient sets are proposed.

To load the FIR-filters, the following data values are to be transferred **8 bits at a time embedded LSB-bound in a 16-bit word**.

The loading sequences must be obeyed. To change a coefficient set, the complete block FIR1 or FIR2 must be transmitted.

**Note:** For compatibility with MSP 3410B, IMREG1 and IMREG2 have to be transmitted. The value for IMREG1 and IMREG2 is 004. Due to the partitioning to 8-bit units, the values $04_{hex}$, $40_{hex}$, and $00_{hex}$ arise.

### 6.3.7. DCO-Registers

**Note:** The use of this register is no longer recommended. It should be used only in cases where software compatibility to the MSP 34x7D is required. Using the STANDARD SELECTION register together with the MODUS register provides a more economic way to program the MSP 34x7G.

When selecting a TV-sound standard by means of the STANDARD SELECT register, all frequency tuning is performed automatically.

IF manual setting of the tuning frequency is required, a set of 24-bit registers determining the mixing frequencies of the quadrature mixers can be written manually into the IC. In Table 6–15, some examples of DCO registers are listed. It is necessary to divide them up into low part and high part. The formula for the calculation of the registers for any chosen IF-Frequency is as follows:

$$INCR_{dec} = int(f/fs \cdot 2^{24})$$

with: int = integer function
f = IF-frequency in MHz
$f_S$ = sampling frequency (18.432 MHz)

Conversion of INCR into hex-format and separation of the 12-bit low and high parts lead to the required register values (DCO1_HI or _LO for MSP-Ch1, DCO2_HI or LO for MSP-Ch2).

**Table 6–14:** 8-bit FIR-coefficients (decimal integer); reset status: all coefficients are “0”

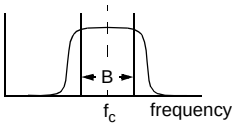
| Coefficients for FIR1 00 $01_{hex}$ and FIR2 00 $05_{hex}$ | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Terrestrial TV Standards | | | | | | | FM - Satellite FIR filter corresponds to a band-pass with a band-width of B = 130 to 500 kHz   | | | | | | |
| | B/G-, D/K-NICAM-FM | | I-NICAM-FM | | L-NICAM-AM | | B/G-, D/K-, M-Dual FM | 130 kHz | 180 kHz | 200 kHz | 280 kHz | 380 kHz | 500 kHz | Auto-search |
| **Coef(i)** | **FIR1** | **FIR2** | **FIR1** | **FIR2** | **FIR1** | **FIR2** | **FIR2** | **FIR2** | **FIR2** | **FIR2** | **FIR2** | **FIR2** | **FIR2** | **FIR2** |
| **0** | –2 | 3 | 2 | 3 | –2 | –4 | 3 | 73 | 9 | 3 | –8 | –1 | –1 | –1 |
| **1** | –8 | 18 | 4 | 18 | –8 | –12 | 18 | 53 | 18 | 18 | –8 | –9 | –1 | –1 |
| **2** | –10 | 27 | –6 | 27 | –10 | –9 | 27 | 64 | 28 | 27 | 4 | –16 | –8 | –8 |
| **3** | 10 | 48 | –4 | 48 | 10 | 23 | 48 | 119 | 47 | 48 | 36 | 5 | 2 | 2 |
| **4** | 50 | 66 | 40 | 66 | 50 | 79 | 66 | 101 | 55 | 66 | 78 | 65 | 59 | 59 |
| **5** | 86 | 72 | 94 | 72 | 86 | 126 | 72 | 127 | 64 | 72 | 107 | 123 | 126 | 126 |
| **Mode-REG[12]** | 0 | | 0 | | 0 | | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| **Mode-REG[13]** | 0 | | 0 | | 0 | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| For compatibility, except for the FIR2-AM and the Autosearch-sets, the FIR-filter programming as used for the MSP 3410B is also possible. | | | | | | | | | | | | | | |

**Table 6–15:** DCO registers for the MSP 34x7G; reset status: DCO_HI/LO = “0000”

| DCO1_LO 00 $93_{hex}$, DCO1_HI 00 $9B_{hex}$; DCO2_LO 00 $A3_{hex}$, DCO2_HI 00 $AB_{hex}$ | | | | | |
|---|---|---|---|---|---|
| **Freq. MHz** | **DCO_HI/hex** | **DCO_LO/hex** | **Freq. MHz** | **DCO_HI/hex** | **DCO_LO/hex** |
| 4.5 | 03E8 | 0000 | | | |
| 5.04<br>5.5<br>5.58<br>5.7421875 | 0460<br>04C6<br>04D8<br>04FC | 0000<br>038E<br>0000<br>00AA | 5.76<br>5.85<br>5.94 | 0500<br>0514<br>0528 | 0000<br>0000<br>0000 |
| 6.0<br>6.2<br>6.5<br>6.552 | 0535<br>0561<br>05A4<br>05B0 | 0555<br>0C71<br>071C<br>0000 | 6.6<br>6.65<br>6.8 | 05BA<br>05C5<br>05E7 | 0AAA<br>0C71<br>01C7 |
| 7.02 | 0618 | 0000 | 7.2 | 0640 | 0000 |
| 7.38 | 0668 | 0000 | 7.56 | 0690 | 0000 |

### 6.4. Manual/Compatibility Mode: Description of Demodulator Read Registers

**Note:** The use of these register is no longer recommended. It should be used only in cases where software compatibility to the MSP 34x7D is required. Using the STANDARD SELECTION register together with the STATUS register provides a more economic way to program the MSP 34x7G and to retrieve information from the IC.

All registers except C_AD_BITs are 8 bit wide. They can be read out of the RAM of the MSP 34x7G if the MSP 34x7D compatibility mode is required.

All transmissions take place in 16-bit words. The valid 8-bit data are the 8 LSBs of the received data word.

If the Automatic Sound Select feature is not used, the NICAM or FM-identification parameters must be read and evaluated by the controller in order to enable appropriate switching of the channel select matrix of the baseband processing part. The FM-identification registers are described in Section 6.6.1. To handle the NICAM-sound and to observe the NICAM-quality, at least the registers C_AD_BITS and ERROR_RATE must be read and evaluated by the controller. Additional data bits and CIB bits, if supplied by the NICAM transmitter, can be obtained by reading the registers ADD_BITS and CIB_BITS.

#### 6.4.1. NICAM Mode Control/Additional Data Bits Register

NICAM operation mode control bits and A[2:0] of the additional data bits.

Format:

| MSB | | | | C_AD_BITS 00 $23_{hex}$ | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|
| 11 | ... | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Auto _FM | ... | A[2] | A[1] | A[0] | C4 | C3 | C2 | C1 | S |

**Important:** “S” = bit[0] indicates correct NICAM-synchronization (S = 1). If S = 0, the MSP 3417/3457G has not yet synchronized correctly to frame and sequence, or has lost synchronization. The remaining read registers are therefore not valid. The MSP mutes the NICAM output automatically and tries to synchronize again as long as MODE_REG[6] is set.

The operation mode is coded by C4-C1 as shown in Table 6–16.

**Table 6–16:** NICAM operation modes as defined by the EBU NICAM 728 specification

| C4 | C3 | C2 | C1 | Operation Mode |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Stereo sound (NICAMA/B), independent mono sound (FM1) |
| 0 | 0 | 0 | 1 | Two independent mono signals (NICAMA, FM1) |
| 0 | 0 | 1 | 0 | Three independent mono channels (NICAMA, NICAMB, FM1) |
| 0 | 0 | 1 | 1 | Data transmission only; no audio |
| 1 | 0 | 0 | 0 | Stereo sound (NICAMA/B), FM1 carries same channel |
| 1 | 0 | 0 | 1 | One mono signal (NICAMA). FM1 carries same channel as NICAMA |
| 1 | 0 | 1 | 0 | Two independent mono channels (NICAMA, NICAMB). FM1 carries same channel as NICAMA |
| 1 | 0 | 1 | 1 | Data transmission only; no audio |
| x | 1 | x | x | Unimplemented sound coding option (not yet defined by EBU NICAM 728 specification) |
| AUTO_FM: monitor bit for the AUTO_FM Status:<br>0: NICAM source is NICAM<br>1: NICAM source is FM | | | | |

**Note:** It is no longer necessary to read out and evaluate the C_AD_BITS. All evaluation is performed in the MSP and indicated in the STATUS register.

#### 6.4.2. Additional Data Bits Register

Contains the remaining 8 of the 11 additional data bits. The additional data bits are not yet defined by the NICAM 728 system.

Format:

| MSB | | | | ADD_BITS 00 $38_{hex}$ | | | LSB |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| A[10] | A[9] | A[8] | A[7] | A[6] | A[5] | A[4] | A[3] |

#### 6.4.3. CIB Bits Register

Cib bits 1 and 2 (see NICAM 728 specifications).

Format:

| MSB | | | | CIB_BITS 00 $3E_{hex}$ | | | LSB |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| x | x | x | x | x | x | CIB1 | CIB2 |

### 6.4.4. NICAM Error Rate Register

| ERROR_RATE | 00 $57_{hex}$ |
|---|---|
| Error free | $0000_{hex}$ |
| maximum error rate | $07FF_{hex}$ |

Average error rate of the NICAM reception in a time interval of 182 ms, which should be close to 0. The initial and maximum value of ERROR_RATE is 2047. This value is also active if the NICAM bit of MODE_REG is not set. Since the value is achieved by filtering, a certain transition time (approx. 0.5 sec) is unavoidable. Acceptable audio may have error rates up to a value of 700 int. Individual evaluation of this value by the controller and an appropriate threshold may define the fallback mode from NICAM to FM/ AM-mono in case of poor NICAM reception.

The bit error rate per second (BER) can be calculated by means of the following formula:

BER= ERROR_RATE * $12.3*10^{-6}$ /s

### 6.4.5. PLL_CAPS Readback Register

It is possible to read out the actual setting of the PLL_CAPS. In standard applications, this register is not of interest for the customer.

| PLL_CAPS | 02 $1F_{hex}$ L | |
|---|---|---|
| minimum frequency | 1111 1111 | $FF_{hex}$ |
| nominal frequency | 0101 0110<br>RESET | $56_{hex}$ |
| maximum frequency | 0000 0000 | $00_{hex}$ |
| **PLL_CAPS** | **02 $1F_{hex}$ H** | |
| PLL open | xxxx xxx0 | |
| PLL closed | xxxx xxx1 | |

### 6.4.6. AGC_GAIN Readback Register

It is possible to read out the actual setting of AGC_GAIN in Automatic Gain Mode. In standard applications, this register is not of interest for the customer .

| AGC_GAIN | 02 $1E_{hex}$ | |
|---|---|---|
| max. amplification<br>(20 dB) | 0001 0100 | $14_{hex}$ |
| min. amplification<br>(3 dB) | 0000 0000 | $00_{hex}$ |

### 6.4.7. Automatic Search Function for FM-Carrier Detection in Satellite Mode

The AM demodulation ability of the MSP 3417G and MSP 3457G offers the possibility to calculate the “field strength” of the momentarily selected FM carrier, which can be read out by the controller. In SAT receivers, this feature can be used to make automatic FM carrier search possible.

For this, the MSP has to be switched to AM-mode (MODE_REG[8]), FM-Prescale must be set to $7F_{hex}$= $+127_{dec}$, and the FM DC notch (see Section 6.5.7.) must be switched off. The sound-IF frequency range must now be “scanned” in the MSP-channel 2 by means of the programmable quadrature mixer with an appropriate incremental frequency (i.e. 10 kHz). After each incrementation, a field strength value is available at the quasi-peak detector output (quasi-peak detector source must be set to FM), which must be examined for relative maxima by the controller. This results in either continuing search or switching the MSP back to FM demodulation mode.

During the search process, the FIR2 must be loaded with the coefficient set “AUTOSEARCH”, which enables small bandwidth, resulting in appropriate field strength characteristics. The absolute field strength value (can be read out of “quasi peak detector output FM1”) also gives information on whether a main FM carrier or a subcarrier was detected; and as a practical consequence, the FM bandwidth (FIR1/2) and the deemphasis (50 µs or adaptive) can be switched accordingly.

Due to the fact that a constant demodulation frequency offset of a few kHz, leads to a DC level in the demodulated signal, further fine tuning of the found carrier can be achieved by evaluating the “DC Level Readout FM1”. Therefore, the FM DC Notch must be switched on, and the demodulator part must be switched back to FM-demodulation mode.

For a detailed description of the automatic search function, please refer to the corresponding MSP Windows software.

## 6.5. Manual/Compatibility Mode: Description of DSP Write Registers

### 6.5.1. Additional Channel Matrix Modes

| **Loudspeaker Matrix** | **00 $08_{hex}$** | **L** |
|---|---|---|
| **SCART1 Matrix** | **00 $0A_{hex}$** | **L** |
| **Quasi-Peak Detector Matrix** | **00 $0C_{hex}$** | **L** |
| SUM/DIFF | 0100 0000 | $40_{hex}$ |
| AB_XCHANGE | 0101 0000 | $50_{hex}$ |
| PHASE_CHANGE_B | 0110 0000 | $60_{hex}$ |
| PHASE_CHANGE_A | 0111 0000 | $70_{hex}$ |
| A_ONLY | 1000 0000 | $80_{hex}$ |
| B_ONLY | 1001 0000 | $90_{hex}$ |

This table shows more modes for the channel matrix registers.

The sum/difference mode can be used together with the quasi-peak detector to determine the sound material mode. If the difference signal on channel B (right) is near to zero, and the sum signal on channel A (left) is high, the incoming audio signal is mono. If there is a significant level on the difference signal, the incoming audio is stereo.

### 6.5.2. Volume Modes of SCART1 Output

| **Volume Mode SCART1** | **00 $07_{hex}$** | **[3:0]** |
|---|---|---|
| linear | 0000 RESET | $0_{hex}$ |
| logarithmic | 0001 | $1_{hex}$ |

| **Linear Mode** | | |
|---|---|---|
| **Volume SCART1** | **00 $07_{hex}$** | **H** |
| OFF | 0000 0000 RESET | $00_{hex}$ |
| 0 dB gain (digital full scale to 2 $V_{RMS}$ output) | 0100 0000 | $40_{hex}$ |
| +6 dB gain (–6 dBFS to 2 $V_{RMS}$ output) | 0111 1111 | $7F_{hex}$ |

### 6.5.3. FM Fixed Deemphasis

| **FM Deemphasis** | **00 $0F_{hex}$** | **H** |
|---|---|---|
| 50 µs | 0000 0000 RESET | $00_{hex}$ |
| 75 µs | 0000 0001 | $01_{hex}$ |
| J17 | 0000 0100 | $04_{hex}$ |
| OFF | 0011 1111 | $3F_{hex}$ |

**Note:** This register is initialized during STANDARD SELECTION and is automatically updated when Automatic Sound Select (MODUS[0]=1) is on.

### 6.5.4. FM Adaptive Deemphasis

| **FM Adaptive Deemphasis WP1** | **00 $0F_{hex}$** | **L** |
|---|---|---|
| OFF | 0000 0000 RESET | $00_{hex}$ |
| WP1 | 0011 1111 | $3F_{hex}$ |

**Note:** This register is initialized during STANDARD SELECTION and is automatically updated when Automatic Sound Select (MODUS[0]=1) is on.

### 6.5.5. NICAM Deemphasis

A J17 Deemphasis is always applied to the NICAM signal. It is not switchable.

### 6.5.6. Identification Mode for A2 Stereo Systems

| Identification Mode | 00 $15_{hex}$ | L |
|---|---|---|
| Standard B/G (German Stereo) | 0000 0000 RESET | $00_{hex}$ |
| Standard M (Korean Stereo) | 0000 0001 | $01_{hex}$ |
| Reset of Ident-Filter | 0011 1111 | $3F_{hex}$ |

To shorten the response time of the identification algorithm after a program change between two FM-Stereo capable programs, the reset of the ident-filter can be applied.

Sequence:

1. Program change
2. Reset ident-filter
3. Set identification mode back to standard B/G or M
4. Wait approx. 500 ms
5. Read stereo detection register

**Note:** This register is initialized during STANDARD SELECTION and is automatically updated when Automatic Sound Select (MODUS[0]=1) is on.

### 6.5.7. FM DC Notch

The DC compensation filter (FM DC Notch) for FM input can be switched off. This is used to speed up the automatic search function (see Section 6.4.7.). In normal FM-mode, the FM DC Notch should be switched on.

| FM DC Notch | 00 $17_{hex}$ | L |
|---|---|---|
| ON | 0000 0000 Reset | $00_{hex}$ |
| OFF | 0011 1111 | $3F_{hex}$ |

### 6.6. Manual/Compatibility Mode: Description of DSP Read Registers

All readable registers are 16-bit wide. Transmissions via $I^2C$ bus have to take place in 16-bit words. Some of the defined 16-bit words are divided into low and high byte, thus holding two different control entities.

These registers are not writable.

### 6.6.1. Stereo Detection Register for A2 Stereo Systems

| Stereo Detection Register | 00 $18_{hex}$ | H |
|---|---|---|
| MONO | near zero | |
| STEREO | positive value (ideal reception: $7F_{hex}$) | |
| BILINGUAL | negative value (ideal reception: $80_{hex}$) | |

**Note:** It is no longer necessary to read out and evaluate the A2 identification level. All evaluation is performed in the MSP and indicated in the STATUS register.

### 6.6.2. DC Level Register

| DC Level Readout FM1 (MSP-Ch2) | 00 $1B_{hex}$ | H+L |
|---|---|---|
| DC Level Readout FM2 (MSP-Ch1) | 00 $1C_{hex}$ | H+L |
| DC Level | [$8000_{hex}$ ... $7FFF_{hex}$] values are 16 bit two's complement | |

The DC level register measures the DC component of the incoming FM signals (FM1 and FM2). This can be used for seek functions in satellite receivers and for IF FM frequencies fine tuning. A too low demodulation frequency (DCO) results in a positive DC-Level and vice versa. For further processing, the DC content of the demodulated FM signals is suppressed. The time constant $\tau$, defining the transition time of the DC Level Register, is approximately 28 ms.

## 6.7. Demodulator Source Channels in Manual Mode

### 6.7.1. Terrestric Sound Standards

Table 6–17 shows the source channel assignment of the demodulated signals in case of manual mode for all terrestric sound standards. See Table 2–2 for the assignment in the Automatic Sound Select mode. In manual mode for terrestric sound standards, only two demodulator sources are defined.

### 6.7.2. SAT Sound Standards

Table 6–18 shows the source channel assignment of the demodulated signals for SAT sound standards.

## 6.8. Exclusions of Audio Baseband Features

In general, all functions can be switched independently. Two exceptions exist:

1. NICAM cannot be processed simultaneously with the FM2 channel.
2. FM adaptive deemphasis cannot be processed simultaneously with FM-identification.

## 6.9. Compatibility Restrictions to MSP 34x7D

The MSP 34x7G is fully hardware compatible to the MSP 34x7D. However, to substitute a MSP 34x7D by the corresponding MSP 34x7G, the controller software has to be adapted slightly:

1. The register FM-Matrix (00 $0E_{hex}$ low part) must be changed from “no matrix ($00_{hex}$)” to “sound A mono ($03_{hex}$)” during mono transmission of all TV-sound standards (see also Table 6–17).
2. With the MSP 34x7G, the STANDARD SELECTION initializes the FM-deemphasis, which is not the case for the MSP 34x7D. So, if STANDARD SELECTION is applied, this $I^2C$ instruction can be omitted.

**Table 6–17:** Manual Sound Select Mode for Terrestric Sound Standards

| | | | | Source Channels of Sound Select Block | |
|---|---|---|---|---|---|
| **Broadcasted Sound Standard** | **Selected MSP Standard Code** | **Broadcasted Sound Mode** | **FM Matrix** | **FM/AM** (use 0 for channel select) | **Stereo or A/B** (use 1 for channel select) |
| B/G-FM<br>D/K-FM<br>M-Korea<br>M-Japan | 03<br>04, 05<br>02<br>30 | MONO | Sound A Mono | Mono | Mono |
| | | STEREO | German Stereo<br>Korean Stereo | Stereo | Stereo |
| | | BILINGUAL, Languages A and B | No Matrix | Left = A<br>Right = B | Left = A<br>Right = B |
| B/G-NICAM<br>L-NICAM<br>I-NICAM<br>D/K-NICAM<br>D/K-NICAM (with high deviation FM) | 08<br>09<br>0A<br>0B<br>0C<br>0D | NICAM not available or NICAM error rate too high | Sound A Mono[1)] | analog Mono | no sound<br>with AUTO_FM: analog Mono |
| | | MONO | Sound A Mono[1)] | analog Mono | NICAM Mono |
| | | STEREO | Sound A Mono[1)] | analog Mono | NICAM Stereo |
| | | BILINGUAL, Languages A and B | Sound A Mono[1)] | analog Mono | Left = NICAM A<br>Right = NICAM B |
| BTSC | 20 | MONO | Sound A Mono | Mono | Mono |
| | | STEREO | Korean Stereo | Stereo | Stereo |
| | | MONO + SAP | Sound A Mono | Mono | Mono |
| | | STEREO + SAP | Korean Stereo | Stereo | Stereo |
| | 21 | MONO | Sound A Mono | Mono | Mono |
| | | STEREO | | | |
| | | MONO + SAP | No Matrix | Left = Mono<br>Right = SAP | Left = Mono<br>Right = SAP |
| | | STEREO + SAP | | | |
| FM-Radio | 40 | MONO | Sound A Mono | Mono | Mono |
| | | STEREO | Korean Stereo | Stereo | Stereo |

[1)] Automatic refresh to Sound A Mono, do not write any other value to the register FM Matrix!

**Table 6–18:** Manual Sound Select Modes for SAT-Standards

| | | | | Source Channels of Sound Select Block for SAT-Modes | | | |
|---|---|---|---|---|---|---|---|
| **Broadcasted Sound Standard** | **Selected MSP Standard Code** | **Broadcasted Sound Mode** | **FM Matrix** | **FM/AM** (source select: 0) | **Stereo or A/B** (source select: 1) | **Stereo or A** (source select: 3) | **Stereo or B** (source select: 4) |
| FM SAT | $6, 50_{hex}$ | MONO | Sound A Mono | Mono | Mono | Mono | Mono |
| | $51_{hex}$ | STEREO | No Matrix | Stereo | Stereo | Stereo | Stereo |
| | | BILINGUAL | No Matrix | Left = A (FM1)<br>Right = B (FM2) | Left = A (FM1)<br>Right = B (FM2) | A (FM1) | B (FM2) |

## 7. Appendix D: Application Information

### 7.1. Phase Relationship of Analog Outputs

The user does not need to correct output phases when using the loudspeaker output directly. The SCART1 output has opposite phase.

The following schematics shows the phase relationship of all analog inputs and outputs.

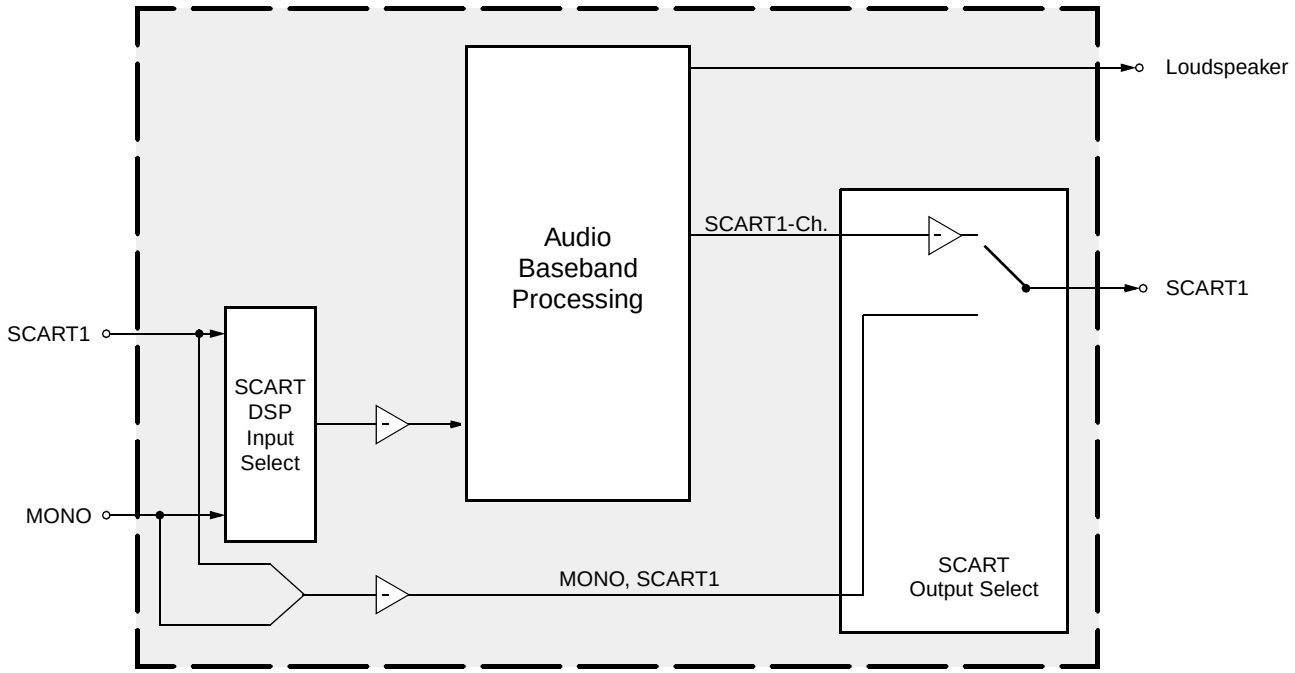
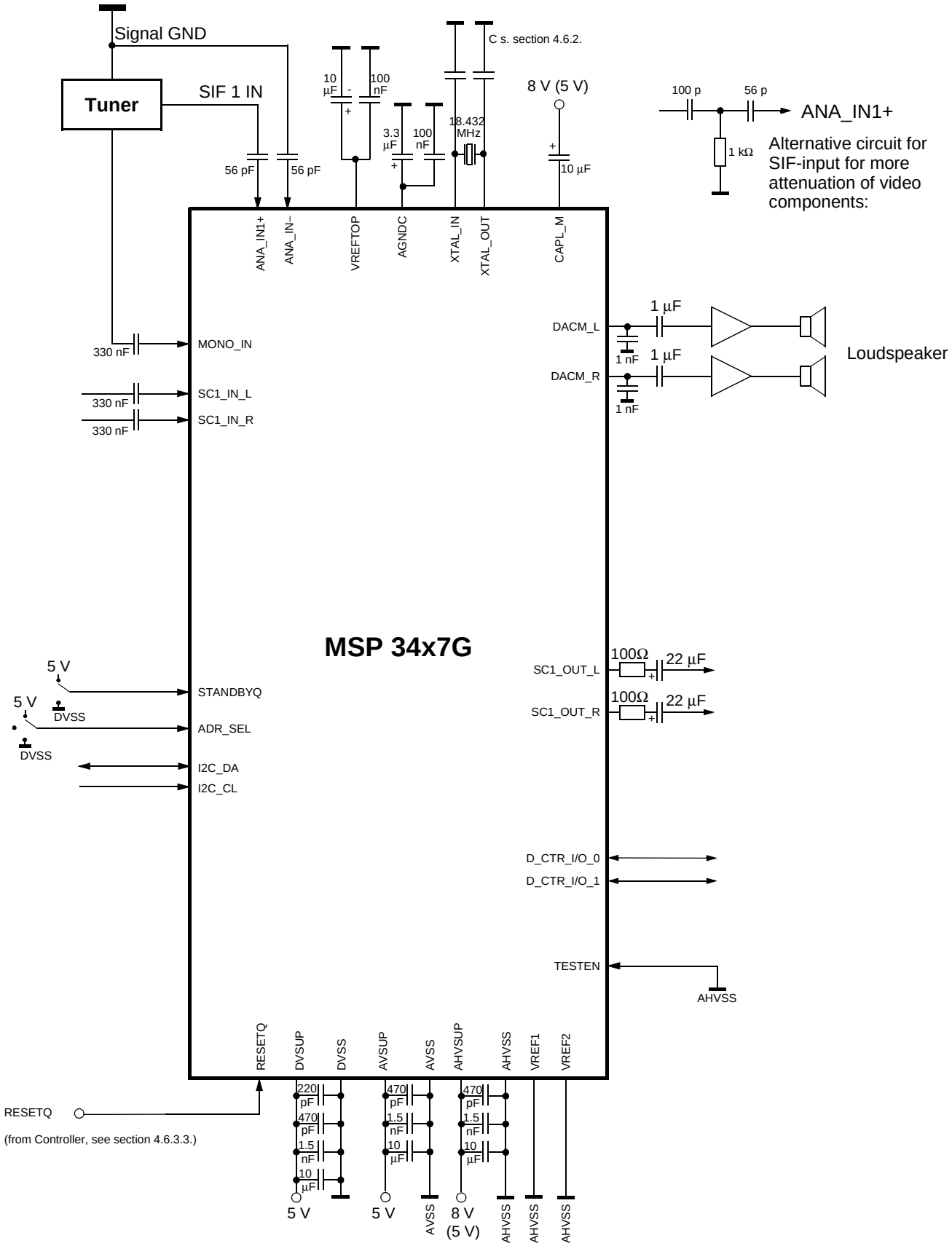



**Fig. 7–1:** Phase diagram of the MSP 34x7G

### 7.2. Application Circuit



## 8. Appendix E: MSP 34x7G Version History

### MSP 34x7G-B6

– improved AM-performance (see page 53)

– new D/K standard for Poland (see Table 3–7 on page 18)

– improved $I^2C$ hardware problem handling (see Section 3.1.1. on page 14)

– faster system-D/K-loop for stereo detection

– extended features in the CONTROL register (see Section 3.1.2. on page 15)

### MSP 34x7G-B8

– fine-tuning of A2-identification and carrier mute

– EIA-J identification: faster transition time stereo/ bilingual to mono

– J17 FM-deemphasis implemented

– input specification for RESETQ and TESTEN changed

## 9. Data Sheet History

1. Preliminary data sheet: “MSP 34x7G Multistandard Sound Processor Family”, Edition Sept. 7, 2000, 6251-535-1PD. First release of the preliminary data sheet.

2. Preliminary data sheet: “MSP 34x7G Multistandard Sound Processor Family”, March 5, 2001, 6251-535-2PD. Second release of the preliminary data sheet. Major changes:

– $I^2C$-bus description changed

– ACB register: documentation for bit allocation D_CTR_I/O changed

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Printed in Germany
Order No. 6251-535-2PD

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# Preliminary Data Sheet Supplement

| | |
|---|---|
| **Subject:** | MSP 34xxG Version History |
| **Data Sheet Concerned:** | All MSP 34xxG Data Sheets |
| **Supplement:** | No. 2/ 6251-525-2PDS |
| **Edition:** | Oct. 11, 2000 |

**Version Changes within the MSP 34xxG Family:**

For a detailed description of the below-mentioned items, see the corresponding data sheets. For quick reference, check the version history in the data sheet appendices.

| | | | | | | |
|---|---|---|---|---|---|---|
| | **MSP 34x0G** | **A4** | **B4** | **B5** | **B6** | **B8** |
| | **MSP 34x1G** | | **A1** | | **A2** | **B8** |
| | **MSP 34x2G** | | | | **A1** | |
| | **MSP 34x5G** | **A4** | | **B5** | **B6** | **B8** |
| | **MSP 34x7G** | | | | **B6** | **B8** |
| technology | | 0.8 µ | 0.5 µ | 0.5 µ | 0.5 µ | 0.45 µ |
| power dissipation (typical) at 8 V operation | MSP 34x0/x1/x5/x7<br>MSP 34x2 | 740 mW | 640 mW | 640 mW | 640 mW<br>690 mW | 600 mW |
| digital input specification change | | | | x | x | x |
| specification of max. analog high voltage (AHVSUP) | | 8.4 V | 8.4 V | 8.7 V | 8.7 V | 8.7 V |
| programmable A2 and carrier mute thresholds | | | | x | x | x |
| new Standard Select Mode $0D_{hex}$: D/K-NICAM together with HDEV3 FM mode | | | | x | x | x |
| additional preference “color” for 4.5 MHz carrier in Automatic Standard Detection | | | | x | x | x |
| improved AM-performance (better SNR and THD) | | | | | x | x |
| new Standard Select Mode $07_{hex}$: D/K3 for Poland | | | | | x | x |
| faster system D/K loop for stereo detection (standards 4, 5, 7, B with ASS = on) | | | | | x | x |
| improved $I^2C$ hardware problem handling | | | | | x | x |
| extended features in the CONTROL register (readout hardware / reset status) | | | | | x | x |
| Micronas Dynamic Bass (MDB) | MSP 34x0/x1/x2 | | | | x | x |
| Micronas Dynamic Bass (improved MDB) | MSP 34x0/x1/x2 | | | | | x |
| faster identification for all standards, major speedup of identification for EIA-J standard | | | | | | x |
| faster carrier mute | | | | | | x |
| J17 deemphasis | | | | | | x |