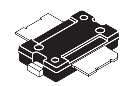
## The RF Sub–Micron MOSFET Line

# RF Power Field Effect Transistor

## N–Channel Enhancement–Mode Lateral MOSFET

**MRF9045M**
**MRF9045MR1**

**945 MHz, 45 W, 28 V**
**LATERAL N–CHANNEL**
**BROADBAND**
**RF POWER MOSFET**



**CASE 1265–06, STYLE 1**
**(TO–270)**

**PLASTIC**

Designed for broadband commercial and industrial applications at frequencies up to 1.0 GHz. The high gain and broadband performance of this device make it ideal for large–signal, common–source amplifier applications in 28 volt base station equipment.

- Typical Performance at 945 MHz, 28 Volts
  - Output Power – 45 Watts PEP
  - Power Gain – 18.5 dB
  - Efficiency – 41% (Two Tones)
  - IMD – –31 dBc
- Integrated ESD Protection
- Guaranteed Ruggedness @ Load VSWR = 5:1, @ 28 Vdc, 945 MHz, 45 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Moisture Sensitivity Level 3
- RF Power Plastic Surface Mount Package
- Available in Tape and Reel. R1 Suffix = 500 Units per 24 mm, 13 inch Reel.

### MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 65 | Vdc |
| Gate–Source Voltage | $V_{GS}$ | +15, –0.5 | Vdc |
| Total Device Dissipation @ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | 156(1)<br>1.25(1) | Watts<br>W/°C |
| Storage Temperature Range | $T_{stg}$ | –65 to +150 | °C |
| Operating Junction Temperature | $T_J$ | 150 | °C |

### ESD PROTECTION CHARACTERISTICS

| Test Conditions | Class |
|---|---|
| Human Body Model | 1 (Typical) |
| Machine Model | M2 (Typical) |

### THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance, Junction to Case | $R_{\theta JC}$ | 0.8(1) | °C/W |

(1) Simulated

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

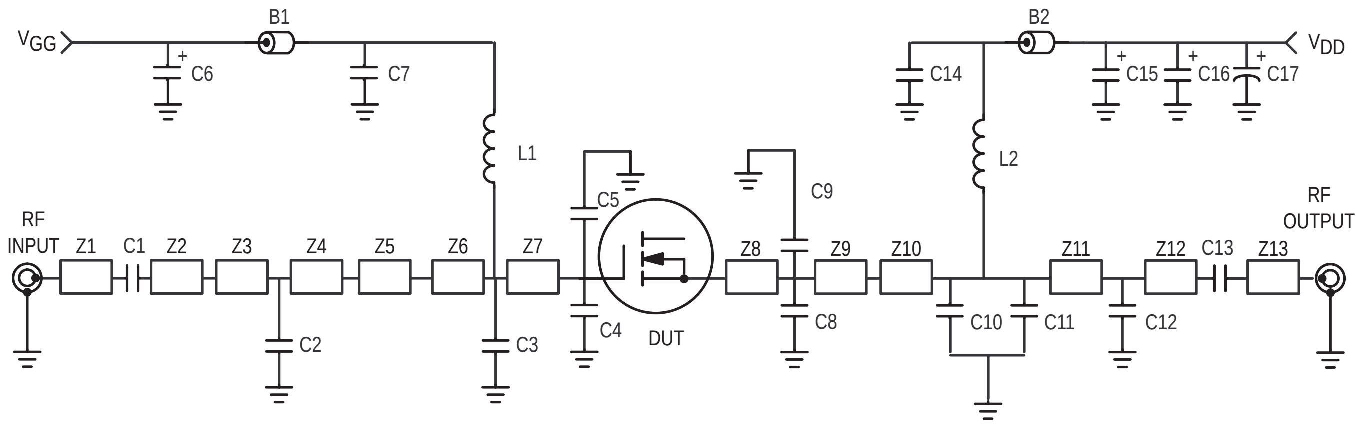
**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Zero Gate Voltage Drain Leakage Current ($V_{DS}$ = 65 Vdc, $V_{GS}$ = 0) | $I_{DSS}$ | — | — | 10 | µAdc |
| Zero Gate Voltage Drain Leakage Current ($V_{DS}$ = 28 Vdc, $V_{GS}$ = 0) | $I_{DSS}$ | — | — | 1 | µAdc |
| Gate–Source Leakage Current ($V_{GS}$ = 5 Vdc, $V_{DS}$ = 0 ) | $I_{GSS}$ | — | — | 1 | µAdc |
| **ON CHARACTERISTICS** | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = 10 Vdc, $I_D$ = 150 µAdc) | $V_{GS(th)}$ | 2 | — | 4 | Vdc |
| Gate Quiescent Voltage ($V_{DS}$ = 28 Vdc, $I_D$ = 350 mAdc) | $V_{GS(Q)}$ | — | 3.7 | — | Vdc |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc, $I_D$ = 1 Adc) | $V_{DS(on)}$ | — | 0.19 | 0.4 | Vdc |
| Forward Transconductance ($V_{DS}$ = 10 Vdc, $I_D$ = 3 Adc) | $g_{fs}$ | — | 4 | — | S |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Input Capacitance ($V_{DS}$ = 28 Vdc, $V_{GS}$ = 0, f = 1 MHz) | $C_{iss}$ | — | 74 | — | pF |
| Output Capacitance ($V_{DS}$ = 28 Vdc, $V_{GS}$ = 0, f = 1 MHz) | $C_{oss}$ | — | 39 | — | pF |
| Reverse Transfer Capacitance ($V_{DS}$ = 28 Vdc, $V_{GS}$ = 0, f = 1 MHz) | $C_{rss}$ | — | 1.9 | — | pF |

(continued)

**ELECTRICAL CHARACTERISTICS — continued** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **FUNCTIONAL TESTS** (In Motorola Test Fixture) | | | | | |
| Two–Tone Common–Source Amplifier Power Gain ($V_{DD}$ = 28 Vdc, $P_{out}$ = 45 W PEP, $I_{DQ}$ = 350 mA, f1 = 945.0 MHz, f2 = 945.1 MHz) | $G_{ps}$ | 17 | 18.5 | — | dB |
| Two–Tone Drain Efficiency ($V_{DD}$ = 28 Vdc, $P_{out}$ = 45 W PEP, $I_{DQ}$ = 350 mA, f1 = 945.0 MHz, f2 = 945.1 MHz) | η | 38 | 41 | — | % |
| 3rd Order Intermodulation Distortion ($V_{DD}$ = 28 Vdc, $P_{out}$ = 45 W PEP, $I_{DQ}$ = 350 mA, f1 = 945.0 MHz, f2 = 945.1 MHz) | IMD | — | –31 | –28 | dBc |
| Input Return Loss ($V_{DD}$ = 28 Vdc, $P_{out}$ = 45 W PEP, $I_{DQ}$ = 350 mA, f1 = 945.0 MHz, f2 = 945.1 MHz) | IRL | 9 | 15 | — | dB |
| Two–Tone Common–Source Amplifier Power Gain ($V_{DD}$ = 28 Vdc, $P_{out}$ = 45 W PEP, $I_{DQ}$ = 350 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz) | $G_{ps}$ | — | 18.5 | — | dB |
| Two–Tone Drain Efficiency ($V_{DD}$ = 28 Vdc, $P_{out}$ = 45 W PEP, $I_{DQ}$ = 350 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz) | η | — | 41 | — | % |
| 3rd Order Intermodulation Distortion ($V_{DD}$ = 28 Vdc, $P_{out}$ = 45 W PEP, $I_{DQ}$ = 350 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz) | IMD | — | –31 | — | dBc |
| Input Return Loss ($V_{DD}$ = 28 Vdc, $P_{out}$ = 45 W PEP, $I_{DQ}$ = 350 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz) | IRL | — | 13 | — | dB |




| | | | |
|---|---|---|---|
| B1, B2 | Short Ferrite Beads, Surface Mount | Z3 | 0.14″ x 0.32″ |
| C1, C7, C13, C14 | 47 pF, Chip Capacitors, B Case | Z4 | 0.47″ x 0.32″ |
| C2, C8 | 2.7 pF, Chip Capacitors, B Case | Z5 | 0.16″ x 0.32″ x 0.62″ Tapered |
| C3 | 3.9 pF, Chip Capacitor, B Case | Z6 | 0.18″ x 0.62″ |
| C4, C5, C8, C9 | 10 pF, Chip Capacitors, B Case | Z7 | 0.56″ x 0.62″ |
| C6 | 10 μF, 35 V Tantalum Surface Mount Capacitor | Z8 | 0.33″ x 0.32″ |
| C10 | 2.2 pF, Chip Capacitor, B Case | Z9 | 0.14″ x 0.32″ |
| C11 | 4.7 pF, Chip Capacitor, B Case | Z10 | 0.36″ x 0.08″ |
| C12 | 1.2 pF, Chip Capacitor, B Case | Z11 | 1.01″ x 0.08″ |
| C17 | 220 μF, 50 V Electrolytic Capacitor | Z12 | 0.15″ x 0.08″ |
| L1, L2 | 12.5 nH, Inductors | Z13 | 0.29″ x 0.08″ |
| Z1 | 0.20″ x 0.08″ | | |
| Z2 | 0.57″ x 0.12″ | | |

**Figure 1. 945 MHz Broadband Test Circuit Schematic**

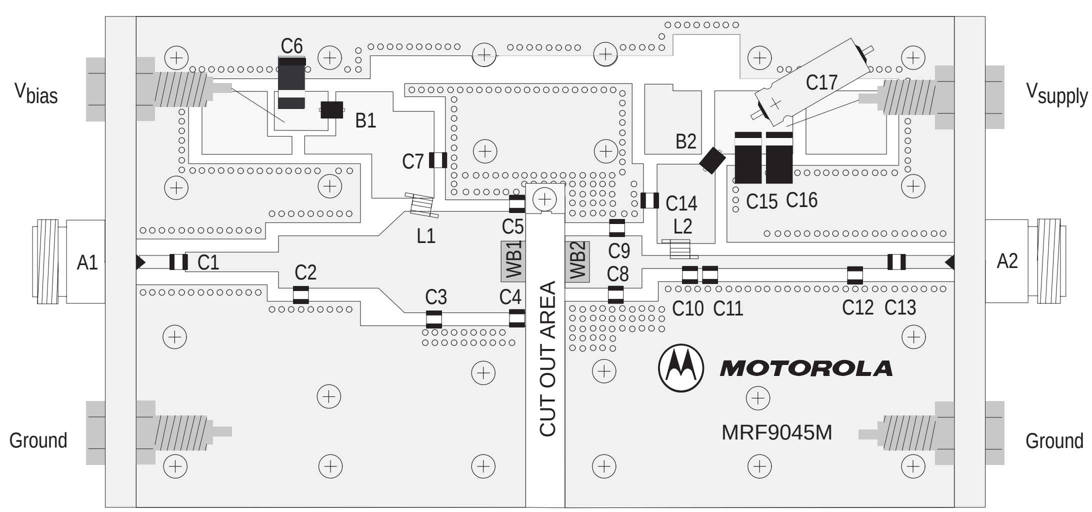



**Figure 2. 945 MHz Broadband Test Circuit Components Layout**

## TYPICAL CHARACTERISTICS

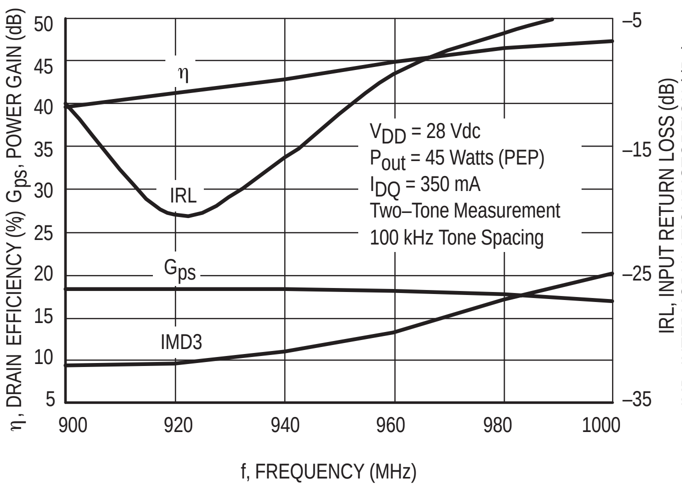



Figure 3. Class AB Test Circuit Performance

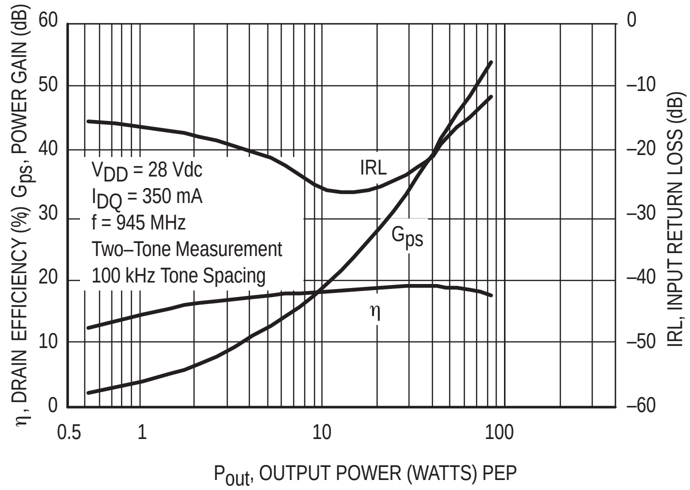



Figure 4. Power Gain, Efficiency and IRL versus Output Power

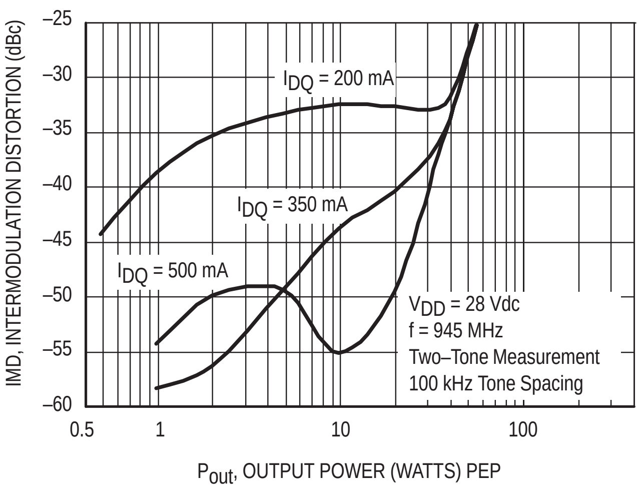



Figure 5. Intermodulation Distortion versus Output Power

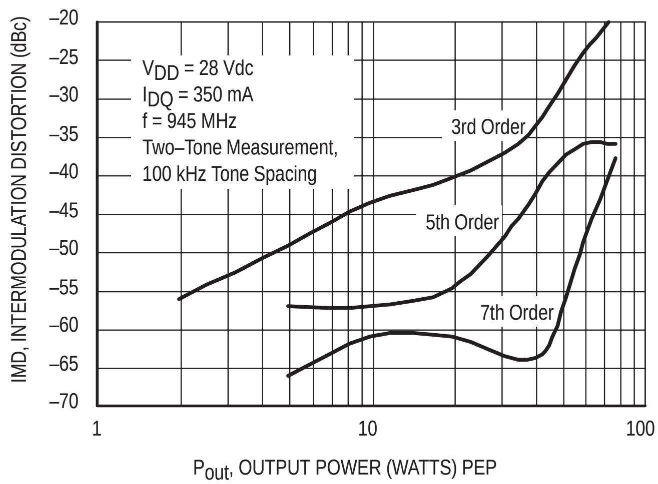



Figure 6. Intermodulation Distortion Products versus Output Power

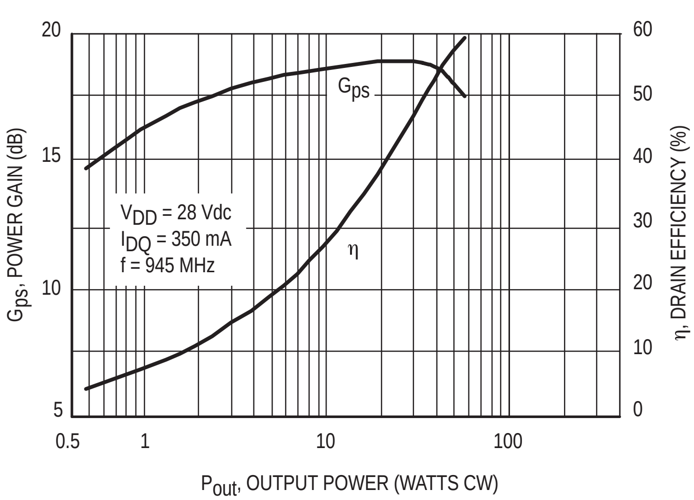



Figure 7. CW Power Gain and Drain Efficiency versus Output Power

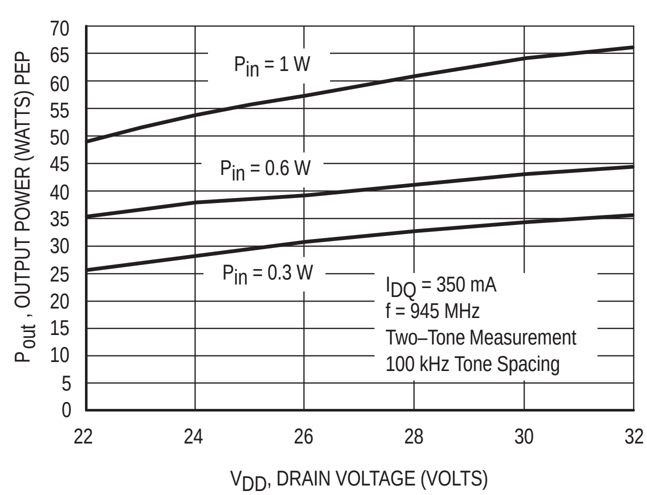
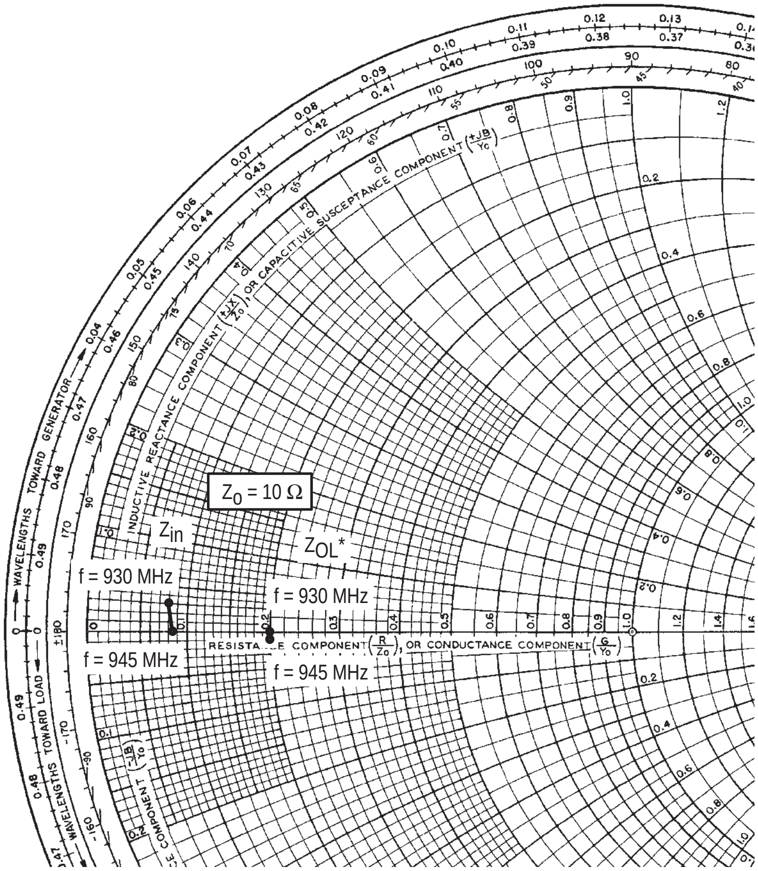



Figure 8. Output Voltage versus Supply Voltage




$V_{DD}$ = 28 V, $I_{DQ}$ = 350 mA, $P_{out}$ = 45 W (PEP)

| f MHz | $Z_{in}$ Ω | $Z_{OL}$* Ω |
|---|---|---|
| 930 | 0.81 + j0.25 | 2.03 – j0.09 |
| 945 | 0.85 + j0.05 | 2.03 – j0.28 |

$Z_{in}$ = Complex conjugate of source impedance.

$Z_{OL}$* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: $Z_{OL}$* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

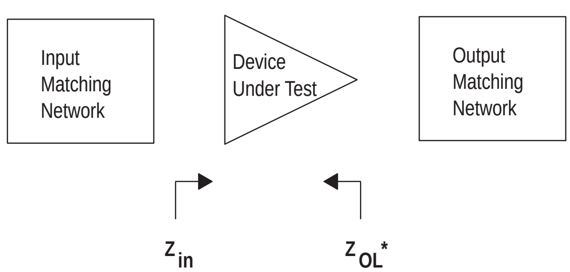
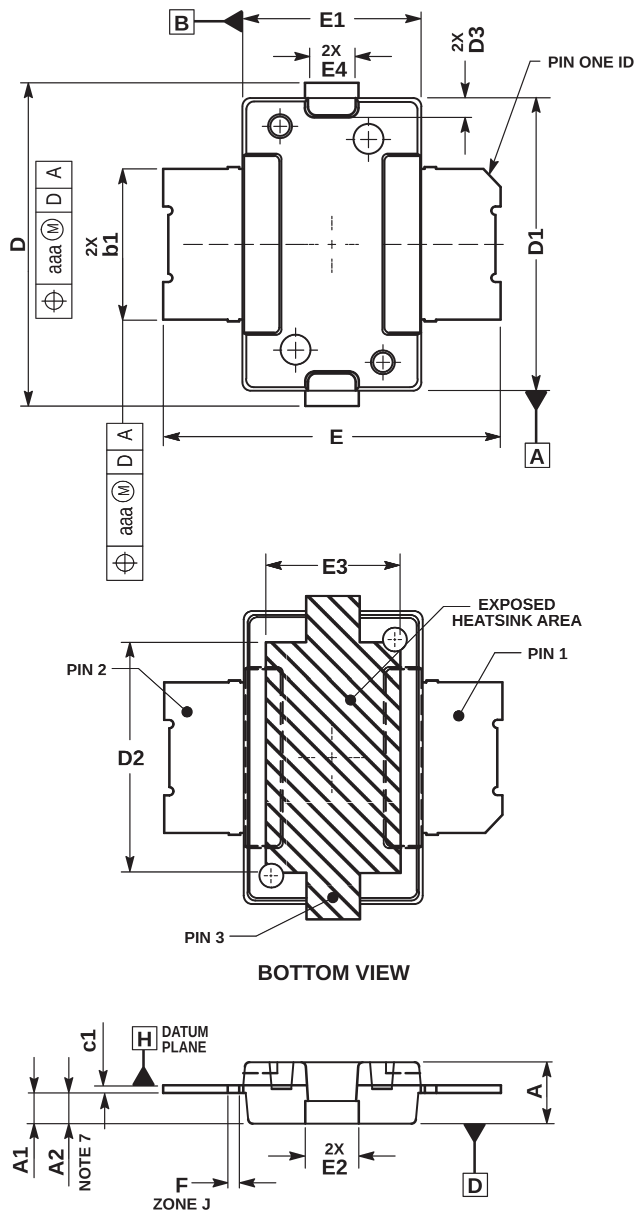



**Figure 9. Series Equivalent Input and Output Impedance**

## PACKAGE DIMENSIONS




NOTES:
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUM PLANE –H– IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS “D1” AND “E1” DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS “D1” AND “E1” DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
5. DIMENSION b1 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE b1 DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION A2 APPLIES WITHIN ZONE “J” ONLY.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | .076 | .084 | 1.93 | 2.13 |
| A1 | .038 | .044 | 0.96 | 1.12 |
| A2 | .040 | .042 | 1.02 | 1.07 |
| D | .416 | .424 | 10.57 | 10.77 |
| D1 | .376 | .384 | 9.55 | 9.75 |
| D2 | .290 | .320 | 7.37 | 8.13 |
| D3 | .016 | .024 | 0.41 | 0.61 |
| E | .436 | .444 | 11.07 | 11.28 |
| E1 | .236 | .244 | 5.99 | 6.20 |
| E2 | .066 | .074 | 1.68 | 1.88 |
| E3 | .150 | .180 | 3.81 | 4.57 |
| E4 | .058 | .066 | 1.47 | 1.68 |
| F | .025 BSC | | 0.64 BSC | |
| b1 | .193 | .199 | 4.90 | 5.06 |
| c1 | .007 | .011 | 0.18 | 0.28 |
| aaa | .004 | | 0.10 | |

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

**CASE 1265–06**
**ISSUE E**
**(TO–270)**

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