

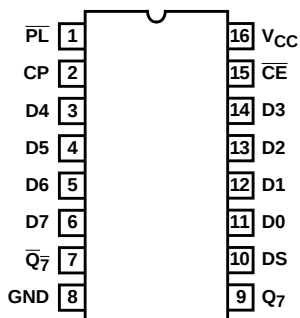
## High-Speed CMOS Logic 8-Bit Parallel-In/Serial-Out Shift Register

### Features

- Buffered Inputs
- Asynchronous Parallel Load
- Complementary Outputs
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Pinout

CD54HC165, CD54HCT165  
(CERDIP)  
CD74HC165, CD74HCT165  
(PDIP, SOIC)  
TOP VIEW



### Description

The 'HC165 and 'HCT165 are 8-bit parallel or serial-in shift registers with complementary serial outputs ( $Q_7$  and  $\overline{Q_7}$ ) available from the last stage. When the parallel load ( $\overline{PL}$ ) input is LOW, parallel data from the D0 to D7 inputs are loaded into the register asynchronously. When the  $\overline{PL}$  is HIGH, data enters the register serially at the DS input and shifts one place to the right ( $Q_0 \rightarrow Q_1 \rightarrow Q_2$ , etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by typing the  $Q_7$  output to the DS input of the succeeding device.

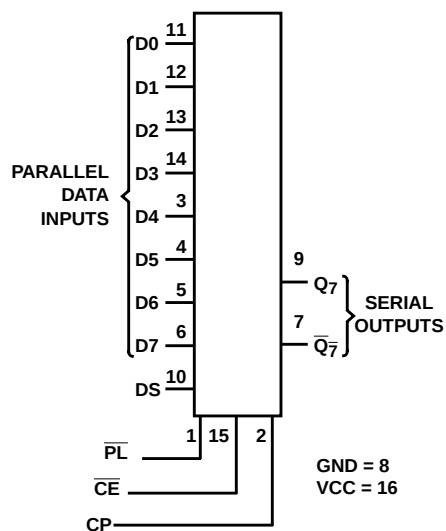
For predictable operation the LOW-to-HIGH transition of  $\overline{CE}$  should only take place while CP is HIGH. Also, CP and  $\overline{CE}$  should be LOW before the LOW-to-HIGH transition of PL to prevent shifting the data when  $\overline{PL}$  goes HIGH.

### Ordering Information

| PART NUMBER   | TEMP. RANGE (°C) | PACKAGE      |
|---------------|------------------|--------------|
| CD54HC165F3A  | -55 to 125       | 16 Ld CERDIP |
| CD54HCT165F3A | -55 to 125       | 16 Ld CERDIP |
| CD74HC165E    | -55 to 125       | 16 Ld PDIP   |
| CD74HC165M    | -55 to 125       | 16 Ld SOIC   |
| CD74HC165MT   | -55 to 125       | 16 Ld SOIC   |
| CD54HC165M96  | -55 to 125       | 16 Ld SOIC   |
| CD74HCT165E   | -55 to 125       | 16 Ld PDIP   |
| CD74HCT165M   | -55 to 125       | 16 Ld SOIC   |
| CD74HCT165MT  | -55 to 125       | 16 Ld SOIC   |
| CD54HCT165M96 | -55 to 125       | 16 Ld SOIC   |

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

## Functional Diagram



TRUTH TABLE

| OPERATING MODE  | INPUTS |    |    |    |         | Q <sub>n</sub> REGISTER |                                 | OUTPUTS        |                             |
|-----------------|--------|----|----|----|---------|-------------------------|---------------------------------|----------------|-----------------------------|
|                 | PL     | CE | CP | DS | D0 - D7 | Q <sub>0</sub>          | Q <sub>1</sub> - Q <sub>6</sub> | Q <sub>7</sub> | Q <sub>7</sub> <sup>̄</sup> |
| Parallel Load   | L      | X  | X  | X  | L       | L                       | L-L                             | L              | H                           |
|                 | L      | X  | X  | X  | H       | H                       | H-H                             | H              | L                           |
| Serial Shift    | H      | L  | ↑  | l  | X       | L                       | q <sub>0</sub> - q <sub>5</sub> | q <sub>6</sub> | q <sub>6</sub> <sup>̄</sup> |
|                 | H      | L  | ↑  | h  | X       | H                       | q <sub>0</sub> - q <sub>5</sub> | q <sub>6</sub> | q <sub>6</sub> <sup>̄</sup> |
| Hold Do Nothing | H      | H  | X  | X  | X       | q <sub>0</sub>          | q <sub>1</sub> - q <sub>6</sub> | q <sub>7</sub> | q <sub>7</sub> <sup>̄</sup> |

H = High Voltage Level

h = High Voltage Level One Set-up Time Prior To The Low-to-high Clock Transition

l = Low Voltage Level One Set-up Time Prior To The Low-to-high Clock Transition

L = Low Voltage Level

X = Don't Care

↑ = Transition from Low to High Level

q<sub>n</sub> = Lower Case Letters Indicate The State Of the Reference Output Clock Transition

# CD54HC165, CD74HC165, CD54HCT165, CD74HCT165

## Absolute Maximum Ratings

DC Supply Voltage,  $V_{CC}$  ..... -0.5V to 7V  
 DC Input Diode Current,  $I_{IK}$   
 For  $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$  .....  $\pm 20mA$   
 DC Output Diode Current,  $I_{OK}$   
 For  $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$  .....  $\pm 20mA$   
 DC Drain Current per Output,  $I_O$   
 For  $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$  .....  $\pm 25mA$   
 DC Output Source or Sink Current per Output Pin,  $I_O$   
 For  $V_O > -0.5V$  or  $V_O < V_{CC} + 0.5V$  .....  $\pm 25mA$   
 DC  $V_{CC}$  or Ground Current,  $I_{CC}$  or  $I_{GND}$  .....  $\pm 50mA$

## Thermal Information

Thermal Resistance (Typical, Note 1)  $\theta_{JA}$  ( $^{\circ}C/W$ )  
 E (PDIP) Package ..... 67  
 M (SOIC) Package ..... 73  
 Maximum Junction Temperature .....  $150^{\circ}C$   
 Maximum Storage Temperature Range .....  $-65^{\circ}C$  to  $150^{\circ}C$   
 Maximum Lead Temperature (Soldering 10s) .....  $300^{\circ}C$   
 (SOIC - Lead Tips Only)

## Operating Conditions

Temperature Range ( $T_A$ ) .....  $-55^{\circ}C$  to  $125^{\circ}C$   
 Supply Voltage Range,  $V_{CC}$   
 HC Types ..... 2V to 6V  
 HCT Types ..... 4.5V to 5.5V  
 DC Input or Output Voltage,  $V_I$ ,  $V_O$  ..... 0V to  $V_{CC}$   
 Input Rise and Fall Time  
 2V ..... 1000ns (Max)  
 4.5V ..... 500ns (Max)  
 6V ..... 400ns (Max)

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

| PARAMETER                               | SYMBOL          | TEST CONDITIONS                       |                     | V <sub>CC</sub> (V) | 25°C |     |      | -40°C TO 85°C |      | -55°C TO 125°C |      | UNITS |
|-----------------------------------------|-----------------|---------------------------------------|---------------------|---------------------|------|-----|------|---------------|------|----------------|------|-------|
|                                         |                 | V <sub>I</sub> (V)                    | I <sub>O</sub> (mA) |                     | MIN  | TYP | MAX  | MIN           | MAX  | MIN            | MAX  |       |
| HC TYPES                                |                 |                                       |                     |                     |      |     |      |               |      |                |      |       |
| High Level Input Voltage                | V <sub>IH</sub> | -                                     | -                   | 2                   | 1.5  | -   | -    | 1.5           | -    | 1.5            | -    | V     |
|                                         |                 |                                       |                     | 4.5                 | 3.15 | -   | -    | 3.15          | -    | 3.15           | -    | V     |
|                                         |                 |                                       |                     | 6                   | 4.2  | -   | -    | 4.2           | -    | 4.2            | -    | V     |
| Low Level Input Voltage                 | V <sub>IL</sub> | -                                     | -                   | 2                   | -    | -   | 0.5  | -             | 0.5  | -              | 0.5  | V     |
|                                         |                 |                                       |                     | 4.5                 | -    | -   | 1.35 | -             | 1.35 | -              | 1.35 | V     |
|                                         |                 |                                       |                     | 6                   | -    | -   | 1.8  | -             | 1.8  | -              | 1.8  | V     |
| High Level Output Voltage<br>CMOS Loads | V <sub>OH</sub> | V <sub>IH</sub> or<br>V <sub>IL</sub> | -0.02               | 2                   | 1.9  | -   | -    | 1.9           | -    | 1.9            | -    | V     |
|                                         |                 |                                       | -0.02               | 4.5                 | 4.4  | -   | -    | 4.4           | -    | 4.4            | -    | V     |
|                                         |                 |                                       | -0.02               | 6                   | 5.9  | -   | -    | 5.9           | -    | 5.9            | -    | V     |
| High Level Output Voltage<br>TTL Loads  | V <sub>OH</sub> | V <sub>IH</sub> or<br>V <sub>IL</sub> | -4                  | 4.5                 | 3.98 | -   | -    | 3.84          | -    | 3.7            | -    | V     |
| -5.2                                    |                 |                                       | 6                   | 5.48                | -    | -   | 5.34 | -             | 5.2  | -              | V    |       |
| Low Level Output Voltage<br>CMOS Loads  | V <sub>OL</sub> | V <sub>IH</sub> or<br>V <sub>IL</sub> | 0.02                | 2                   | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                       | 0.02                | 4.5                 | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                       | 0.02                | 6                   | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
| Low Level Output Voltage<br>TTL Loads   | V <sub>OL</sub> | V <sub>IH</sub> or<br>V <sub>IL</sub> | 4                   | 4.5                 | -    | -   | 0.26 | -             | 0.33 | -              | 0.4  | V     |
|                                         |                 |                                       | 5.2                 | 6                   | -    | -   | 0.26 | -             | 0.33 | -              | 0.4  | V     |
| Input Leakage Current                   | I <sub>I</sub>  | V <sub>CC</sub> or<br>GND             | -                   | 6                   | -    | -   | ±0.1 | -             | ±1   | -              | ±1   | μA    |

# **CD54HC165, CD74HC165, CD54HCT165, CD74HCT165**

## **DC Electrical Specifications**    (Continued)

| PARAMETER                                                      | SYMBOL                   | TEST CONDITIONS      |            | $V_{CC}$ (V) | 25°C |     |           | -40°C TO 85°C |         | -55°C TO 125°C |         | UNITS   |
|----------------------------------------------------------------|--------------------------|----------------------|------------|--------------|------|-----|-----------|---------------|---------|----------------|---------|---------|
|                                                                |                          | $V_I$ (V)            | $I_O$ (mA) |              | MIN  | TYP | MAX       | MIN           | MAX     | MIN            | MAX     |         |
| Quiescent Device Current                                       | $I_{CC}$                 | $V_{CC}$ or GND      | 0          | 6            | -    | -   | 8         | -             | 80      | -              | 160     | $\mu A$ |
| <b>HCT TYPES</b>                                               |                          |                      |            |              |      |     |           |               |         |                |         |         |
| High Level Input Voltage                                       | $V_{IH}$                 | -                    | -          | 4.5 to 5.5   | 2    | -   | -         | 2             | -       | 2              | -       | V       |
| Low Level Input Voltage                                        | $V_{IL}$                 | -                    | -          | 4.5 to 5.5   | -    | -   | 0.8       | -             | 0.8     | -              | 0.8     | V       |
| High Level Output Voltage<br>CMOS Loads                        | $V_{OH}$                 | $V_{IH}$ or $V_{IL}$ | -0.02      | 4.5          | 4.4  | -   | -         | 4.4           | -       | 4.4            | -       | V       |
| High Level Output Voltage<br>TTL Loads                         |                          |                      | -4         | 4.5          | 3.98 | -   | -         | 3.84          | -       | 3.7            | -       | V       |
| Low Level Output Voltage<br>CMOS Loads                         | $V_{OL}$                 | $V_{IH}$ or $V_{IL}$ | 0.02       | 4.5          | -    | -   | 0.1       | -             | 0.1     | -              | 0.1     | V       |
| Low Level Output Voltage<br>TTL Loads                          |                          |                      | 4          | 4.5          | -    | -   | 0.26      | -             | 0.33    | -              | 0.4     | V       |
| Input Leakage Current                                          | $I_I$                    | $V_{CC}$ to GND      | 0          | 5.5          | -    | -   | $\pm 0.1$ | -             | $\pm 1$ | -              | $\pm 1$ | $\mu A$ |
| Quiescent Device Current                                       | $I_{CC}$                 | $V_{CC}$ or GND      | 0          | 5.5          | -    | -   | 8         | -             | 80      | -              | 160     | $\mu A$ |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | $\Delta I_{CC}$ (Note 2) | $V_{CC}$ -2.1        | -          | 4.5 to 5.5   | -    | 100 | 360       | -             | 450     | -              | 490     | $\mu A$ |

NOTE:

- For dual-supply systems theoretical worst case ( $V_I = 2.4V$ ,  $V_{CC} = 5.5V$ ) specification is 1.8mA.

## **HCT Input Loading Table**

| INPUT               | UNIT LOADS |
|---------------------|------------|
| DS, D0 to D7        | 0.35       |
| CP, $\overline{PL}$ | 0.65       |

NOTE: Unit Load is  $\Delta I_{CC}$  limit specified in DC Electrical Specifications table, e.g. 360 $\mu A$  max at 25°C.

## **Prerequisite For Switching Specifications**

| PARAMETER      | SYMBOL                            | V <sub>CC</sub> (V) | 25°C |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|----------------|-----------------------------------|---------------------|------|-----|---------------|-----|----------------|-----|-------|
|                |                                   |                     | MIN  | MAX | MIN           | MAX | MIN            | MAX |       |
| HC TYPES       |                                   |                     |      |     |               |     |                |     |       |
| CP Pulse Width | t <sub>WL</sub> , t <sub>WH</sub> | 2                   | 80   | -   | 100           | -   | 120            | -   | ns    |
|                |                                   | 4.5                 | 16   | -   | 20            | -   | 24             | -   | ns    |
|                |                                   | 6                   | 14   | -   | 17            | -   | 20             | -   | ns    |

**CD54HC165, CD74HC165, CD54HCT165, CD74HCT165**

**Prerequisite For Switching Specifications (Continued)**

| PARAMETER                                       | SYMBOL             | V <sub>CC</sub> (V) | 25°C |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|-------------------------------------------------|--------------------|---------------------|------|-----|---------------|-----|----------------|-----|-------|
|                                                 |                    |                     | MIN  | MAX | MIN           | MAX | MIN            | MAX |       |
| $\overline{\text{PL}}$ Pulse Width              | $t_{\text{WL}}$    | 2                   | 80   | -   | 100           | -   | 120            | -   | ns    |
|                                                 |                    | 4.5                 | 16   | -   | 20            | -   | 24             | -   | ns    |
|                                                 |                    | 6                   | 14   | -   | 17            | -   | 20             | -   | ns    |
| Set-up Time<br>DS to CP                         | $t_{\text{SU}}$    | 2                   | 80   | -   | 100           | -   | 120            | -   | ns    |
|                                                 |                    | 4.5                 | 16   | -   | 20            | -   | 24             | -   | ns    |
|                                                 |                    | 6                   | 14   | -   | 17            | -   | 20             | -   | ns    |
| $\overline{\text{CE}}$ to CP                    | $t_{\text{SU(L)}}$ | 2                   | 80   | -   | 100           | -   | 120            | -   | ns    |
|                                                 |                    | 4.5                 | 16   | -   | 20            | -   | 24             | -   | ns    |
|                                                 |                    | 6                   | 14   | -   | 17            | -   | 20             | -   | ns    |
| D0-D7 to $\overline{\text{PL}}$                 | $t_{\text{SU}}$    | 2                   | 80   | -   | 100           | -   | 120            | -   | ns    |
|                                                 |                    | 4.5                 | 16   | -   | 20            | -   | 24             | -   | ns    |
|                                                 |                    | 6                   | 14   | -   | 17            | -   | 20             | -   | ns    |
| Hold Time<br>DS to CP or $\overline{\text{CE}}$ | $t_{\text{H}}$     | 2                   | 35   | -   | 45            | -   | 55             | -   | ns    |
|                                                 |                    | 4.5                 | 7    | -   | 9             | -   | 11             | -   | ns    |
|                                                 |                    | 6                   | 6    | -   | 8             | -   | 9              | -   | ns    |
| $\overline{\text{CE}}$ to CP                    | $t_{\text{H}}$     | 2                   | 0    | -   | 0             | -   | 0              | -   | ns    |
|                                                 |                    | 4.5                 | 0    | -   | 0             | -   | 0              | -   | ns    |
|                                                 |                    | 6                   | 0    | -   | 0             | -   | 0              | -   | ns    |
| Recovery Time<br>$\overline{\text{PL}}$ to CP   | $t_{\text{REC}}$   | 2                   | 100  | -   | 125           | -   | 150            | -   | ns    |
|                                                 |                    | 4.5                 | 20   | -   | 25            | -   | 30             | -   | ns    |
|                                                 |                    | 6                   | 17   | -   | 21            | -   | 26             | -   | ns    |
| Maximum Clock Pulse<br>Frequency                | $f_{\text{MAX}}$   | 2                   | 6    | -   | 5             | -   | 4              | -   | MHz   |
|                                                 |                    | 4.5                 | 30   | -   | 24            | -   | 20             | -   | MHz   |
|                                                 |                    | 6                   | 35   | -   | 28            | -   | 24             | -   | MHz   |

**HCT TYPES**

|                                                 |                                |     |    |   |    |   |    |   |     |
|-------------------------------------------------|--------------------------------|-----|----|---|----|---|----|---|-----|
| CP Pulse Width                                  | $t_{\text{WL}}, t_{\text{WH}}$ | 4.5 | 18 | - | 23 | - | 27 | - | ns  |
| $\overline{\text{PL}}$ Pulse Width              | $t_{\text{WL}}$                | 4.5 | 20 | - | 25 | - | 30 | - | ns  |
| Set-up Time<br>DS to CP                         | $t_{\text{SU}}$                | 4.5 | 20 | - | 25 | - | 30 | - | ns  |
| $\overline{\text{CE}}$ to CP                    | $t_{\text{SU(L)}}$             | 4.5 | 20 | - | 25 | - | 30 | - | ns  |
| D0-D7 to $\overline{\text{PL}}$                 | $t_{\text{SU}}$                | 6   | 20 | - | 25 | - | 30 | - | ns  |
| Hold Time<br>DS to CP or $\overline{\text{CE}}$ | $t_{\text{H}}$                 | 4.5 | 7  | - | 9  | - | 11 | - | ns  |
| $\overline{\text{CE}}$ to CP                    | $t_{\text{S}}, t_{\text{H}}$   | 4.5 | 0  | - | 0  | - | 0  | - | ns  |
| Recovery Time<br>$\overline{\text{PL}}$ to CP   | $t_{\text{REC}}$               | 4.5 | 20 | - | 25 | - | 30 | - | ns  |
| Maximum Clock Pulse<br>Frequency                | $f_{\text{MAX}}$               | 4.5 | 27 | - | 22 | - | 18 | - | MHz |

**CD54HC165, CD74HC165, CD54HCT165, CD74HCT165**

**Switching Specifications** Input  $t_r, t_f = 6\text{ns}$

| PARAMETER                                                   | SYMBOL                              | TEST CONDITIONS       | V <sub>CC</sub> (V) | 25°C |     | -40°C TO 85°C | -55°C TO 125°C | UNITS |
|-------------------------------------------------------------|-------------------------------------|-----------------------|---------------------|------|-----|---------------|----------------|-------|
|                                                             |                                     |                       |                     | TYP  | MAX | MAX           | MAX            |       |
| HC TYPES                                                    |                                     |                       |                     |      |     |               |                |       |
| Propagation Delay                                           | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | 165 | 205           | 250            | ns    |
| CP or $\overline{CE}$ to Q <sub>7</sub> or $\overline{Q_7}$ |                                     |                       | 4.5                 | -    | 33  | 41            | 50             | ns    |
|                                                             |                                     | C <sub>L</sub> = 15pF | 5                   | 13   | -   | -             | -              | ns    |
|                                                             |                                     | C <sub>L</sub> = 50pF | 6                   | -    | 28  | 35            | 43             | ns    |
| $\overline{PL}$ to Q <sub>7</sub> or $\overline{Q_7}$       | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | 175 | 220           | 265            | ns    |
|                                                             |                                     |                       | 4.5                 | -    | 35  | 44            | 53             | ns    |
|                                                             |                                     | C <sub>L</sub> = 15pF | 5                   | 14   | -   | -             | -              | ns    |
|                                                             |                                     | C <sub>L</sub> = 50pF | 6                   | -    | 30  | 37            | 45             | ns    |
| D7 to Q <sub>7</sub> or $\overline{Q_7}$                    | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | 150 | 190           | 225            | ns    |
|                                                             |                                     |                       | 4.5                 | -    | 30  | 38            | 45             | ns    |
|                                                             |                                     | C <sub>L</sub> = 15pF | 5                   | 12   | -   | -             | -              | ns    |
|                                                             |                                     | C <sub>L</sub> = 50pF | 6                   | -    | 26  | 33            | 38             | ns    |
| Output Transition Times                                     | t <sub>TLH</sub> , t <sub>THL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | 75  | 95            | 110            | ns    |
|                                                             |                                     |                       | 4.5                 | -    | 15  | 19            | 22             | ns    |
|                                                             |                                     |                       | 6                   | -    | 13  | 16            | 19             | ns    |
| Input Capacitance                                           | C <sub>IN</sub>                     | -                     | -                   | -    | 10  | 10            | 10             | pF    |
| Power Dissipation Capacitance<br>(Notes 3, 4)               | C <sub>PD</sub>                     | -                     | 5                   | 17   | -   | -             | -              | pF    |
| HCT TYPES                                                   |                                     |                       |                     |      |     |               |                |       |
| Propagation Delay                                           | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 4.5                 | -    | 40  | 50            | 60             | ns    |
| CP or $\overline{CE}$ to Q <sub>7</sub> or $\overline{Q_7}$ |                                     | C <sub>L</sub> = 15pF | 5                   | 17   | -   | -             | -              | ns    |
| $\overline{PL}$ to Q <sub>7</sub> or $\overline{Q_7}$       | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 4.5                 | -    | 40  | 50            | 60             | ns    |
|                                                             |                                     | C <sub>L</sub> = 15pF | 5                   | 17   | -   | -             | -              | ns    |
| D7 to Q <sub>7</sub> or $\overline{Q_7}$                    | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 4.5                 | -    | 35  | 44            | 53             | ns    |
|                                                             |                                     | C <sub>L</sub> = 15pF | 5                   | 14   | -   | -             | -              | ns    |
| Output Transition Times                                     | t <sub>TLH</sub> , t <sub>THL</sub> | C <sub>L</sub> = 50pF | 4.5                 | -    | 15  | 19            | 22             | ns    |
| Input Capacitance                                           | C <sub>IN</sub>                     | C <sub>L</sub> = 50pF | -                   | -    | 10  | 10            | 10             | pF    |
| Power Dissipation Capacitance<br>(Notes 3, 4)               | C <sub>PD</sub>                     | -                     | 5                   | 24   |     | -             | -              | pF    |

**NOTES:**

- $C_{PD}$  is used to determine the dynamic power consumption, per package.
- $P_D = V_{CC}^2 f_i + \sum (C_L V_{CC}^2 + f_O)$  where  $f_i$  = Input Frequency,  $f_O$  = Output Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

## Test Circuits and Waveforms

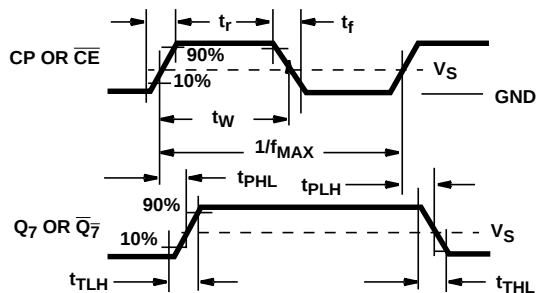


FIGURE 3. SERIAL-SHIFT MODE

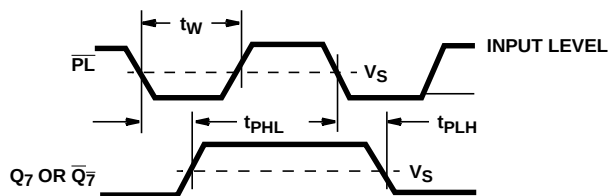


FIGURE 4. PARALLEL-LOAD MODE

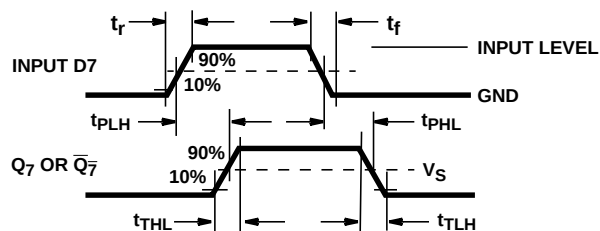


FIGURE 5. PARALLEL-LOAD MODE

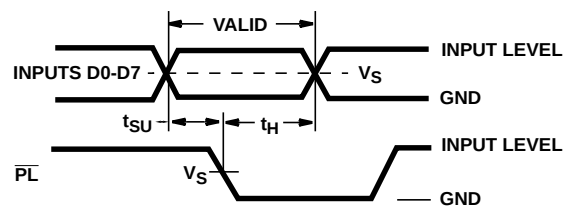


FIGURE 6. PARALLEL-LOAD MODE

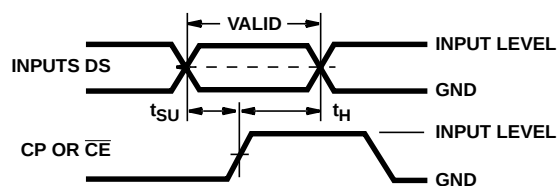


FIGURE 7. SERIAL-SHIFT MODE

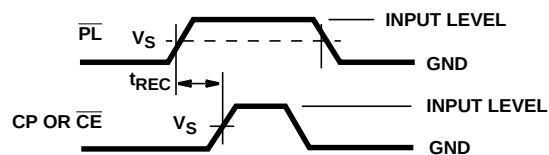


FIGURE 8. SERIAL-SHIFT MODE

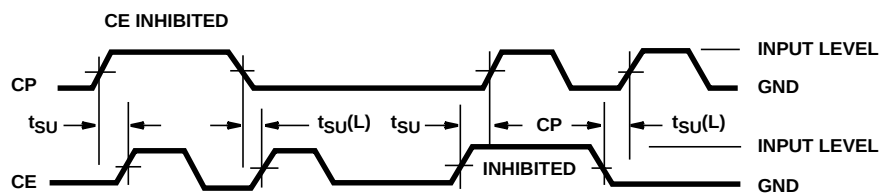


FIGURE 9. SERIAL-SHIFT, CLOCK-INHIBIT MODE

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 5962-8685501EA   | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | Call TI          | Level-NC-NC-NC               |
| CD54HC165F3A     | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | Call TI          | Level-NC-NC-NC               |
| CD54HCT165F3A    | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | Call TI          | Level-NC-NC-NC               |
| CD74HC165E       | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | Level-NC-NC-NC               |
| CD74HC165EE4     | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | Level-NC-NC-NC               |
| CD74HC165M       | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC165M96     | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC165M96E4   | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC165ME4     | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC165MT      | ACTIVE                | SOIC         | D               | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC165MTE4    | ACTIVE                | SOIC         | D               | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HCT165E      | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | Level-NC-NC-NC               |
| CD74HCT165EE4    | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | Level-NC-NC-NC               |
| CD74HCT165M      | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HCT165M96    | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HCT165M96E4  | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HCT165ME4    | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HCT165MT     | ACTIVE                | SOIC         | D               | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HCT165MTE4   | ACTIVE                | SOIC         | D               | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

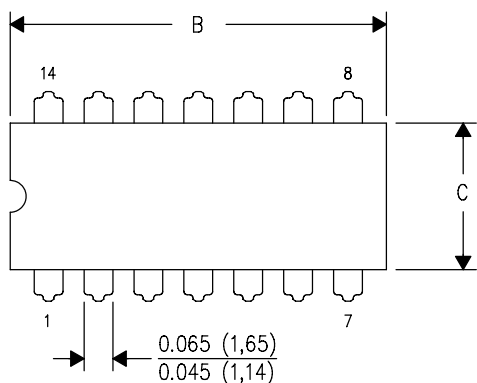
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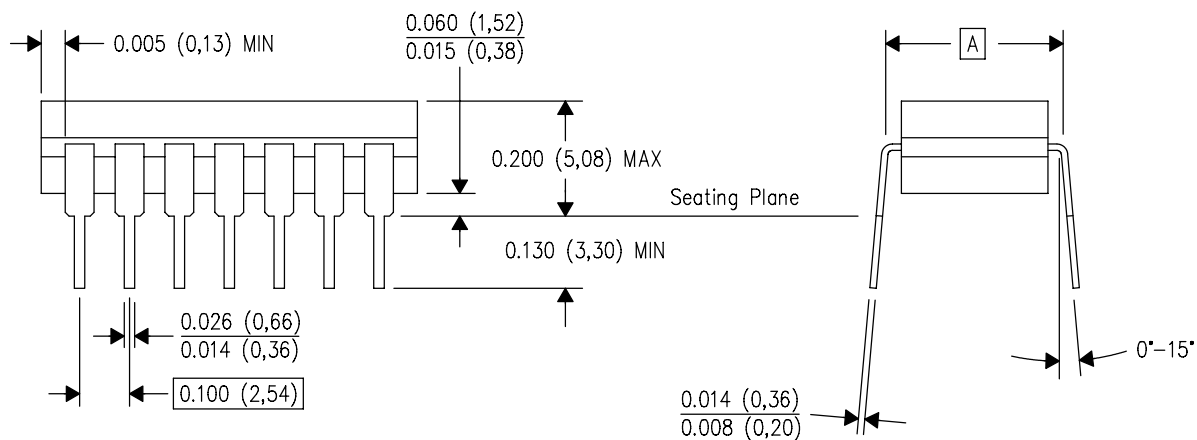
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



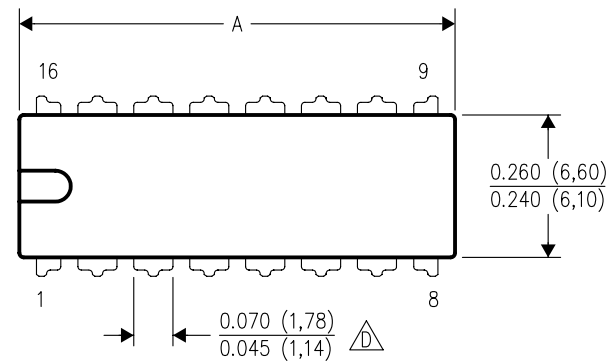
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

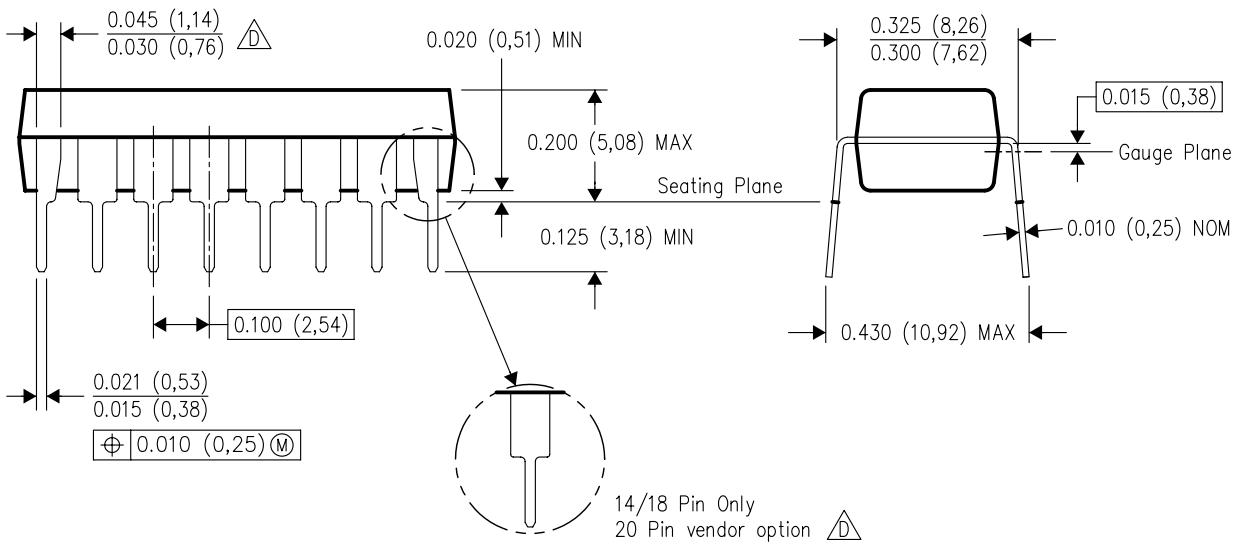
N (R-PDIP-T\*\*)

16 PINS SHOWN

# PLASTIC DUAL-IN-LINE PACKAGE



| DIM \ PINS **       | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



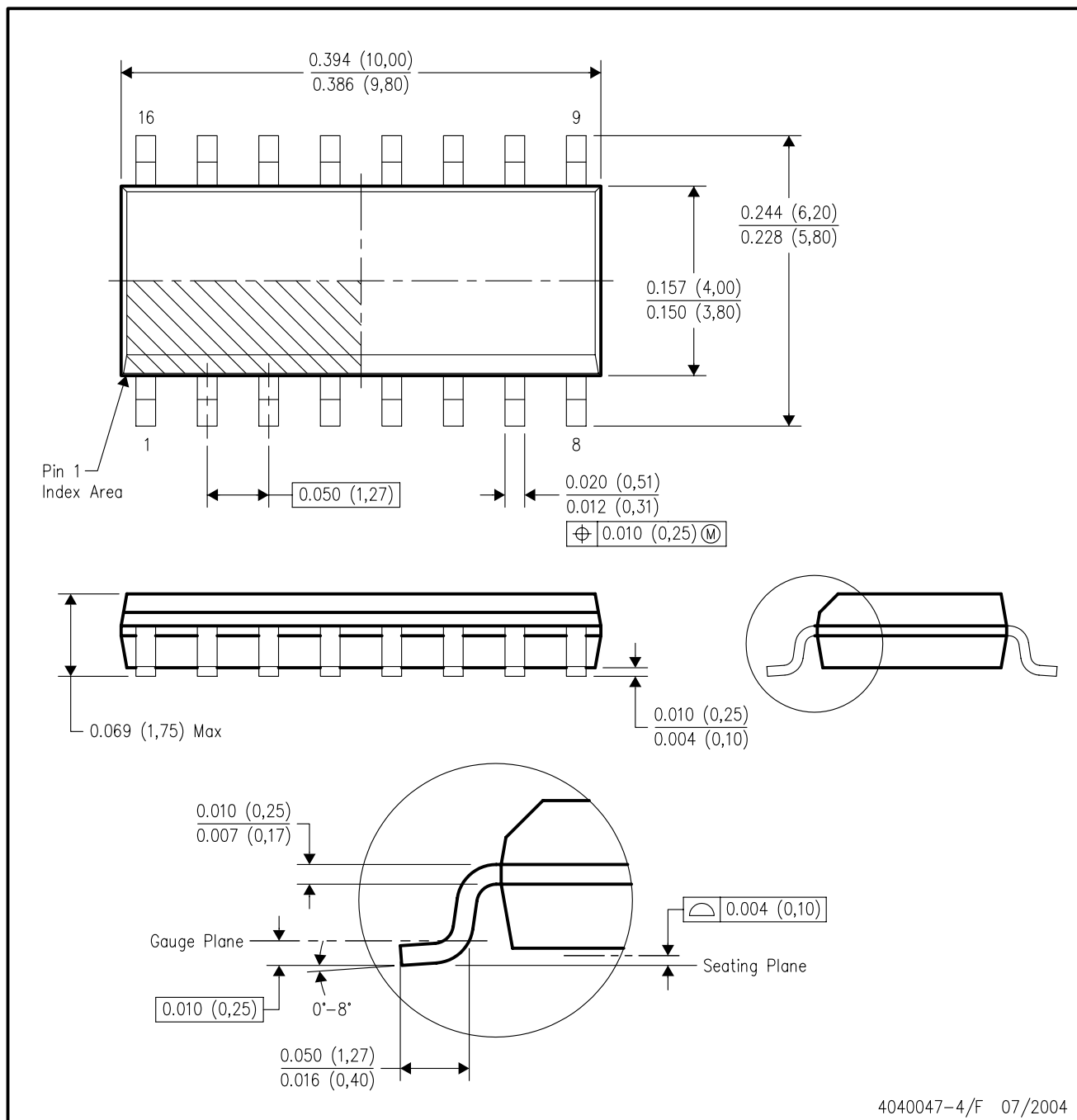
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

## D (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/F 07/2004

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-012 variation AC.

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