Canal+Compatible I²C Bus Controlled 4-input 3-output AV Switch
Monolithic IC MM1422, 1423, 1442, 1443

June 21, 1999

Outline

This IC is a Canal+ compatible I²C bus controlled AV switch with 4-input 3-output developed for VCRs and DVD players for Europe. There are four models available, which are either stereo or mono (audio) with or without a clamp circuit (video).

Features

1. I²C bus serial control
2. Includes two 75Ω driver outputs for video and two 600Ω driver outputs for audio.
3. Enables audio mute with an external pin
4. Operating power supply voltage 11 to 13V
5. Two types of video inputs; with or without a clamp
6. Two types of audio; mono or stereo

Packages

SSOP-34A (MM1443XJ)
SDIP-32A (MM1443XD)

Applications

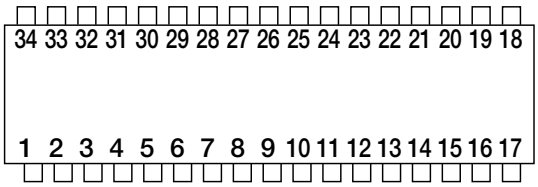
1. Canal+ compatible VCRs for Europe
2. DVD players

Series Table

	Video input clamp	Stereo	Monaural	Package	
				SDIP−32A	SSOP−34A
MM1422			○	○	○
MM1423		○		○	○
MM1442	○		○	○	○
MM1443	○	○		○	○

Pin Assignment

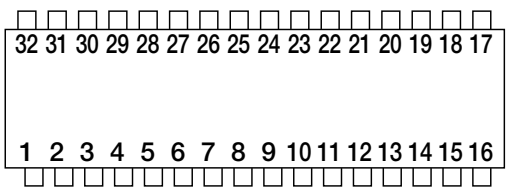
MM1443XJ



SSOP-34A

1	E1–V	10	E1–L	19	GND1	28	TUN–V
2	Vcc2	11	FS	20	TUN–R(N.C.)	29	VOUT3
3	E2–V	12	EXT–R(N.C.)	21	ROUT3(N.C.)	30	VOUT2
4	Vcc1	13	Port1	22	ROUT2(N.C.)	31	VOUT1
5	EXT–V	14	E2–R(N.C.)	23	ROUT1(N.C.)	32	SDA
6	EXT–L	15	Port2	24	TUN–L	33	SCL
7	BIAS	16	E1–R(N.C.)	25	LOUT3	34	GND2
8	E2–L	17	NC	26	LOUT2		
9	Mute	18	NC	27	LOUT1		

MM1443XD

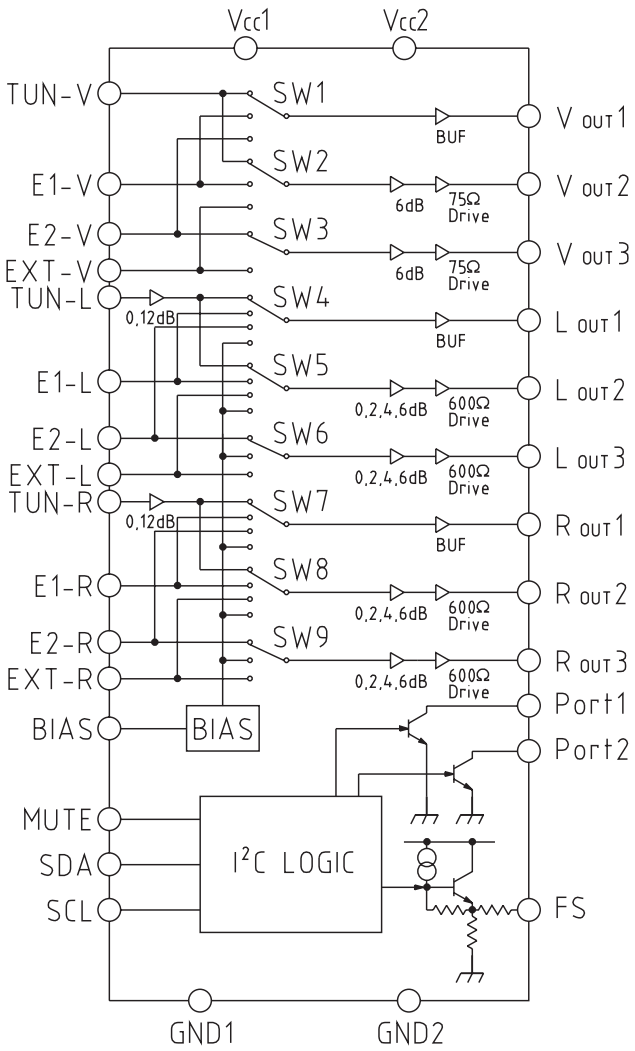


SDIP-32A

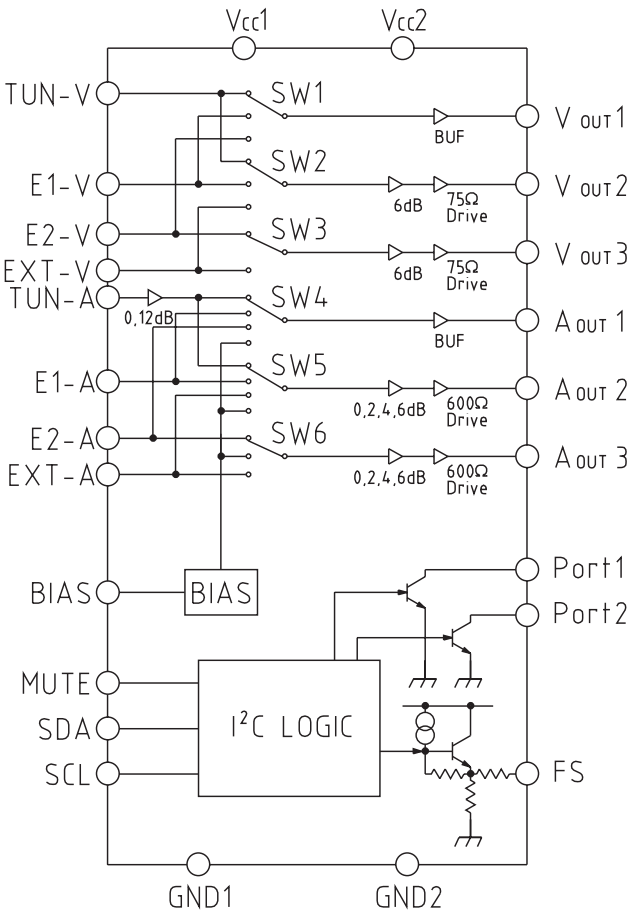
1	E1–V	9	Mute	17	GND1	25	LOUT1
2	Vcc2	10	E1–L	18	TUN–R(N.C.)	26	TUN–V
3	E2–V	11	FS	19	ROUT3(N.C.)	27	VOUT3
4	Vcc1	12	EXT–R(N.C.)	20	ROUT2(N.C.)	28	VOUT2
5	EXT–V	13	Port1	21	ROUT1(N.C.)	29	VOUT1
6	EXT–L	14	E2–R(N.C.)	22	TUN–L	30	SDA
7	BIAS	15	Port2	23	LOUT3	31	SCL
8	E2–L	16	E1–R(N.C.)	24	LOUT2	32	GND2

Block Diagram

Stereo type (MM1423, MM1443)



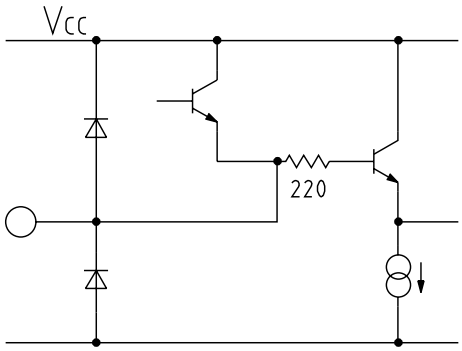
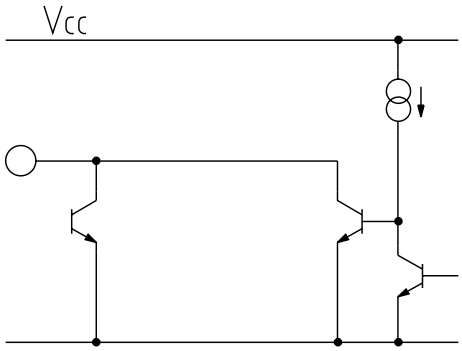
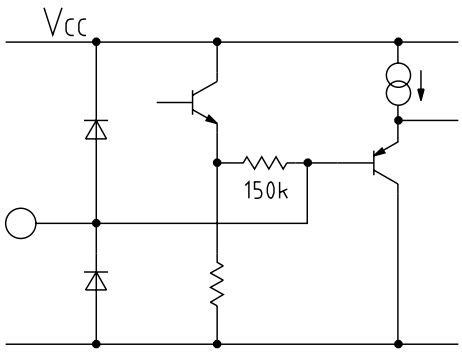
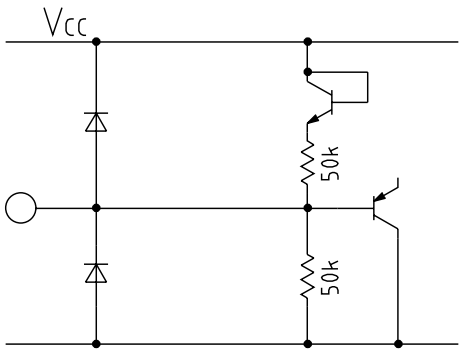
Monaural type (MM1422, MM1442)

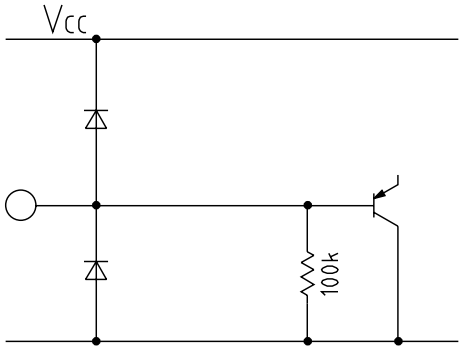
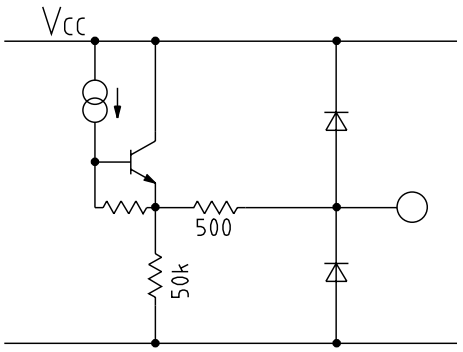
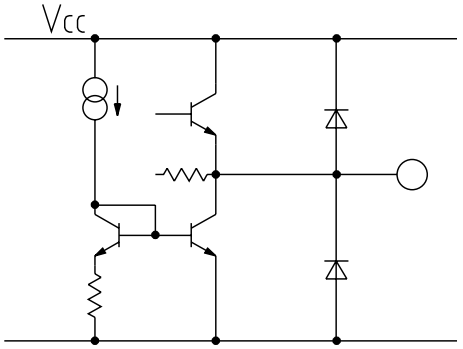
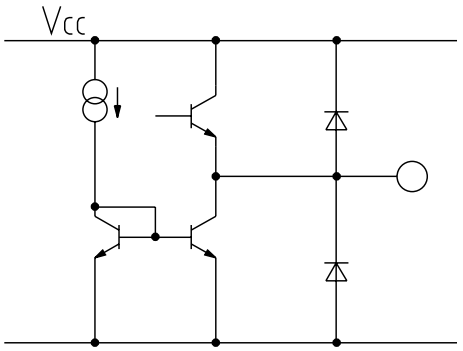


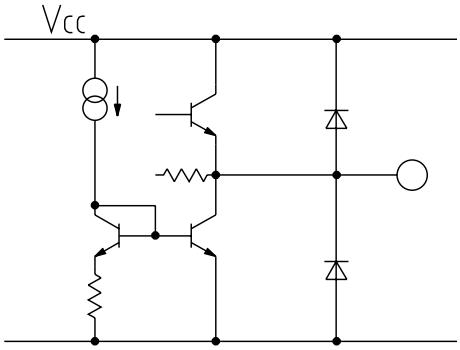
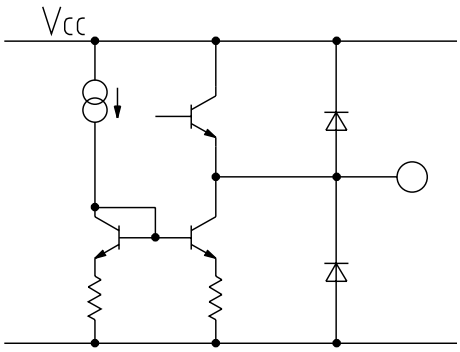
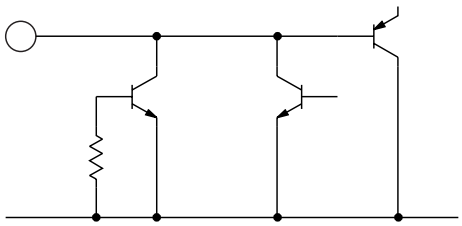
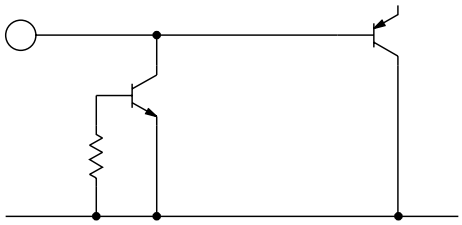
Introduction of Main Model

AV Switch for I²C BUS Control, 4-input, 3-output and Canal Plus Compatible
Monolithic IC MM1443

Pin Description

Pin No.	Pin name	Functions	Equivalent circuit diagram
1 3 5 28	E1–V E2–V EXT–V TUN–V	Video input pin	
2 4	Vcc2 Vcc1	Vcc2 is power supply voltage pin for 75Ω driver	
13 15	Port1 Port2	Port output pin	
6 8 10 12 14 16 20 24	EXT–L E2–L E1–L EXT–R E2–R E1–R TUN–R TUN–L	Audio input pin	
7	BIAS	Bias pin	

Pin No.	Pin name	Functions	Equivalent circuit diagram
9	Mute	Mute pin	
19 34	GND1 GND2	GND2 is a GND pin for 75Ω driver	
11	FS	FS output pin	
21 22 25 26	ROUT3 ROUT2 LOUT3 LOUT2	Audio driver output pin	
23 27	ROUT1 LOUT1	Audio buffer output pin	

Pin No.	Pin name	Functions	Equivalent circuit diagram
29 30	VOUT3 VOUT2	Video driver output pin	
31	VOUT1	Video buffer output pin	
32	SDA	SDA pin	
33	SCL	SCL pin	
17 18	NC		

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Unit
Storage temperature	T_{STG}	–40~+125	°C
Operating temperature	T_{OPR}	-25~+75	°C
Power supply voltage	V_{CC} max.	15	V
Allowable loss	Pd	700	mW

Recommend Operating Conditions

Item	Symbol	Ratings	Unit
Operating temperature	T_{OPR}	-25~+75	°C
Operating voltage	V_{OP}	11~13	V

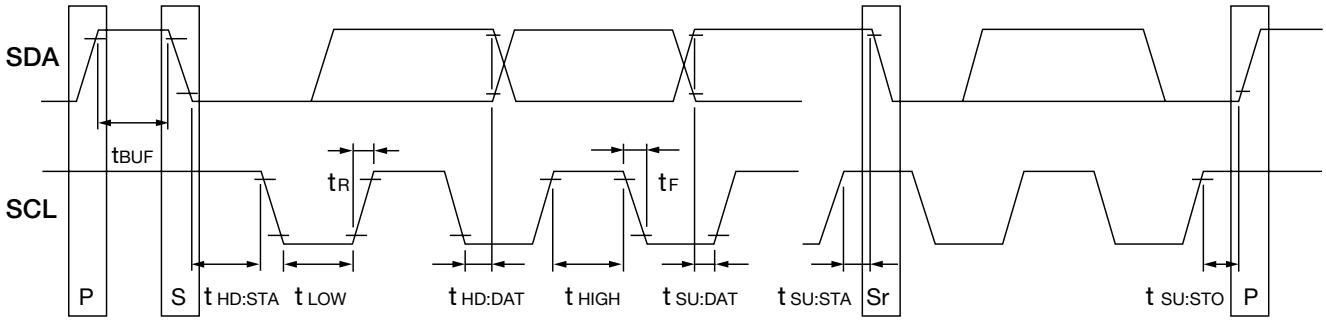
Electrical Characteristics (Except where noted otherwise, Ta=25°C, V_{CC}=12V)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Consumption current	I_{CC}	No-signal, no-load		33.5	40.0	mA
[FS pin output level]						
High voltage	V_{FSH}	FS pin control High selected	9.5	11.0	12.0	V
Middle voltage	V_{FSM}	FS pin control Mid selected	4.5	6.0	7.0	V
Low voltage	V_{FSL}	FS pin control Low selected		0.2	1.0	V
[Crosstalk]						
V_{OUT}1 V_{OUT}2 V_{OUT}3	CT_{V1} CT_{V2} CT_{V3}	V_{IN}=1V_{P-P} f=4.43MHz		–70	–50	dB
L_{OUT}1 L_{OUT}2 L_{OUT}3	CT_{L1} CT_{L2} CT_{L3}	V_{IN}=1Vrms f=1kHz		–90	–70	dB
R_{OUT}1 R_{OUT}2 R_{OUT}3	CT_{R1} CT_{R2} CT_{R3}	V_{IN}=1Vrms f=1kHz		–90	–70	dB
[V_{OUT}1]						
Voltage gain	G_{V1}	V_{IN}=1V_{P-P} f=100kHz	–0.5	0	+0.5	dB
Frequency characteristic	F_{V1}	V_{IN}=1V_{P-P} 10MHz/100kHz	–1.0	0	+1.0	dB
Differential gain	DG_1	V_{IN}=1V_{P-P}: staircase APL = 10~90%	–3	0	+3	%
Differential phase	DP_1	V_{IN}=1V_{P-P}: staircase APL = 10~90%	–3	0	+3	deg
Maximam output level	V_{OV1}	f = 100kHz, Maximum output at THD < 1.0%	2.1			V_{P-P}
Input pin voltage	V_{IV1}	No-signal, no-load	2.3	2.8	3.3	V
Output pin voltage	V_{OV1}	No-signal, no-load	1.0	1.5	2.0	V
[V_{OUT}2, V_{OUT}3]						
Voltage gain	G_{V2} G_{V3}	V_{IN}=1V_{P-P} f=100kHz	5.5	6.0	6.5	dB
Frequency characteristic	F_{V2} F_{V3}	V_{IN}=1V_{P-P} 10MHz/100kHz	–1.0	0	+1.0	dB
Differential gain	DG_2 DG_3	V_{IN}=1V_{P-P}: staircase APL = 10~ 90%	–3	0	+3	%

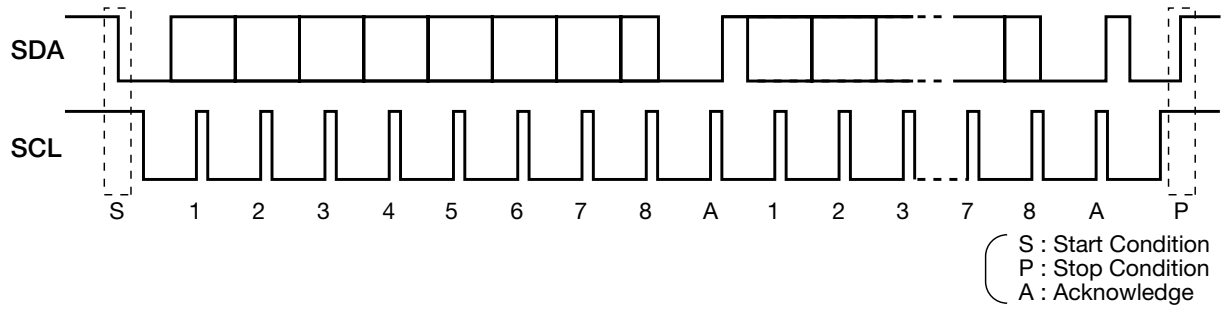
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Differential phase	DP_2 DP_3	V_{IN}=1V_{P-P}: staircase APL = 10~90%	–3	0	+3	deg
Maximam output level	V_{OV2} V_{OV3}	f = 100kHz, Maximum output at THD < 1.0%	4.2			V_{P-P}
Input pin voltage	V_{IV2} V_{IV3}	No-signal, no-load	2.3	2.8	3.3	V
Output pin voltage	V_{OV2} V_{OV3}	No-signal, no-load	1.0	1.5	2.0	V
[L_{OUT}1, R_{OUT}1]						
Voltage gain	G_{1L1}	V_{IN}=1Vrms f=1kHz TUN-L GAIN adjustment at 0dB	–0.5	0	+0.5	dB
	G_{2L1}	V_{IN}=0.25Vrms f=1kHz TUN-L GAIN adjustment at 12dB	11.5	12	12.5	dB
Maximam output level	D_{L1}	V_{CC} = 12V, f = 1kHz Maximum output at THD < 0.5%	3.0			Vrms
Total harmonic distortion	THD_{L1}	V_{IN} such that V_{OUT} = 1Vrms, f = 1kHz		0.03	0.1	%
Output noise voltage	V_{NL1}	A curve band 20kHz		3	50	µVrms
Output offset voltage	V_{OFL1}	DC step for switching	–15	0	15	mV
Input impedance	Z_{INL1}		100	150	200	kΩ
Input pin voltage	V_{IL1}	No-signal, no-load	5.30	5.65	6.00	V
Output pin voltage	V_{OL1}	No-signal, no-load	5.30	5.65	6.00	V
[L_{OUT}2, L_{OUT}3, R_{OUT}2, R_{OUT}3]						
Voltage gain	G_{OL2} G_{OL3}	V_{IN}=1Vrms TUN–L=0dB Output GAIN adjustment at 0dB	–0.5	0	+0.5	dB
	G_{2L2} G_{2L3}	V_{IN}=1Vrms TUN–L=0dB Output GAIN adjustment at 2dB	1.5	2	2.5	dB
	G_{4L2} G_{4L3}	V_{IN}=1Vrms TUN–L=0dB Output GAIN adjustment at 4dB	3.5	4	4.5	dB
	G_{6L2} G_{6L3}	V_{IN}=1Vrms TUN–L=0dB Output GAIN adjustment at 6dB	5.5	6	6.5	dB
Maximam output level	V_{L2} V_{L3}	V_{CC}=12V f=1kHz Maximum output when THD < 0.5%	3.0			Vrms
Total harmonic distortion	THD_{L2} THD_{L3}	V_{IN} such that V_{OUT} = 1Vrms f=1kHz G=0, 2, 4, 6dB		0.03	0.1	%
Output noise voltage	V_{NL2} V_{NL3}	A curve band 20kHz		20	50	µVrms
Output offset voltage	V_{OFL2} V_{OFL3}	DC step for switching	–15	0	15	mV
Input impedance	Z_{INL2} Z_{INL3}		100	150	200	kΩ
Input terminal voltage	V_{IL2} V_{IL3}	No-signal, no-load	5.30	5.65	6.00	V
Output terminal voltage	V_{OL2} V_{OL3}	No-signal, no-load	5.30	5.65	6.00	V
[Logic] (refer to next page)						
Input voltage L	V_{IL}	I²C logic L level judgment value	0.0		1.5	V
Input voltage H	V_{IH}	I²C logic H level judgment value	3.0		5.0	V
Low level output voltage	V_{OL}	for SDA 3mA inflow	0.0		0.4	V
High level input current	I_{IH}	for SDA, SCL = 4.5V impressed	–10		+10	µA
Low level input current	I_{IL}	for SDA, SCL = 0.4V impressed	–10		+10	µA
Clock frequency	f_{SCL}				100	kHz

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Data transfer waiting time	t_{BUF}		4.7			µs
SCL start hold time	$t_{HD:STA}$		4.0			µs
SCL low level hold time	t_{LOW}		4.7			µs
SCL high level hold time	t_{HIGH}		4.0			µs
SCL start setup time	$t_{SU:STA}$		4.7			µs
SDA data hold time	$t_{HD:DAT}$		200			ns
SDA data setup time	$t_{SU:DAT}$		250			ns
SCL rise time	t_R				1000	ns
SCL fall time	t_F				300	ns
SCL stop setup time	$t_{SU:STO}$		4.0			µs

I²C BUS control signal



I²C BUS



I²C BUS (Inter IC BUS) is an inter bus system developed by Philips Co. It transmits and receives data through 2 (SDA, SCL) lines. Data are transmitted and received in the units of bytes by MSB first from the start condition.

[Control registers]

Control registers are data sent from the master for determining the switch condition of the MM1422 series.

S	Slave address							R/W	A	Control Register 1								A	Control Register 2								A	P
	1	0	0	1	0	0	0	0		b7	b6	b5	b4	b3	b2	b1	b0		b7	b6	b5	b4	b3	b2	b1	b0		

Address byte — Control data

The data format of the MM1422 series is set as shown in the above figure. Out of the address bytes, first 7 bits are assigned to the slave addresses, while the residual 1 bit is assigned to the R/W bit. Set the R/W bit to 0 when data are used as control registers. Slave address of the MM1422 series is 90H. Each bit of control registers is reset to 0. MM1422 series consists of one address byte and two control data bytes(3 bytes in total). For details of the control contents of control register 1 and 2, refer to the separate table.

[Control Register 1]

b7	b6	b5	b4	b3	b2	b1	b0
OUT 1 select		OUT 2 select		OUT 3 select		FS CTRL	

[Control Register 2]

b7	b6	b5	b4	b3	b2	b1	b0
0, 12dB select	Port 1 CTRL	Port 2 CTRL	Audio OUT2 gain select		Audio OUT3 gain select		Mute

All data over the limited length (4th and subsequent bytes) are fully neglected. Because of this, the faulty operation that switch changes by the data after the 4th byte doesn't occur.

Each audio output can be set to mute by setting MUTE terminal to high.

[Status registers]

There is no preparation of the status register in MM1422 series. A status register returns all the 1 when is set in the R/W bit.

S	Slave address							R/W	A	status register								NA	P
	1	0	0	1	0	0	0	1		b7	b6	b5	b4	b3	b2	b1	b0		
	Address byte									Status data									

Switch Control Table

[Control register 1] (2nd byte)

b7	b6	b5	b4	b3	b2	b1	b0	V OUT1	A OUT1	V OUT2	A OUT2	V OUT3	A OUT3	FS
0	0							*1	MUTE					
0	1							TUNER	TUNER					
1	0							SCART E1	SCART E1					
1	1							SCART E2	SCART E2					
		0	0							*1	MUTE			
		0	1							TUNER	TUNER			
		1	0							SCART E1	SCART E1			
		1	1							EXT IN	EXT IN			
				0	0							*2	MUTE	
				0	1							EXT IN	EXT IN	
				1	0							SCART E2	SCART E2	
				1	1							SCART E2	SCART E2	
						0	0							Low
						0	1							Middle
						1	0							High
						1	1							High

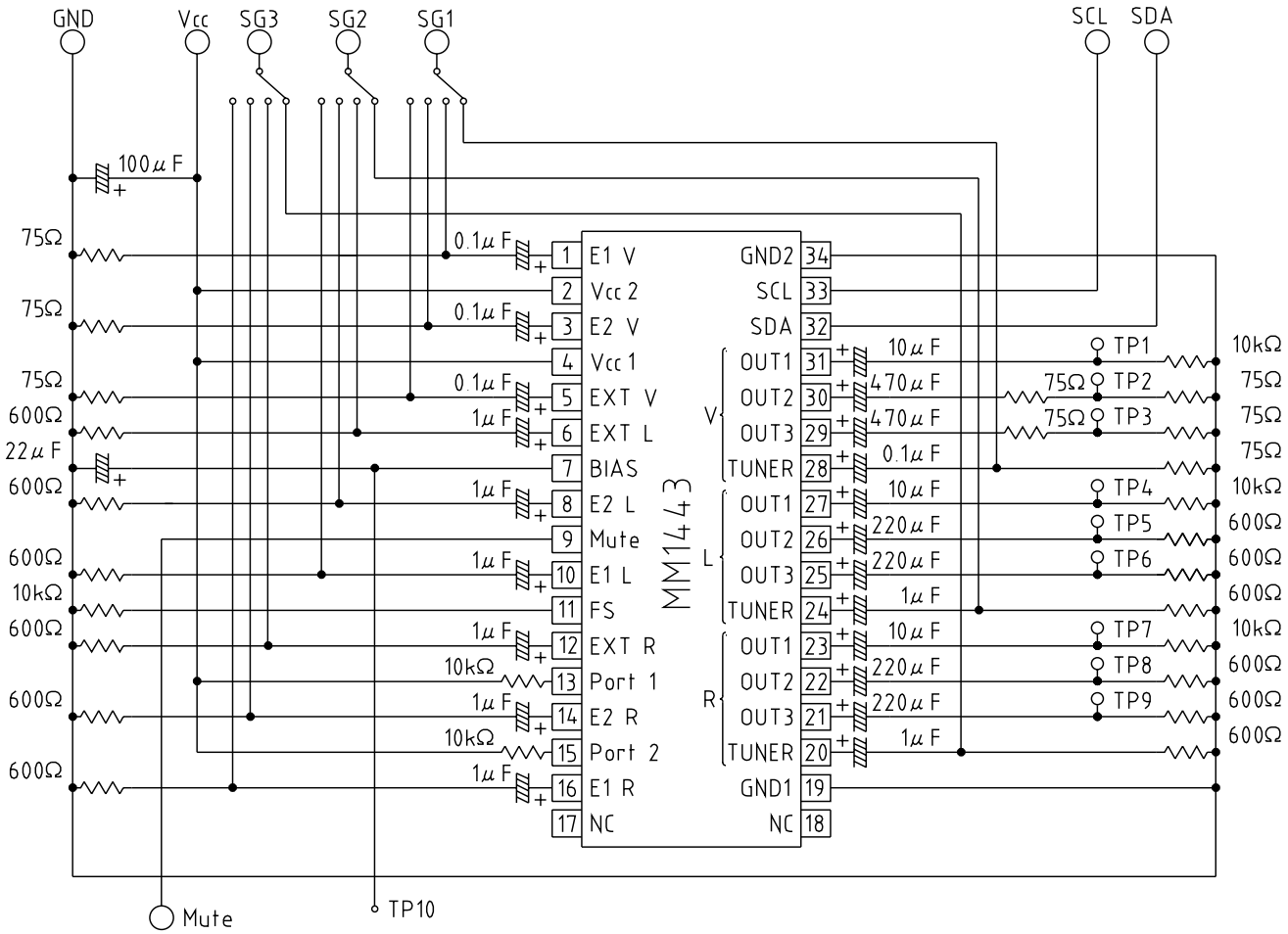
Note 1 : Previous choice condition is held. TUNER is chosen at power on.

Note 2 : Previous choice condition is held. EXT IN is chosen at power on.

[Control register 2] (3rd byte)

b7	b6	b5	b4	b3	b2	b1	b0	0, 12dB	Port 1	Port 2	GainOUT2	GainOUT3	MUTE
0								0dB					
1								12dB					
	0								Low				
	1								High				
		0								Low			
		1								High			
			0	0							0dB		
			0	1							2dB		
			1	0							4dB		
			1	1							6dB		
					0	0						0dB	
					0	1						2dB	
					1	0						4dB	
					1	1						6dB	
							0						OFF
							1						ON

Measuring Circuit



Application Circuit