National Semiconductor

September 2006

DS15BR400/DS15BR401
4-Channel LVDS Buffer/Repeater with Pre-Emphasis

General Description

The DS15BR400/DS15BR401 are four channel LVDS buffer/repeaters capable of datarates of up to 2 Gbps. High speed data paths and flow-through pinout minimize internal device jitter and simplify board layout, while pre-emphasis overcomes ISI jitter effects from lossy backplanes and cables. The differential inputs interface to LVDS, and Bus LVDS signals such as those on National's 10-, 16-, and 18- bit Bus LVDS SerDes, as well as CML and LVPECL. The differential inputs and outputs of the DS15BR400 are internally terminated with 100Ω resistors to improve performance and minimize board space. The DS15BR401 does not have input termination resistors. The repeater function is especially useful for boosting signals for longer distance transmission over lossy cables and backplanes.

The DS15BR400/DS15BR401 are powered from a single 3.3V supply and consume 578 mW (typ). They operate over the full -40˚C to +85˚C industrial temperature range and are available in space saving LLP-32 and TQFP-48 packages.

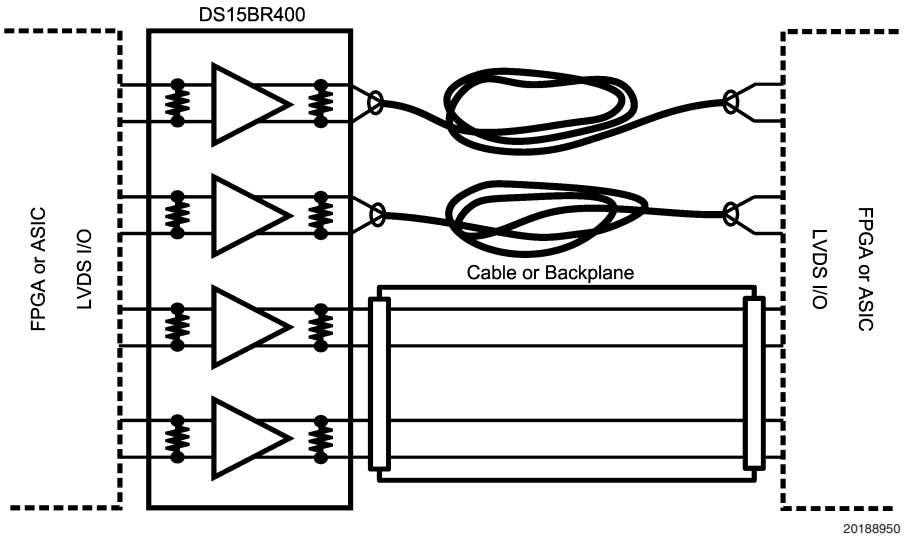
Features

- DC to 2 Gbps low jitter, high noise immunity, low power operation
- 6 dB of pre-emphasis drives lossy backplanes and cables
- LVDS/CML/LVPECL compatible input, LVDS output
- On-chip 100 Ω output termination, optional 100 Ω input termination
- 15 kV ESD protection on LVDS inputs and outputs
- Single 3.3V supply
- Industrial -40 to +85˚C temperature range
- Space saving LLP-32 or TQFP-48 packages
- Evaluation Kit Available

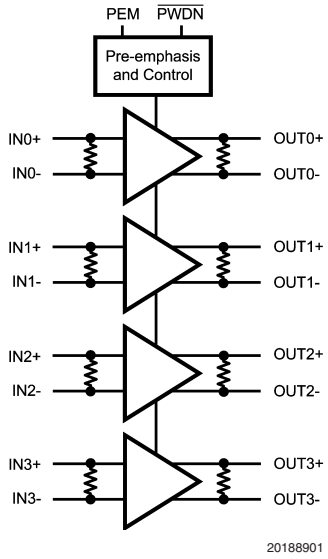
Applications

- Cable extention applications
- Signal repeating and buffering
- Digital routers

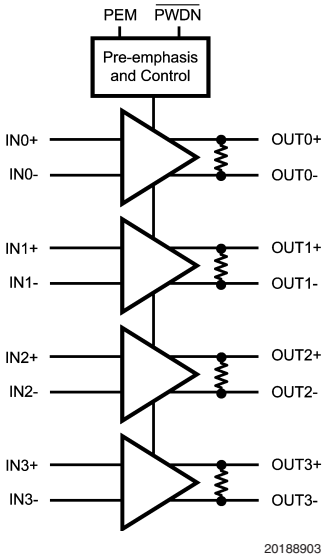
Typical Application



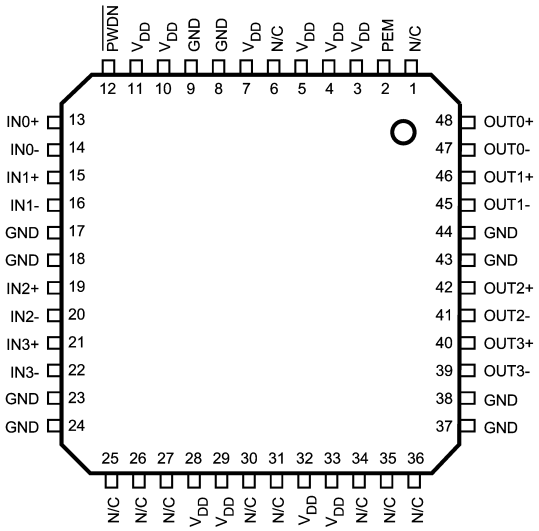
Block and Connection Diagrams



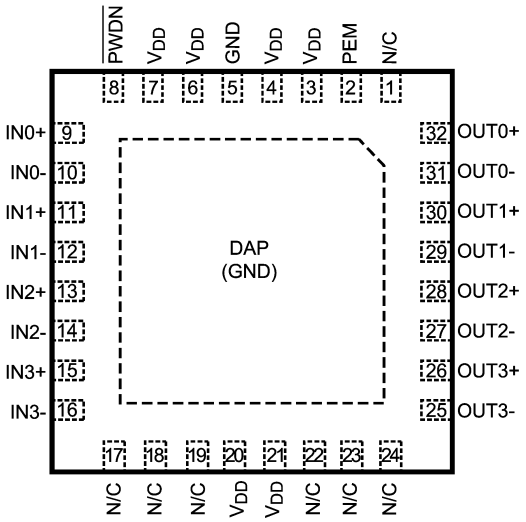
DS15BR400 Block Diagram



DS15BR401 Block Diagram



TQFP Pinout - Top View



LLP Pinout - Top View

Pin Descriptions

Pin Name	TQFP Pin Number	LLP Pin Number	I/O, Type	Description
DIFFERENTIAL INPUTS				
IN0+ IN0–	13 14	9 10	I, LVDS	Channel 0 inverting and non-inverting differential inputs.
IN1+ IN1–	15 16	11 12	I, LVDS	Channel 1 inverting and non-inverting differential inputs.
IN2+ IN2–	19 20	13 14	I, LVDS	Channel 2 inverting and non-inverting differential inputs.
IN3+ IN3–	21 22	15 16	I, LVDS	Channel 3 inverting and non-inverting differential inputs.
DIFFERENTIAL OUTPUTS				
OUT0+ OUT0–	48 47	32 31	O, LVDS	Channel 0 inverting and non-inverting differential outputs. (Note 2)
OUT1+ OUT1–	46 45	30 29	O, LVDS	Channel 1 inverting and non-inverting differential outputs. (Note 2)
OUT2+ OUT2–	42 41	28 27	O, LVDS	Channel 2 inverting and non-inverting differential outputs. (Note 2)
OUT3+ OUT3-	40 39	26 25	O, LVDS	Channel 3 inverting and non-inverting differential outputs. (Note 2)
DIGITAL CONTROL INTERFACE				
$\overline{\text{PWDN}}$	12	8	I, LVTTL	A logic low at $\overline{\text{PWDN}}$ activates the hardware power down mode (all channels).
PEM	2	2	I, LVTTL	Pre-emphasis Control Input (affects all Channels)
POWER				
V_{DD}	3, 4, 5, 7, 10, 11, 28, 29, 32, 33	3, 4, 6, 7, 20, 21	I, Power	V_{DD} = 3.3V, ±10%
GND	8, 9, 17, 18, 23, 24, 37, 38, 43, 44	5 (Note 1)	I, Ground	Ground reference for LVDS and CMOS circuitry. For the LLP package, the DAP is used as the primary GND connection to the device in addition to the pin numbers listed. The DAP is the exposed metal contact at the bottom of the LLP-32 package. It should be connected to the ground plane with at least 4 vias for optimal AC and thermal performance.
N/C	1,6, 25, 26, 27, 30, 31, 34, 35, 36	1, 17, 18,19,22, 23, 24		No Connect

Note 1: Note that for the LLP package the GND is connected thru the DAP on the back side of the LLP package in addition to the actual pin numbers listed.

Note 2: The LVDS outputs do not support a multidrop (BLVDS) environment. The LVDS output characteristics of the DS15BR400 and DS15BR401 are optimized for point-to-point backplane and cable applications.

Absolute Maximum Ratings (Note 3)

Supply Voltage (V_{DD})	−0.3V to +4.0V
CMOS Input Voltage	−0.3V to (V_{DD}+0.3V)
LVDS Receiver Input Voltage	−0.3V to (V_{DD}+0.3V)
LVDS Driver Output Voltage	−0.3V to (V_{DD}+0.3V)
LVDS Output Short Circuit Current	+40 mA
Junction Temperature	+150˚C
Storage Temperature	−65˚C to +150˚C
Lead Temperature (Solder, 4sec)	260˚C
Max Pkg Power Capacity @ 25˚C	
TQFP	1.64W
LLP	4.16W
Thermal Resistance (θ_{JA})	
TQFP	76˚C/W
LLP	30˚C/W
Package Derating above +25˚C	
TQFP	13.2mW/˚C
LLP	33.3mW/˚C
ESD Last Passing Voltage	
HBM, 1.5kΩ, 100pF	8 kV
LVDS pins to GND only	15 kV
EIAJ, 0Ω, 200pF	250V
Charged Device Model	1000V

Recommended Operating Conditions

Supply Voltage (V_{CC})	3.0V to 3.6V
Input Voltage (V_I) (Note 4)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
Industrial	−40˚C to +85˚C

Note 3: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of products outside of recommended operation conditions.

Note 4: V_{ID} max < 2.4V

Electrical Characteristics

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ (Note 5)	Max	Units
LVCMOS DC SPECIFICATIONS ($\overline{PWDN}$, PEM)						
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IH}	High Level Input Current	V_{IN} = V_{DD} = 3.6V ($\overline{PWDN}$ pin)	−10		+10	µA
I_{IHR}	High Level Input Current	V_{IN} = V_{DD} = 3.6V (PEM pin)	40		200	µA
I_{IL}	Low Level Input Current	V_{IN} = V_{SS}, V_{DD} = 3.6V	−10		+10	µA
C_{IN1}	LVCMOS Input Capacitance	Any Digital Input Pin to V_{SS}		5.5		pF
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA, V_{DD} = 0V	−1.5	−0.8		V
LVDS INPUT DC SPECIFICATIONS (INn±)						
V_{TH}	Differential Input High Threshold (Note 6)	V_{CM} = 0.8V to 3.55V, V_{DD} = 3.6V		0	100	mV
V_{TL}	Differential Input Low Threshold (Note 6)	V_{CM} = 0.8V to 3.55V, V_{DD} = 3.6V	−100	0		mV
V_{ID}	Differential Input Voltage	V_{CM} = 0.8V to 3.55V, V_{DD} = 3.6V	100		2400	mV
V_{CMR}	Common Mode Voltage Range	V_{ID} = 150 mV, V_{DD} = 3.6V	0.05		3.55	V
C_{IN2}	LVDS Input Capacitance	IN+ or IN− to V_{SS}		3.0		pF
I_{IN}	Input Current	V_{IN} = 3.6V, V_{DD} = 3.6V	−10		+10	µA
		V_{IN} = 0V, V_{DD} = 3.6V	−10		+10	µA

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ (Note 5)	Max	Units
LVDS OUTPUT DC SPECIFICATIONS (OUTn±)						
V_{OD}	Differential Output Voltage, 0% Pre-emphasis (Note 6)	R_L = 100Ω external resistor between OUT+ and OUT– *Figure 1*	250	360	500	mV
ΔV_{OD}	Change in V_{OD} between Complementary States		–35		35	mV
V_{OS}	Offset Voltage (Note 7)		1.05	1.18	1.475	V
ΔV_{OS}	Change in V_{OS} between Complementary States		–35		35	mV
C_{OUT}	LVDS Output Capacitance	OUT+ or OUT– to V_{SS}		2.5		pF
I_{OS}	Output Short Circuit Current	OUT+ or OUT– Short to GND		–21	–40	mA
		OUT+ or OUT– Short to VDD		6	40	mA
SUPPLY CURRENT (Static)						
I_{CC}	Supply Current	All inputs and outputs enabled and active, terminated with differential load of 100Ω between OUT+ and OUT-. PEM = L		175	215	mA
I_{CCZ}	Supply Current - Power Down Mode	$\overline{PWDN}$ = L, PEM = L		20	200	µA
SWITCHING CHARACTERISTICS—LVDS OUTPUTS						
t_{LHT}	Differential Low to High Transition Time (Note 12)	Use an alternating 1 and 0 pattern at 200 Mbps, measure between 20% and 80% of V_{OD}. *Figures 2, 4*		170	250	ps
t_{HLT}	Differential High to Low Transition Time (Note 12)			170	250	ps
t_{PLHD}	Differential Low to High Propagation Delay	Use an alternating 1 and 0 pattern at 200 Mbps, measure at 50% V_{OD} between input to output. *Figures 2, 3*		1.0	2.0	ns
t_{PHLD}	Differential High to Low Propagation Delay			1.0	2.0	ns
t_{SKD1}	Pulse Skew (Note 12)	$\lvert t_{PLHD} - t_{PHLD} \rvert$		10	60	ps
t_{SKCC}	Output Channel to Channel Skew (Note 12)	Difference in propagation delay (t_{PLHD} or t_{PHLD}) among all output channels.		25	75	ps
t_{SKP}	Part to Part Skew (Note 12)	Common edge, parts at same temp and V_{CC}			550	ps
t_{JIT}	Jitter (0% Pre-emphasis) (Note 8)	RJ - Alternating 1 and 0 at 750 MHz (Note 9)		0.5	1.5	ps
		DJ - K28.5 Pattern, 1.5 Gbps (Note 10)		14	30	ps
		TJ - PRBS 2^{23}-1 Pattern, 1.5 Gbps (Note 11)		14	31	ps
t_{ON}	LVDS Output Enable Time	Time from $\overline{PWDN}$ to OUT± change from TRI-STATE to active. *Figures 5, 6*			20	µs
t_{OFF}	LVDS Output Disable Time	Time from $\overline{PWDN}$ to OUT± change from active to TRI-STATE. *Figures 5, 6*			12	ns

Note 5: Typical parameters are measured at V_{DD} = 3.3V, T_A = 25˚C. They are for reference purposes, and are not production-tested.

Note 6: Differential output voltage V_{OD} is defined as ABS(OUT+–OUT–). Differential input voltage V_{ID} is defined as ABS(IN+–IN–).

Note 7: Output offset voltage V_{OS} is defined as the average of the LVDS single-ended output voltages at logic high and logic low states.

Note 8: Jitter is not production tested, but guaranteed through characterization on a sample basis.

Note 9: Random Jitter, or RJ, is measured RMS with a histogram including 1500 histogram window hits. Stimulus and fixture Jitter has been subtracted. The input voltage = V_{ID} = 500 mV, input common mode voltage = V_{ICM} = 1.2V, 50% duty cycle at 750 MHz, t_r = t_f = 50 ps (20% to 80%).

Note 10: Deterministic Jitter, or DJ, is a peak to peak value. Stimulus and fixture jitter has been subtracted. The input voltage = V_{ID} = 500 mV, input common mode voltage = V_{ICM} = 1.2V, K28.5 pattern at 1.5 Gbps, t_r = t_f = 50 ps (20% to 80%). The K28.5 pattern is repeating bit streams of (0011111010 1100000101).

Note 11: Total Jitter, or TJ, is measured peak to peak with a histogram including 3500 window hits. Stimulus and fixture Jitter has been subtracted. The input voltage = V_{ID} = 500 mV, input common mode voltage = V_{ICM} = 1.2V, 2^{23}-1 PRBS pattern at 1.5 Gbps, t_r = t_f = 50 ps (20% to 80%).

Note 12: Not production tested. Guaranteed by a statistical analysis on a sample basis at the time of characterization.

DC Test Circuits

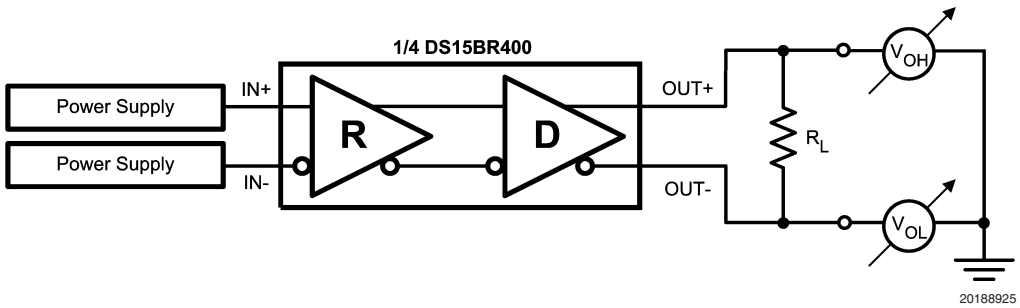


FIGURE 1. Differential Driver DC Test Circuit

AC Test Circuits and Timing Diagrams

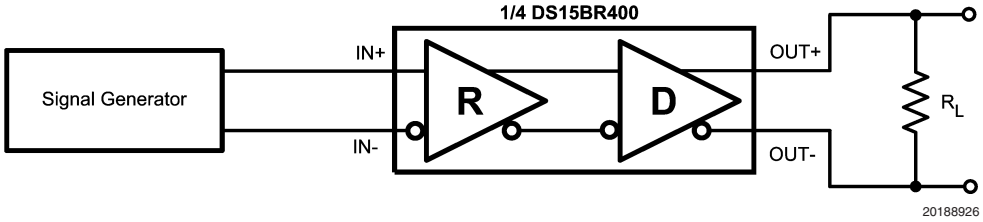


FIGURE 2. Differential Driver AC Test Circuit

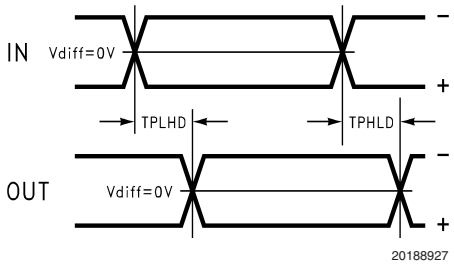


FIGURE 3. Propagation Delay Timing Diagram

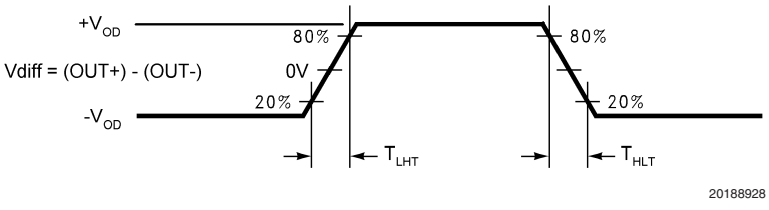


FIGURE 4. LVDS Output Transition Times

AC Test Circuits and Timing Diagrams (Continued)

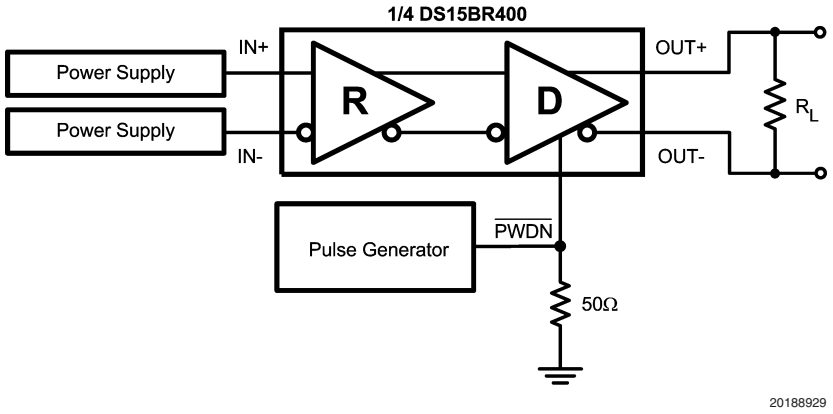


FIGURE 5. Enable/Disable Time Test Circuit

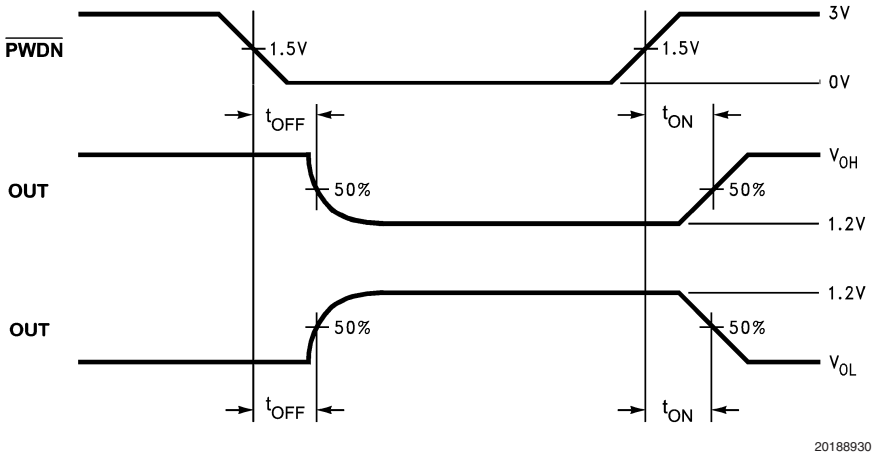


FIGURE 6. Enable/Disable Time Diagram

Application Information

INTERNAL TERMINATIONS

The DS15BR400 has integrated termination resistors on both the input and outputs. The inputs have a 100Ω resistor across the differential pair, placing the receiver termination as close as possible to the input stage of the device. The LVDS outputs also contain an integrated 100Ω ohm termination resistor, this resistor is used to minimize the output return loss and does not take the place of the 100 ohm termination at the inputs to the receiving device. The integrated terminations improve signal integrity and decrease the external component count resulting in space savings. The DS15BR401 has 100Ω output terminations only.

OUTPUT CHARACTERISTICS

The output characteristics of the DS15BRB400/DS15BR401 have been optimized for point-to-point backplane and cable applications, and are not intended for multipoint or multidrop signaling.

POWERDOWN MODE

The $\overline{\text{PWDN}}$ input activates a hardware powerdown mode. When the powerdown mode is active ($\overline{\text{PWDN}}$=L), all input and output buffers and internal bias circuitry are powered off. When exiting powerdown mode, there is a delay associated with turning on bandgap references and input/output buffer circuits as indicated in the LVDS Output Switching Characteristics

PRE-EMPHASIS

Pre-emphasis dramatically reduces ISI jitter from long or lossy transmission media. One pin is used to select the pre-emphasis level for all outputs, off or on. The pre-emphasis boost is approximately 6 dB at 750 MHz.

Pre-emphasis Control Selection Table

PEM	Pre-Emphasis
0	Off
1	On

INPUT FAILSAFE BIASING

External pull up and pull down resistors may be used to provide enough of an offset to enable an input failsafe under open-circuit conditions. This configuration ties the positive LVDS input pin to V_{DD} thru a pull up resistor and the negative LVDS input pin is tied to GND by a pull down resistor. The pull up and pull down resistors should be in the 5kΩ to 15kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point ideally should be set to approximately 1.2V. Please refer to application note AN-1194 “Failsafe Biasing of LVDS Interfaces” for more information.

DECOUPLING

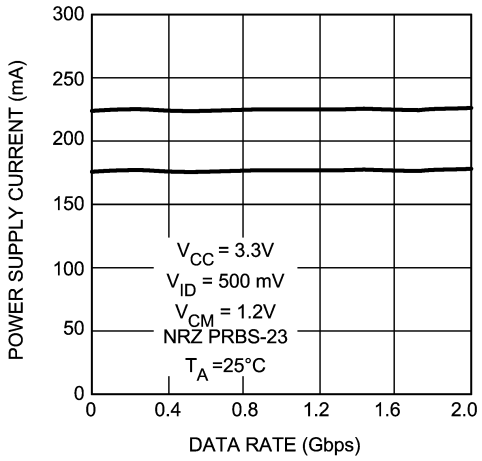
Each power or ground lead of the DS15BR400 should be connected to the PCB through a low inductance path. For best results, one or more vias are used to connect a power or ground pin to the nearby plane. Ideally, via placement is immediately adjacent to the pin to avoid adding trace inductance. Placing power plane closer to the top of the board reduces effective via length and its associated inductance.

Bypass capacitors should be placed close to VDD pins. Small physical size capacitors, such as 0402, X7R, surface mount capacitors should be used to minimize body inductance of capacitors. Each bypass capacitor is connected to the power and ground plane through vias tangent to the pads of the capacitor. An X7R surface mount capacitor of size 0402 has about 0.5 nH of body inductance. At frequencies above 30 MHz or so, X7R capacitors behave as low impedance inductors. To extend the operating frequency range to a few hundred MHz, an array of different capacitor values like 100 pF, 1 nF, 0.03 µF, and 0.1 µF are commonly used in parallel. The most effective bypass capacitor can be built using sandwiched layers of power and ground at a separation of 2–3 mils. With a 2 mil FR4 dielectric, there is approximately 500 pF per square inch of PCB.

The center dap of the LLP package housing the DS15BR400 should be connected to a ground plane through an array of vias. The via array reduces the effective inductance to ground and enhances the thermal performance of the LLP package.

Typical Performance Characteristics

Power Supply Current vs. Data Rate



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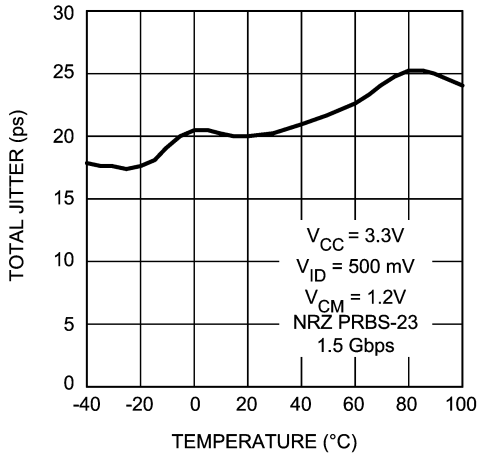
Total Jitter vs. Ambient Temperature



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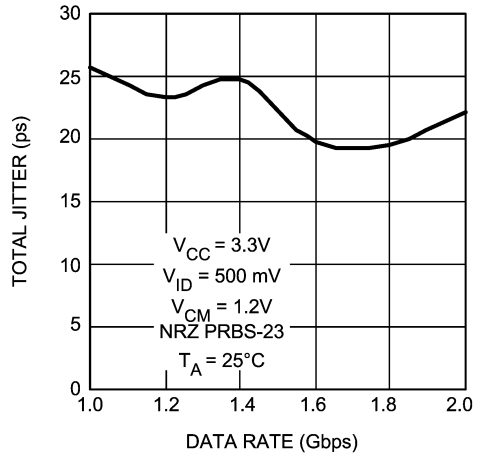
Total Jitter vs. Data Rate



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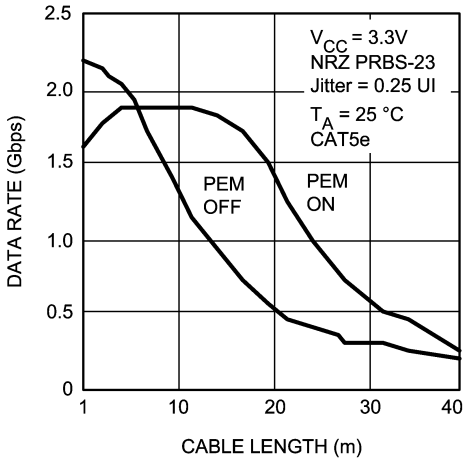
Data Rate vs. Cable Length (0.25 UI Criteria)



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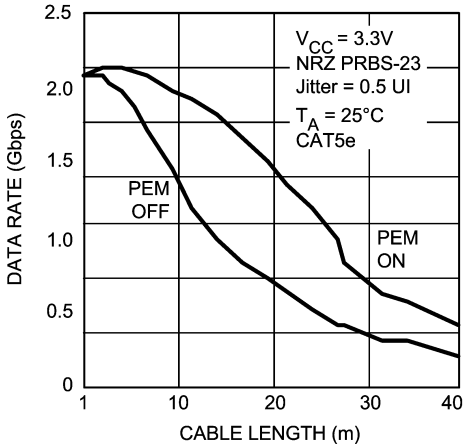
Data presented in this graph was collected using the DS15BR400EVK, a pair of RJ-45 to SMA adapter boards and various length Belden 1700a cables. The maximum data rate was determined based on total jitter (0.25 UI criteria) measured after the cable. The total jitter was a peak to peak value measured with a histogram including 3000 window hits.

Data Rate vs. Cable Length (0.5 UI Criteria)



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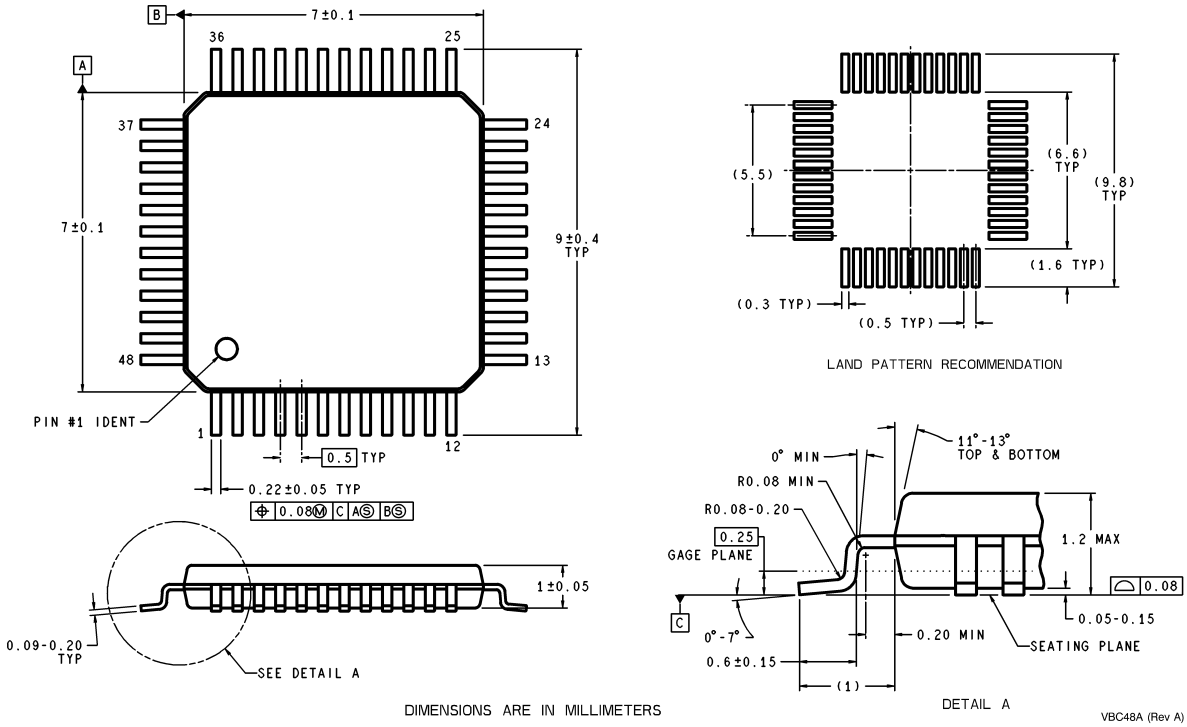
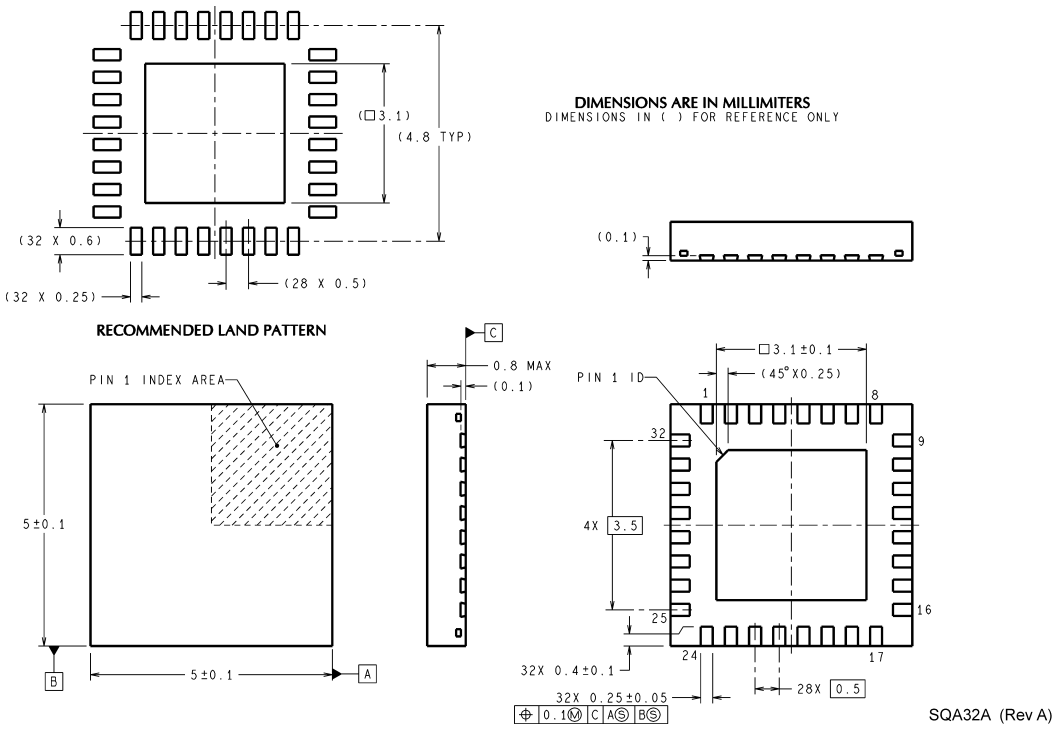
Data presented in this graph was collected using the DS15BR400EVK, a pair of RJ-45 to SMA adapter boards and various length Belden 1700a cables. The maximum data rate was determined based on total jitter (0.5 UI criteria) measured after the cable. The total jitter was a peak to peak value measured with a histogram including 3000 window hits.

Physical Dimensions inches (millimeters) unless otherwise noted



48-TQFP
NS Package Number VBC48a
Order Number DS15BR400TVS, DS15BR401TVS (250 piece Tray)
Order Number DS15BR400TVSX, DS15BR401TVSX (1000 piece Tape and Reel)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



32-LLP
(See AN-1187 for PCB Design and Assembly Recommendations)
NS Package Number SQA32A
Order Number DS15BR400TSQ, DS15BR401TSQ (1000 piece Tape and Reel)
DS15BR400TSQX, DS15BR401TSQX (4500 piece Tape and Reel)

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