



T-77-11

ML926/7

REMOTE CONTROL RECEIVERS (WITH MOMENTARY OUTPUTS)

The ML926 and ML927 are MOS LSI monolithic circuits for use as receivers of remote control signals for television control and many other applications. They are general purpose devices each receiving sixteen of the thirty-two codes transmitted by the SL490 circuit as pulse position modulation (PPM).

FEATURES

- Minimum Package Size — 8-Lead Minidip
- Four Outputs Indicate in Binary the Code Currently Being Received, and Are Switched Off (Low) When No Valid Code Is Detected.
- On-Chip Oscillator
- High Power, Free Drain, Output Buffers

OPERATING NOTES

The receiver operates on a timescale fixed by an internal oscillator and its external timing components. The oscillator may be adjusted to any value between 15Hz and 150kHz (allowing different receivers to respond to different transmission rates within the same area).

Checks are made to ensure 6 pulses, or 5 bits, are received for a word to be valid, and only after two consecutive and identical words is the receiver allowed to respond to the incoming code.

The ML926 responds only to codes 00001 to 01111 from the SL490 transmitter whereas the ML927 responds to codes 10001 to 11111.

ABSOLUTE MAXIMUM RATINGS

V _{DD} supply and inputs w.r.t. V _{SS}	+0.3V to -25V
Storage temperature	-55°C to +125°C
Operating temperature ambient	-10°C to +65°C

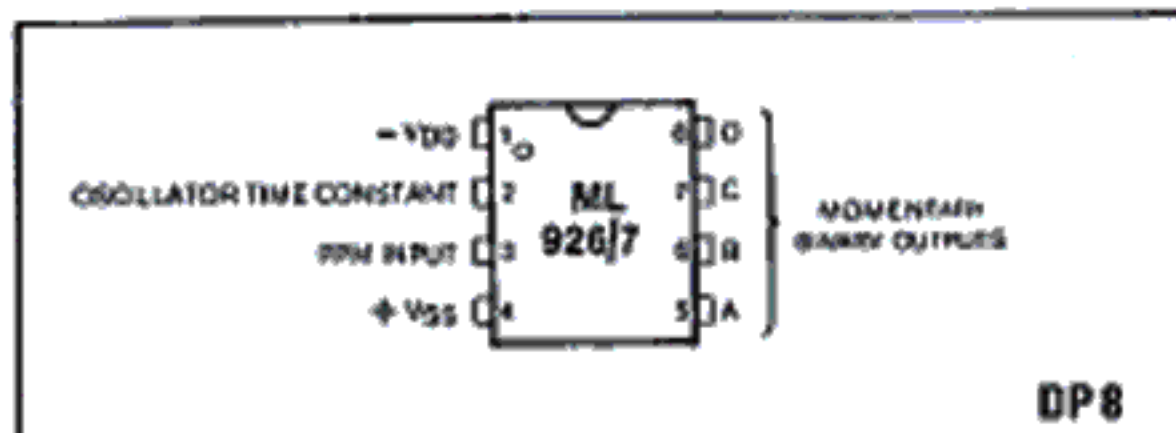


Fig. 1 Pin connections (top view)

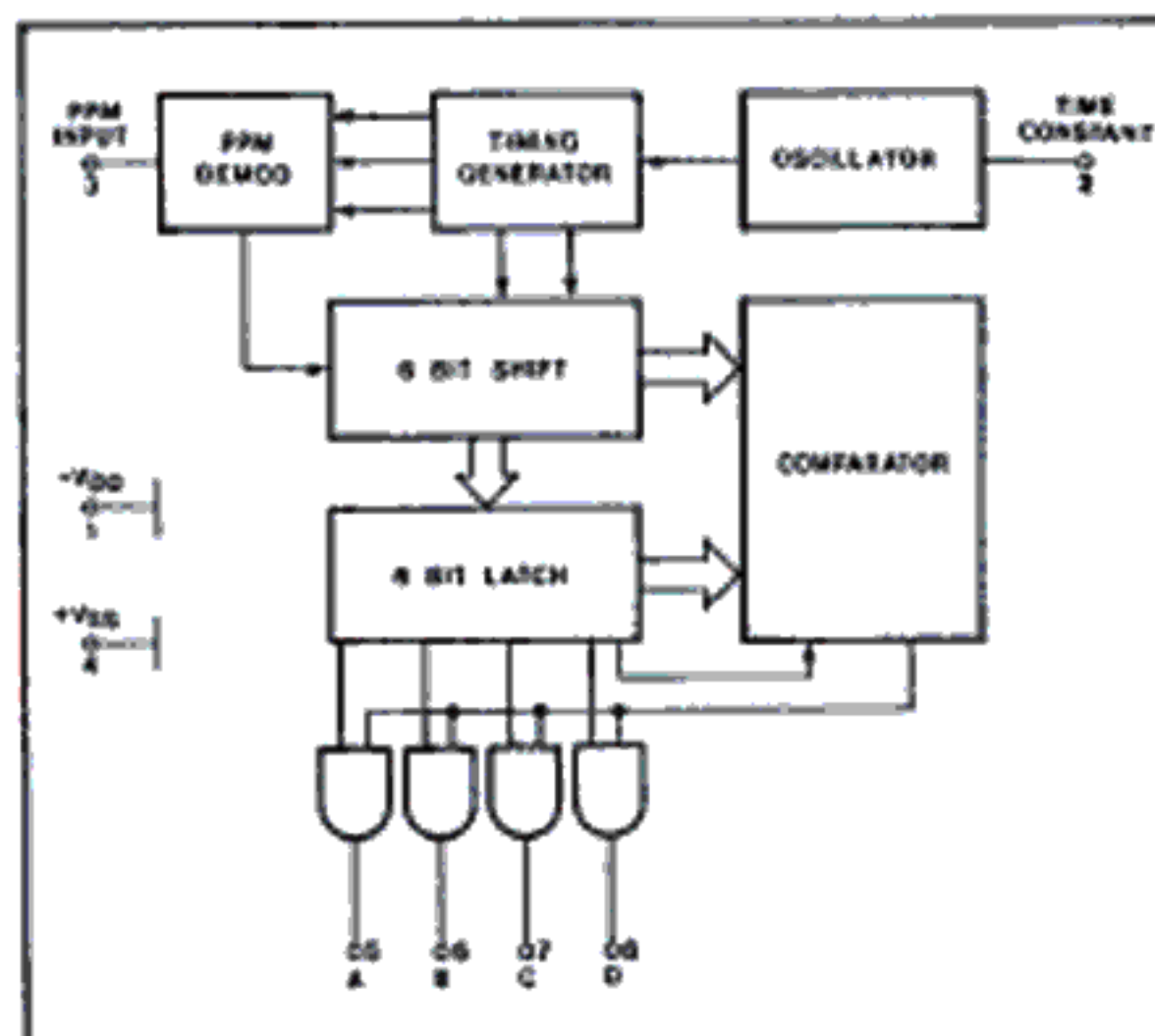


Fig 2 Block diagram

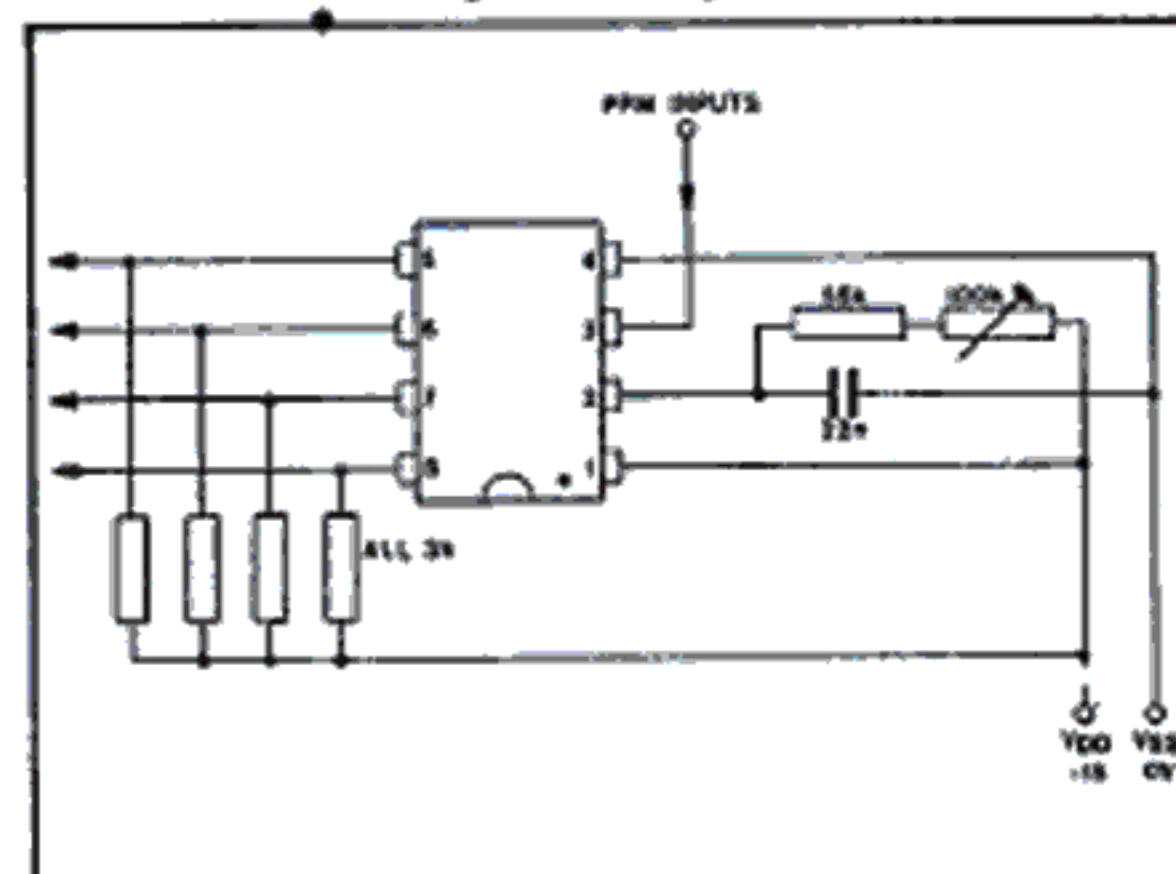


Fig. 3 Test circuit

ELECTRICAL CHARACTERISTICS

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Test Conditions (unless otherwise stated):

$V_{DD} = -16V$, $V_{SS} = 0V$

$T_{amb.} = 25^{\circ}C$

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating supply voltage range	1	12	14	18	V	
Current consumption	1	2	3	4	mA	
PPM Input						
Input level high	3	-1		0	V	
Input level low	3	V_{DD}		-6	V	
Input pulse width	3	1		$22T_{osc}$	μsec	$T = \frac{1}{f_{osc}}$
Oscillator time constant See Note 1						
Oscillator frequency	2	15	3k	150k	Hz	
Variation wrt V_{DD}			1		%/V	Typical TC: 22nF to V_{SS} 100k Ω to V_{DD}
Output voltage high	5-8	-1.5		0	V	$R_L = 3.0K$ to V_{DD}
Output device leakage (Output OFF)	5-8			1	μA	

Note 1. R_{osc} (Pin 2) is 56k-156k Ω , $f_{osc} \approx \frac{1}{0.15CR} \pm 20\%$

PIN FUNCTIONS

POSITIVE LOGIC '1' = V_{SS} , '0' = V_{DD}

1. V_{DD}

-14V to -18V power supply

2. Oscillator time constant

An RC time constant of a capacitor and resistor at this pin defines the internal clock frequency. The clock frequency may be varied from 15Hz to 150kHz.

3. PPM input

The output of the 'front end' amplifier is connected to this pin; the signal must consist of a normal 'low' level with pulses to high level corresponding to the PPM pulses from the transmitter.

4. V_{SS}

0V (ground)

5-8. A,B,C,D

Four open drain high power transistors give a binary coded output of the valid code being received.

Transmitter Code	Momentary binary outputs			
	ML926		ML927	
	E D C B A	D C B A	D C B A	
0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
0 0 0 0 1	0 0 0 1	0 0 0 1	0 0 0 1	
0 0 0 1 0	0 0 1 0	0 0 1 0	0 0 1 0	
0 0 0 1 1	0 0 1 1	0 0 1 1	0 0 1 1	
0 0 1 0 0	0 1 0 0	0 1 0 0	0 1 0 0	
0 0 1 0 1	0 1 0 1	0 1 0 1	0 1 0 1	
0 0 1 1 0	0 1 1 0	0 1 1 0	0 1 1 0	
0 0 1 1 1	0 1 1 1	0 1 1 1	0 1 1 1	
0 1 0 0 0	1 0 0 0	1 0 0 0	1 0 0 0	
0 1 0 0 1	1 0 0 1	1 0 0 1	1 0 0 1	
0 1 0 1 0	1 0 1 0	1 0 1 0	1 0 1 0	
0 1 0 1 1	1 0 1 1	1 0 1 1	1 0 1 1	
0 1 1 0 0	1 1 0 0	1 1 0 0	1 1 0 0	
0 1 1 0 1	1 1 0 1	1 1 0 1	1 1 0 1	
0 1 1 1 0	1 1 1 0	1 1 1 0	1 1 1 0	
0 1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	
1 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
1 0 0 0 1	0 0 0 1	0 0 0 1	0 0 0 1	
1 0 0 1 0	0 0 1 0	0 0 1 0	0 0 1 0	
1 0 0 1 1	0 0 1 1	0 0 1 1	0 0 1 1	
1 0 1 0 0	0 1 0 0	0 1 0 0	0 1 0 0	
1 0 1 0 1	0 1 0 1	0 1 0 1	0 1 0 1	
1 0 1 1 0	0 1 1 0	0 1 1 0	0 1 1 0	
1 0 1 1 1	0 1 1 1	0 1 1 1	0 1 1 1	
1 1 0 0 0	1 0 0 0	1 0 0 0	1 0 0 0	
1 1 0 0 1	1 0 0 1	1 0 0 1	1 0 0 1	
1 1 0 1 0	1 0 1 0	1 0 1 0	1 0 1 0	
1 1 0 1 1	1 0 1 1	1 0 1 1	1 0 1 1	
1 1 1 0 0	1 1 0 0	1 1 0 0	1 1 0 0	
1 1 1 0 1	1 1 0 1	1 1 0 1	1 1 0 1	
1 1 1 1 0	1 1 1 0	1 1 1 0	1 1 1 0	
1 1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	

Table 1 Response to SL490 codes