

## DS7834/DS8834 Quad TRI-STATE® Bus Transceivers

### General Description

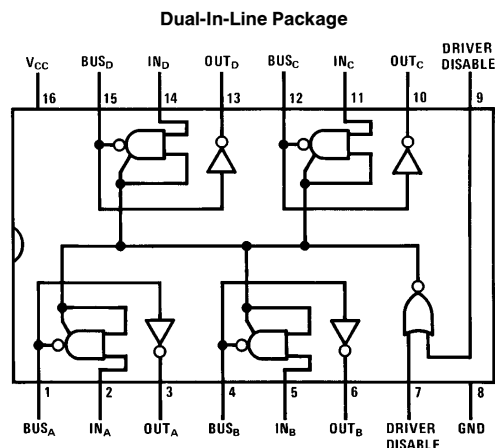
This family of TRI-STATE bus transceivers offers extreme versatility in bus organized data transmission systems. The data bus may be unterminated, or terminated DC or AC, at one or both ends. Drivers in the third (high impedance) state load the data bus with a negligible leakage current. The receiver input current is low, allowing at least 100 driver/receiver pairs to utilize a single bus. The bus loading is unchanged when  $V_{CC} = 0V$ . The receiver incorporates hysteresis to provide greater noise immunity. Both devices utilize a high current TRI-STATE output driver. The DS7834/DS8834 employs TTL outputs on the receiver.

The DS7834/DS8834 are inverting quad transceivers with two common inverter driver disable controls.

### Features

- Receiver hysteresis 400 mV typ
- Receiver noise immunity 1.4V typ
- Bus terminal current for normal  $V_{CC}$  or  $V_{CC} = 0V$  80  $\mu A$  max
- Receivers
  - Sink 16 mA at 0.4V max
  - Source 2.0 mA (Mil) at 2.4V min
  - 5.2 mA (Com) at 2.4V min
- Drivers
  - Sink 50 mA at 0.5V max
  - Source 32 mA at 0.4V max
  - 10.4 mA (Com) at 2.4V min
  - 5.2 mA (Mil) at 2.4V min
- Drivers have TRI-STATE outputs
- Receivers have TRI-STATE outputs
- Capable of driving 100 $\Omega$  DC-terminated Buses
- Compatible with Series 54/74

### Connection Diagram



TL/F/5809-1

**Top View**  
Order Number DS7834J, or DS8834N  
See NS Package Number J16A or N16A

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## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW

\*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

## Operating Conditions

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )			
DS7834	4.5	5.5	V
DS8834	4.75	5.25	V
Temperature ( $T_A$ )			
DS7834	−55	+125	°C
DS8834	0	+70	°C

## Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units	
DISABLE/DRIVER INPUT								
V <sub>IH</sub>	High Level Input Voltage	V <sub>CC</sub> = Min		2.0			V	
V <sub>IL</sub>	Low Level Input Voltage	V <sub>CC</sub> = Min				0.8	V	
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = Max	V <sub>IN</sub> = 2.4V			40	μA	
			V <sub>IN</sub> = 5.5V			1.0	mA	
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = Max, V <sub>IN</sub> = 0.4V			−1.0	−1.6	mA	
I <sub>IND</sub>	Driver Disabled Input Low Current	Driver Disable Input = 2.0V, V <sub>IN</sub> = 0.4V				−40	μA	
V <sub>CL</sub>	Input Clamp Diode	V <sub>CC</sub> = 5.0V, I <sub>IN</sub> = −12 mA, T <sub>A</sub> = 25°C			−0.8	−1.5	V	
RECEIVER INPUT/BUS OUTPUT								
V <sub>TH</sub>	High Level Threshold Voltage	V <sub>CC</sub> = Max		DS7834	1.4	1.75	2.1	V
				DS8834	1.5	1.75	2.0	V
V <sub>TL</sub>	Low Level Threshold Voltage	V <sub>CC</sub> = Min		DS7834	0.8	1.35	1.6	V
				DS8834	0.8	1.35	1.5	V
I <sub>BH</sub>	Bus Current, Output Disabled or High	V <sub>BUS</sub> = 4.0V	V <sub>CC</sub> = Max, Disable Input = 2.0V			25	80	μA
			V <sub>CC</sub> = 0V			5.0	80	μA
		V <sub>CC</sub> = Max, V <sub>SUS</sub> = 0.4V, Disable Input = 2.0V					−40	μA
V <sub>OH</sub>	Logic “1” Output Voltage	V <sub>CC</sub> = Min	I <sub>OUT</sub> = −5.2 mA	DS7834	2.4	2.75		V
			I <sub>OUT</sub> = −10.4 mA	DS7834	2.4	2.75		V
V <sub>OL</sub>	Logic “0” Output Voltage	V <sub>CC</sub> = Min	I <sub>OUT</sub> = 50 mA			0.28	0.5	V
			I <sub>OUT</sub> = 32 mA				0.4	V
I <sub>OS</sub>	Output Short Circuit Current	V <sub>CC</sub> = Max, (Note 4)			−40	−62	−120	mA
RECEIVER OUTPUT								
V <sub>OH</sub>	Logic “1” Output Voltage	V <sub>CC</sub> = Min	I <sub>OUT</sub> = −2.0 mA	DS7834	2.4	3.0		V
			I <sub>OUT</sub> = −5.2 mA	DS8834	2.4	2.9		V
V <sub>OL</sub>	Logic “0” Output Voltage	V <sub>CC</sub> = Min, I <sub>OUT</sub> = 16 mA				0.22	0.4	V
I <sub>OS</sub>	Output Short Circuit Current	V <sub>CC</sub> = Max, (Note 4)		DS7834	−28	−40	−70	mA
				DS8834	−30		−70	mA
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = Max				75	95	mA

**Note 1:** “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. Except for “Operating Temperature Range” they are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” provides conditions for actual device operation.

**Note 2:** Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS7834 and across the 0°C to +70°C range for the DS8834. All typicals are given for  $V_{CC} = 5.0\text{V}$  and  $T_A = 25^\circ\text{C}$ .

**Note 3:** All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

**Note 4:** Only one output at a time should be shorted.

## Switching Characteristics $V_{CC} = 5.0V$ , $T_A = 25^\circ C$

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$t_{pd0}$	Propagation Delay to a Logic "0" from Input to Bus	(Figure 1)	DS7834/DS8834		10	20	ns
$t_{pd1}$	Propagation Delay to a Logic "1" from Input to Bus	(Figure 1)	DS7834/DS8834		11	30	ns
$t_{pd0}$	Propagation Delay to a Logic "0" from Bus to Output	(Figure 2)	DS7834/DS8834		16	35	ns
$t_{pd1}$	Propagation Delay to a Logic "1" from Bus to Output	(Figure 2)	DS7834/DS8834		18	30	ns
$t_{PHZ}$	Delay from Disable Input to High Impedance State (from Logic "1" Level)	$C_L = 5.0$ pF, (Figures 1 and 2) Driver Only			8	20	ns
$t_{PLZ}$	Delay from Disable Input to High Impedance State (from Logic "0" Level)	$C_L = 5.0$ pF, (Figures 1 and 2) Driver Only			20	35	ns
$t_{PZH}$	Delay from Disable Input to Logic "1" Level (from High Impedance State)	$C_L = 50$ pF, (Figures 1 and 2) Driver Only			24	40	ns
$t_{PZL}$	Delay from Disable Input to Logic "0" Level (from High Impedance State)	$C_L = 50$ pF, (Figures 1 and 2) Driver Only			19	35	ns

## AC Test Circuit

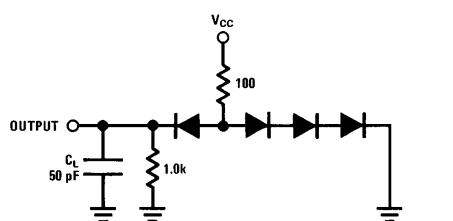


FIGURE 1. Driver Output Load

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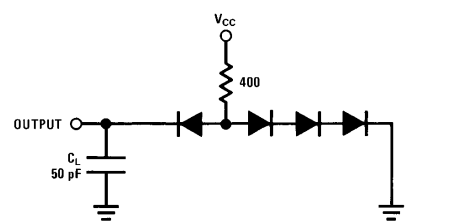
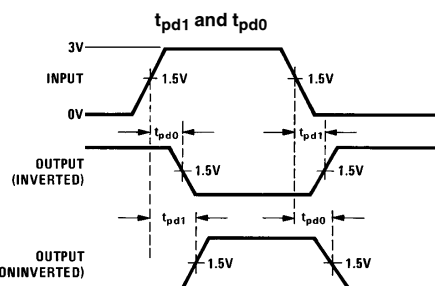


FIGURE 2. Receiver Output Load

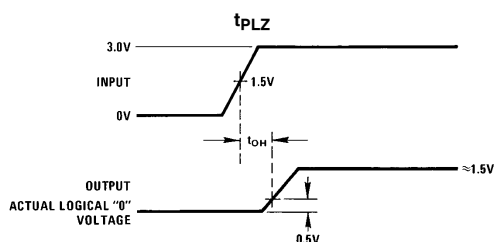
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## Switching Time Waveforms



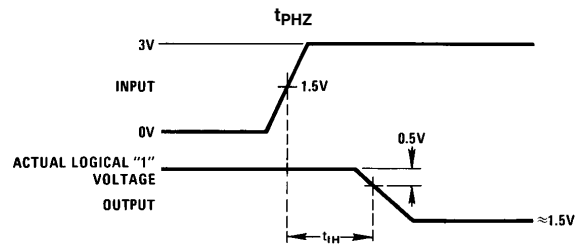
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$f = 1$  MHz  
 $t_r = t_f \leq 10$  ns (10% to 90%)  
 Duty Cycle = 50%

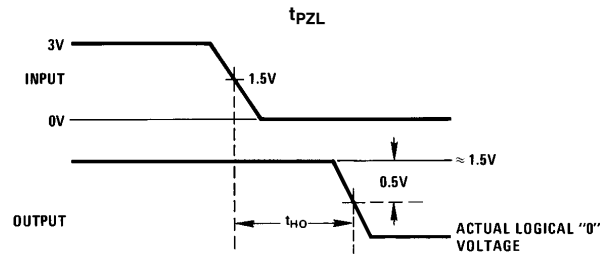


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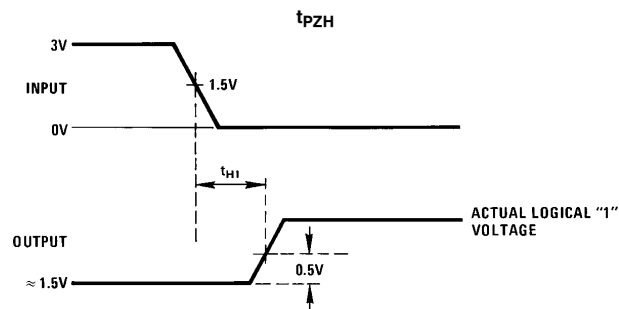
## Switching Time Waveforms (Continued)



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TL/F/5809-8



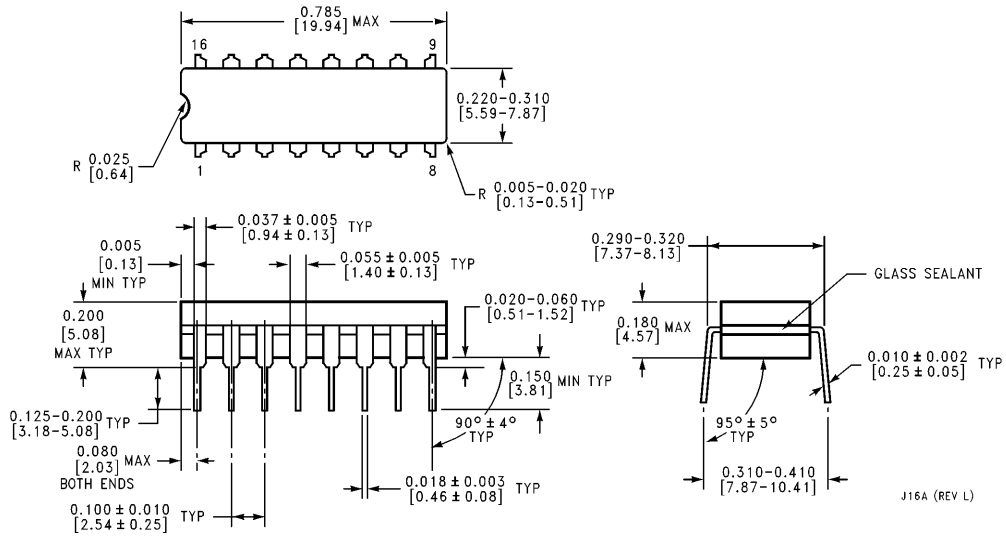
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## Truth Table

Disable Input	Driver Input ( $IN_X$ )	Receiver Input/ Bus Output ( $BUS_X$ )	Receiver Output ( $OUT_X$ )	Mode of Operation
<b>DS7834/DS8834</b>				
1	X		$\overline{BUS}$	Receive Bus Signal
0	1	0	1	Drive Bus
0	0	1	0	Drive Bus

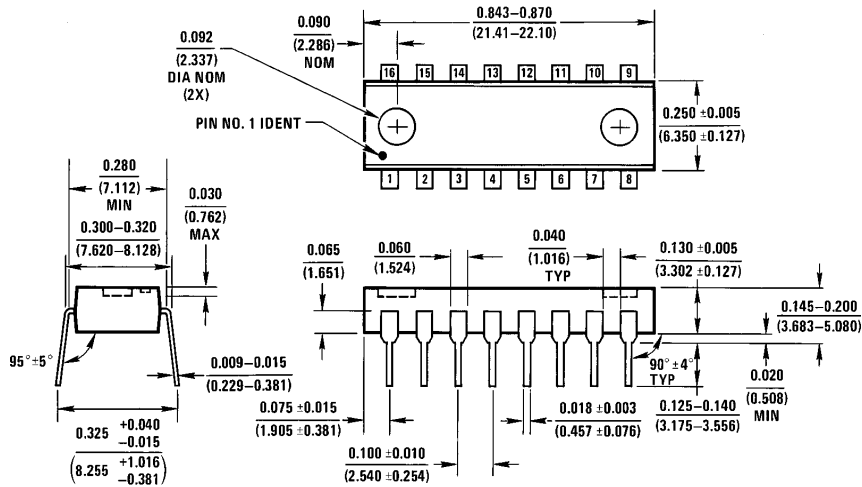
X = Don't care

# Physical Dimensions inches (millimeters)



**Ceramic Dual-In-Line Package (J)**  
**Order Number DS7834J**  
**NS Package Number J16A**

# Physical Dimensions inches (millimeters) (Continued)



N16A (REV E)

**Molded Dual-In-Line Package (N)**  
**Order Number DS8834N**  
**NS Package Number N16A**

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