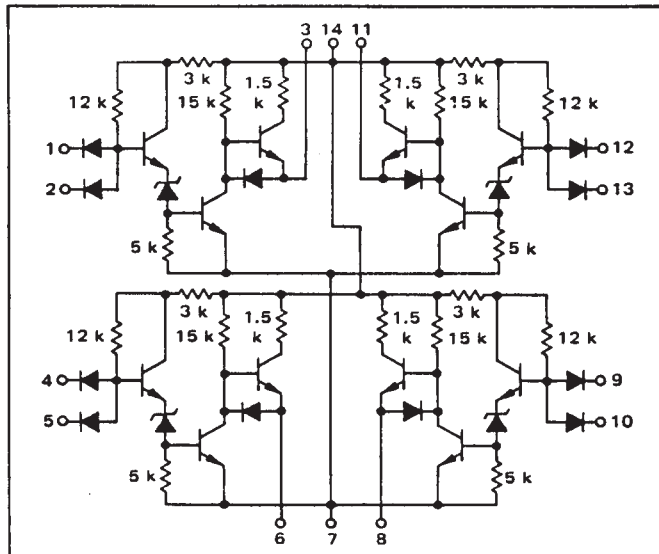


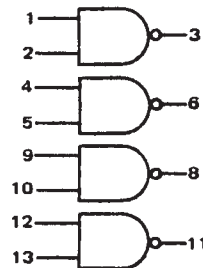
ML672

Quad 2-Input "Nand" Gate

Legacy Device: Motorola MC672



This device consists of four 2-input NAND gates with active output pullup.



Positive Logic: $3 = 1 \cdot 2$

Input Loading Factor = 1

Output Loading Factor = 10

Propagation Delay Time = 110 ns typ

Typical Total Power Dissipation

Inputs High = 176 mW typ/pkg

Input Low = 52 mW typ/pkg

ELECTRICAL CHARACTERISTICS

Test procedures shown are for one gate only. The other gates are tested in the same manner.

Characteristic	Symbol	Pin Under Test	672 Test Limits							TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:											Gnd
			-30°C		+25°C		+75°C		Unit	I _{OL}	I _{OH}	V _{IL}	V _{IH}	V _F	V _R	V _{CEX}	V _{CC}	V _{CCL}	V _{CCH}		
			Min	Max	Min	Max	Min	Max													
Output Voltage	V _{OL}	3	-	1.5	-	1.5	-	1.5	Vdc	3	-	-	1.2	-	-	-	-	14	-	7	
	V _{OH}	3	-	-	12.5	-	12.5	-	Vdc	-	3	1	-	-	-	-	2	14	-	7	
		3	-	-	12.5	-	12.5	-	Vdc	-	3	2	-	-	-	-	1	14	-	7	
Short-Circuit Current	I _{SC}	3	-	-	-6.5	-15.0	-6.5	-15.0	mAdc	-	-	-	-	-	-	-	-	-	14	1.3, 7	
Reverse Current	I _R	1	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	1	-	-	14	-	2.7	
		2	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	2	-	-	14	-	1.7	
Output Leakage Current	I _{CEX}	3	-	-	-	100	-	100	μAdc	-	-	-	-	-	-	3.14	-	-	-	1.7	
Forward Current	I _F	1	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	1	2	-	-	-	14	7	
		2	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	2	1	-	-	-	14	7	
Power Drain Current (Total Device)	I _{CCL}	14	-	-	-	6.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	1, 2, 4, 5, 7, 9, 10, 12, 13	
	I _{CCH}	14	-	-	-	20	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	7	
Switching Times										Pulse In	Pulse Out										
	t ₁₋₃₊	3	-	-	-	200	-	-	ns	1	3	-	-	-	-	-	14	-	-	7	
	t ₁₋₃₋	3	-	-	-	100	-	-	ns	1	3	-	-	-	-	-	14	-	-	7	

Pins not listed are left open.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

