

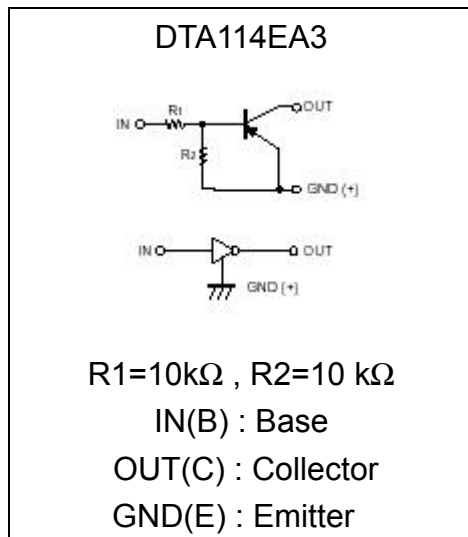
PNP Digital Transistors (Built-in Resistors)

DTA114EA3

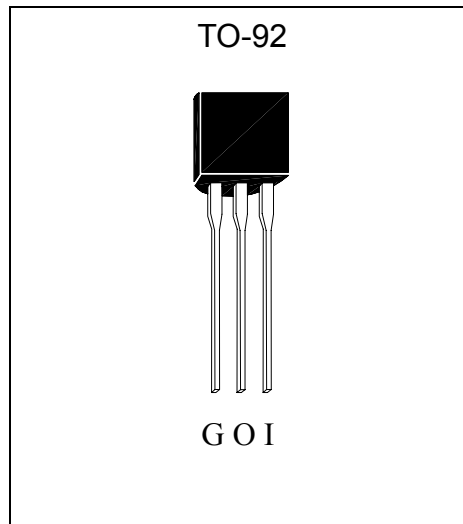
Features

- Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
- The bias resistors consist of thin-film resistors with complete isolation to allow positive biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
- Only the on/off conditions need to be set for operation, making device design easy.
- Complements the DTC114EA3

Equivalent Circuit



Outline



Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{CC}	-50	V
Input Voltage	V_{IN}	-40~+10	V
Output Current	I_O	-50	mA
	$I_{O(max)}$	-100	mA
Power Dissipation	P_d	400	mW
Junction Temperature	T_j	150	°C
Storage Temperature	T_{stg}	-55~+150	°C

**Electrical Characteristics (Ta=25°C)**

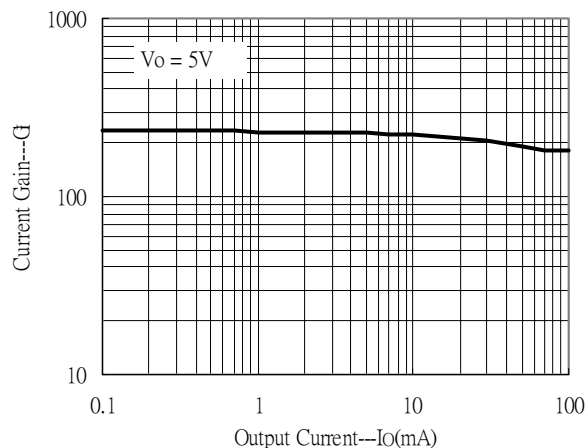
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Voltage	$V_{I(off)}$	-	-	-0.5	V	$V_{CC}=-5V, I_o=-100\mu A$
	$V_{I(on)}$	-3	-	-	V	$V_o=-0.3V, I_o=-10mA$
Output Voltage	$V_{O(on)}$	-	-	-0.3	V	$I_o/I_i=-10mA/-0.5mA$
Input Current	I_i	-	-	-0.88	mA	$V_i=-5V$
Output Current	$I_{O(off)}$	-	-	-0.5	μA	$V_{CC}=-50V, V_i=0V$
DC Current Gain	G_i	30	-	-	-	$V_o=-5V, I_o=-5mA$
Input Resistance	R_i	7	10	13	k Ω	-
Resistance Ratio	R_2/R_1	0.8	1	1.2	-	-
Transition Frequency	f_T	-	250	-	MHz	$V_{CE}=-10V, I_c=-5mA, f=100MHz$ *

* Transition frequency of the device

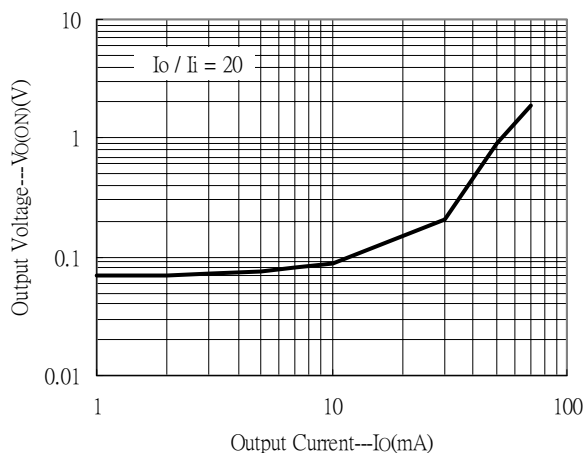


Characteristic Curves

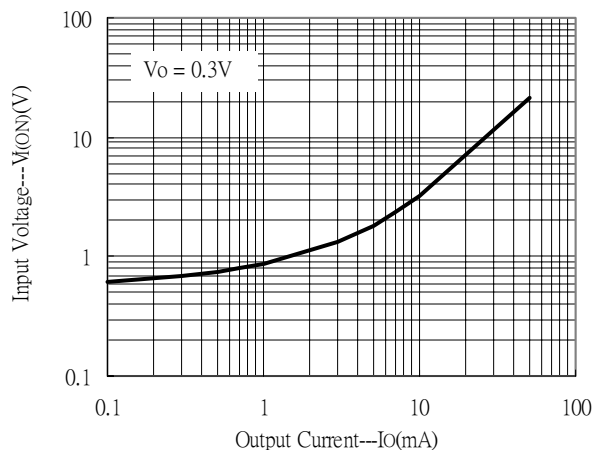
Current Gain vs Output Current



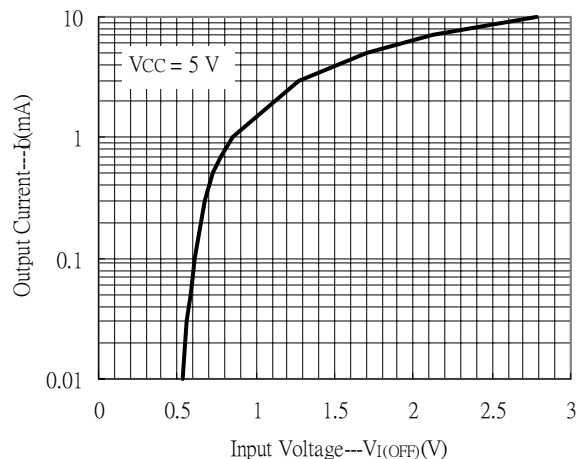
Output Voltage vs Output Current



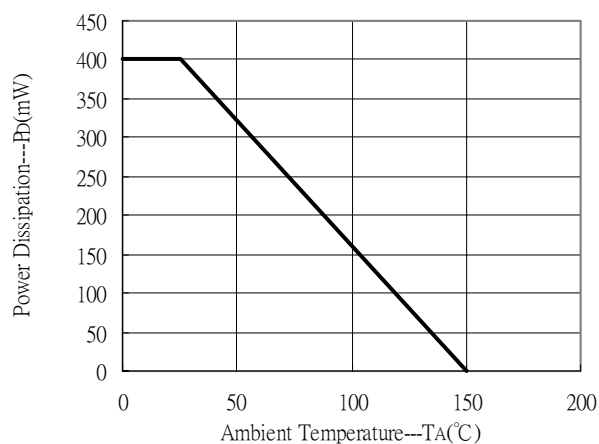
Input Voltage vs Output Current(ON characteristics)



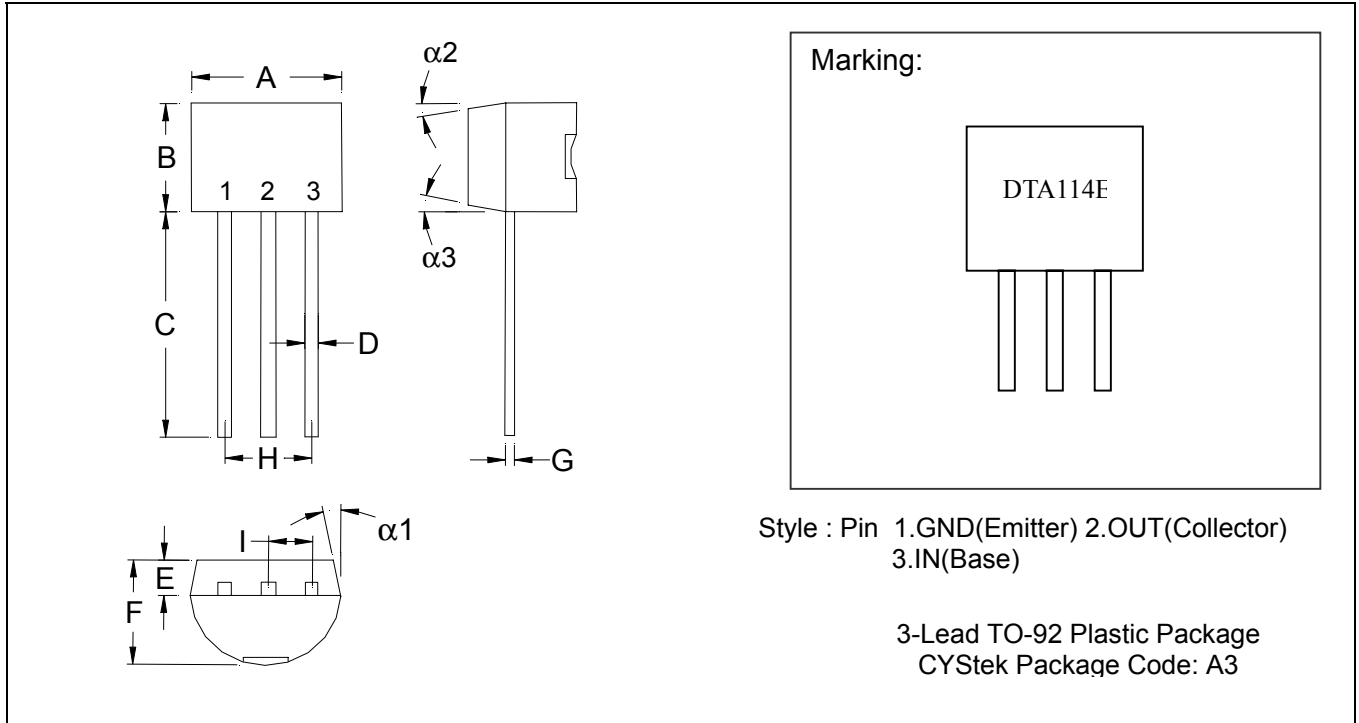
Output Current vs Input Voltage(OFF characteristics)



Power Derating Curve



TO-92 Dimension



*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1704	0.1902	4.33	4.83	G	0.0142	0.0220	0.36	0.56
B	0.1704	0.1902	4.33	4.83	H	-	*0.1000	-	*2.54
C	0.5000	-	12.70	-	I	-	*0.0500	-	*1.27
D	0.0142	0.0220	0.36	0.56	$\alpha 1$	-	*5°	-	*5°
E	-	*0.0500	-	*1.27	$\alpha 2$	-	*2°	-	*2°
F	0.1323	0.1480	3.36	3.76	$\alpha 3$	-	*2°	-	*2°

Notes: 1.Controlling dimension: millimeters.

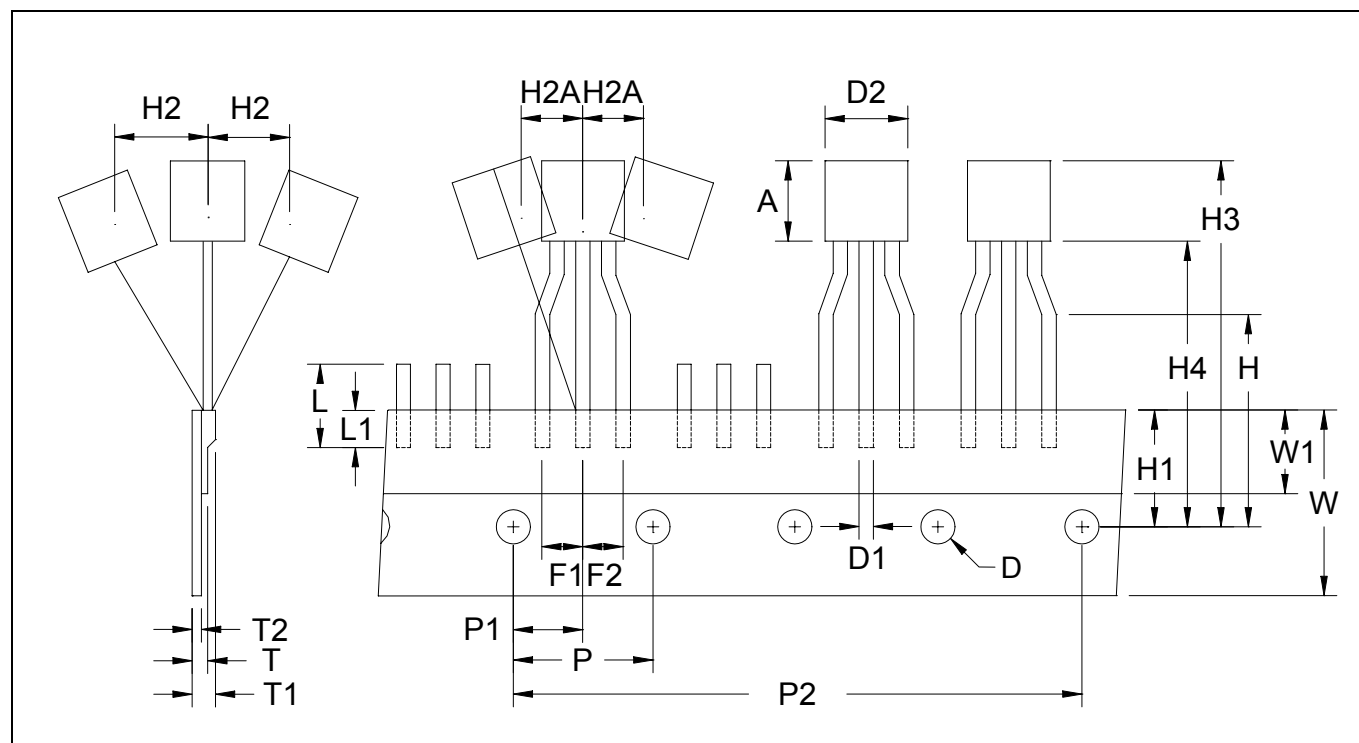
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.

3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: 42 Alloy ; solder plating
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

TO-92 Taping Outline



DIM	Item	Millimeters	
		Min.	Max.
A	Component body height	4.33	4.83
D	Tape Feed Diameter	3.80	4.20
D1	Lead Diameter	0.36	0.53
D2	Component Body Diameter	4.33	4.83
F1,F2	Component Lead Pitch	2.40	2.90
F1,F2	F1-F2	-	±0.3
H	Height Of Seating Plane	15.50	16.50
H1	Feed Hole Location	8.50	9.50
H2	Front To Rear Deflection	-	1
H2A	Deflection Left Or Right	-	1
H3	Component Height	-	27
H4	Feed Hole To Bottom Of Component	-	21
L	Lead Length After Component Removal	-	11
L1	Lead Wire Enclosure	2.50	-
P	Feed Hole Pitch	12.50	12.90
P1	Center Of Seating Plane Location	5.95	6.75
P2	4 Feed Hole Pitch	50.30	51.30
T	Over All Tape Thickness	-	0.55
T1	Total Taped Package Thickness	-	1.42
T2	Carrier Tape Thickness	0.36	0.68
W	Tape Width	17.50	19.00
W1	Adhesive Tape Width	5.00	7.00
-	20 pcs Pitch	253	255

**Important Notice:**

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.