MOTOROLA

MCM14552

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

256-BIT (64 x 4) STATIC RANDOM ACCESS MEMORY

256-BIT STATIC RANDOM ACCESS MEMORY

The MCM14552 is a static random access memory (RAM) organized in a 64 x 4 bit pattern. The three chip enable inputs can be used as extensions of the six address inputs, creating 9-bit address scheme. Eight MCM14552 devices may be used to comprise a 2048-bit memory (512 x 4) without additional address decoding.

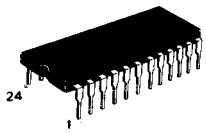
The mode control (M) is used to change the control logic characteristic of the circuit. For example, with M high, the 3-state input (T) fully controls the 3-state characteristic of the output. With M low, the output 3-state characteristic is controlled by chip enable inputs (CE), write enable input (WE) and T.

The memory is designed so that dc signals may operate the memory, with no maximum pulse width restrictions.

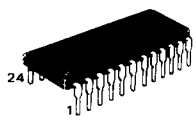
Medium speed, micropower operation, and control flexibility make the device useful in scratch pad or buffer applications where battery operation or high noise immunity are required.

- Quiescent Current = 50 μA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- 3-state Output Capability for Memory Expansion
- Output Data Latch Eliminates Need for Storage Buffer
- Access Time = 700 ns typical @ V_{DD} = 10 Vdc
- Fully Decoded and Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

NOTE: Pin 20(LE)) must be connected to V_{SS}



L SUFFIX
CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

MCM14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

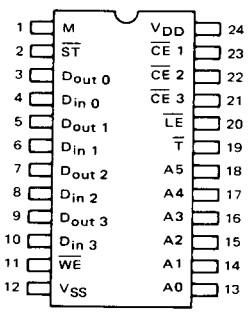
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}.

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±1.0	–	±0.00001	±1.0	–	±14.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.050	5.0	–	150	µAdc
		10	–	10	–	0.100	10	–	300	
		15	–	20	–	0.150	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	50	–	0.050	50	–	375	µAdc
		10	–	100	–	0.100	100	–	750	
		15	–	200	–	0.150	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.98 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.96 µA/kHz) f + I_{DD}							
		15	I_T = (5.86 µA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Figure	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	1	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns			5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 25 ns			10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns			15	–	65	130	
Output Fall Time	1	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns			5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns			10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns			15	–	40	80	
Read Cycle Time	1, 2	$t_{cyc(R)}$	5.0	–	2000	6000	ns
			10	–	750	2200	
			15	–	500	1650	
Write Cycle Time	3, 4	$t_{cyc(W)}$	5.0	–	1200	3600	ns
			10	–	750	2200	
			15	–	500	1650	
Address to $\overline{\text{Strobe}}$ Setup Time	1, 3	$t_{su(A\text{-}\overline{ST})}$	5.0	1500	500	–	ns
			10	450	150	–	
			15	350	120	–	
$\overline{\text{Strobe}}$ to Address Hold Time	1, 3	$t_{h(\overline{ST}\text{-}A)}$	5.0	150	50	–	ns
			10	100	0	–	
			15	75	0	–	
Address to $\overline{\text{Chip Enable}}$ Serup Time	2, 4	$t_{su(A\text{-}\overline{CE})}$	5.0	1800	600	–	ns
			10	600	200	–	
			15	450	150	–	
$\overline{\text{Chip Enable}}$ to Address Hold Time	2, 4	$t_{h(\overline{CE}\text{-}A)}$	5.0	450	150	–	ns
			10	300	100	–	
			15	225	75	–	
$\overline{\text{Strobe}}$ or $\overline{\text{Chip Enable}}$ Pulse Width When Reading	1, 2	$t_{WL(R)}$	5.0	1800	450	–	ns
			10	450	150	–	
			15	350	100	–	
$\overline{\text{Strobe}}$ or $\overline{\text{Chip Enable}}$ Pulse Width When Writing	3, 4	$t_{WL(W)}$	5.0	3600	1200	–	ns
			10	1800	600	–	
			15	1350	400	–	
Read Setup Time	1	$t_{su(R)}$	5.0	0	-100	–	ns
			10	0	-40	–	
			15	0	-30	–	
Read Hold Time	1	$t_{h(R)}$	5.0	540	180	–	ns
			10	240	60	–	
			15	180	45	–	
Data Setup Time	3, 4	$t_{su(D)}$	5.0	1800	600	–	ns
			10	600	200	–	
			15	450	150	–	
Data Hold Time	3, 4	$t_{h(D)}$	5.0	600	200	–	ns
			10	150	50	–	
			15	120	30	–	

*The formula given is for the typical characteristics only.

(continued)

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SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C) (continued)

Characteristic	Figure	Symbol	V_{DD}	Min	Typ	Max	Unit
Write Enable Setup Time	3, 4	$t_{su}(\overline{WE})$	5.0	720	240	–	ns
			10	240	80	–	
			15	180	55	–	
Write Enable Hold Time	3, 4	$t_{h}(\overline{WE})$	5.0	150	50	–	ns
			10	60	20	–	
			15	45	15	–	
Read Access Time from Strobe	1, 3	$t_{acc}(R\text{-}\overline{ST})$	5.0	–	2000	6000	ns
			10	–	700	2100	
			15	–	350	1600	
Read Access Time from Chip Enable	2	$t_{acc}(R\text{-}\overline{CE})$	5.0	–	2100	6300	ns
			10	–	750	2250	
			15	–	400	1700	
Output Enable/Disable Delay from Chip Enable or Write Enable	2, 4	$t_{R(\overline{CE})}$, $t_{R(\overline{WE})}$	5.0	–	400	1200	ns
			10	–	200	600	
			15	–	150	450	
Three-State Enable/Disable Output Delay	2	$t(\overline{T})$	5.0	–	400	1200	ns
			10	–	160	480	
			15	–	120	360	
Latch to Output Propagation Delay	1	$t_{\overline{LE}}$	5.0	–	500	1500	ns
			10	–	200	600	
			15	–	150	450	

*The formula given is for the typical characteristics only.

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LOGIC DIAGRAM

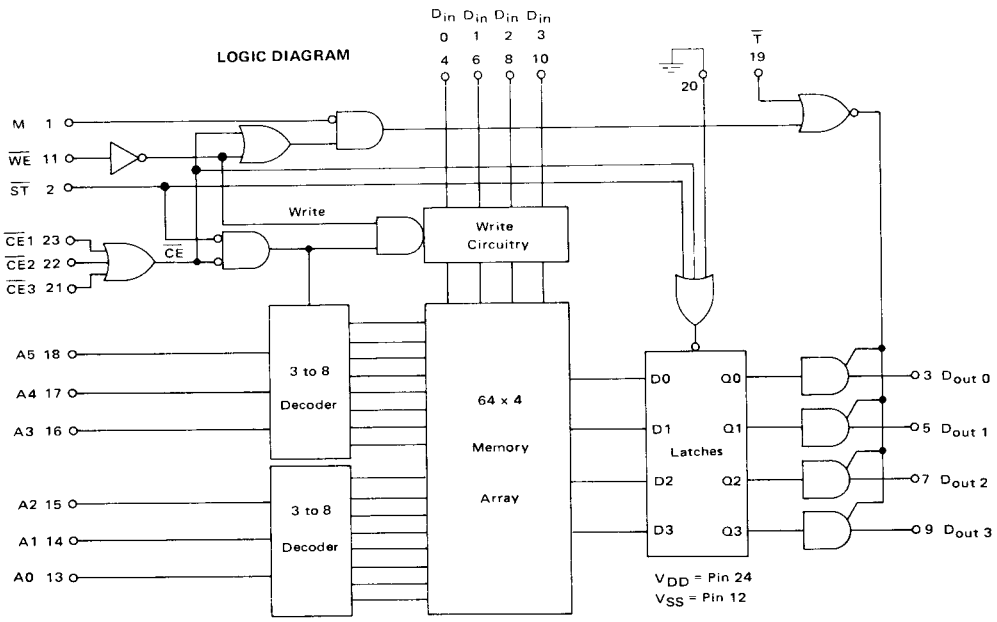
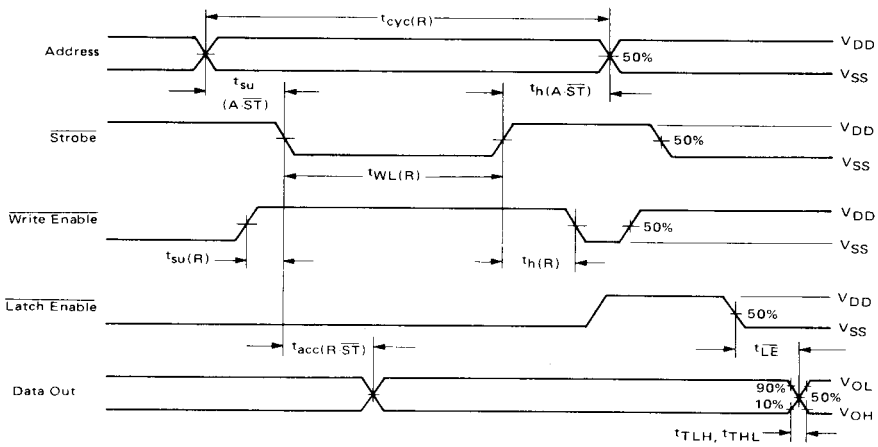
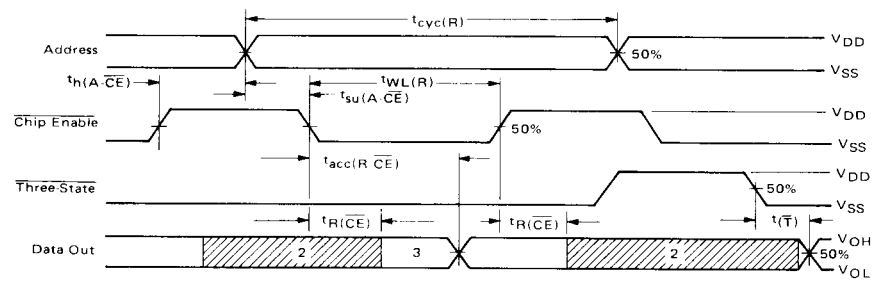


FIGURE 1 – READ CYCLE WAVEFORMS UTILIZING STROBE TO ACCESS MEMORY



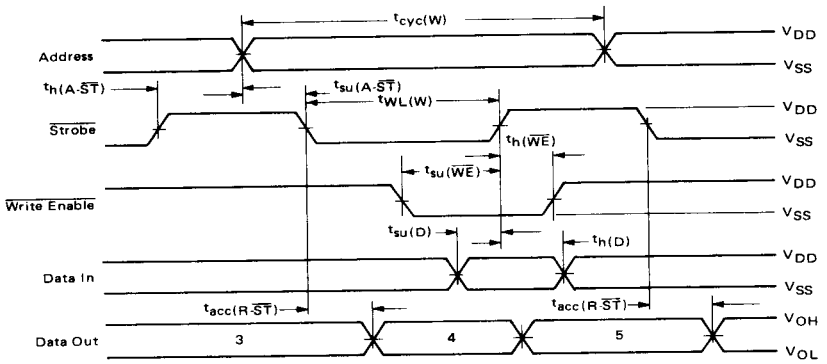
Notes: 1 $\overline{CE}1$, $\overline{CE}2$, $\overline{CE}3$ and $\overline{T}$ are low, M is high.
2 $\overline{WE}$ may be held high during the complete read cycle.

FIGURE 2 – READ CYCLE WAVEFORMS UTILIZING CHIP ENABLE TO ACCESS MEMORY



Notes: 1 – Unused $\overline{CE}$, $\overline{ST}$, M and $\overline{T}$ are low and $\overline{WE}$ is high.
2 – High impedance output state occurs when any $\overline{CE}$ is high and M is low, or when $\overline{T}$ is high.
3 – The output displays data from the previous state.
4 – $t_{WL(R)} \geq t_{acc(R\,\overline{CE})max}$.

FIGURE 3 – WRITE CYCLE WAVEFORMS UTILIZING STROBE



Notes:
1 – $\overline{CE}1$, $\overline{CE}2$, $\overline{CE}3$ and $\overline{T}$ are maintained at the logical "0" level.
2 – M is maintained at the logical "1" level.
3 – The output displays the contents of the previous state.
4 – The output displays the contents of the presently addressed location as in a read modify write cycle.
5 – The output displays the data that was written into addressed location.

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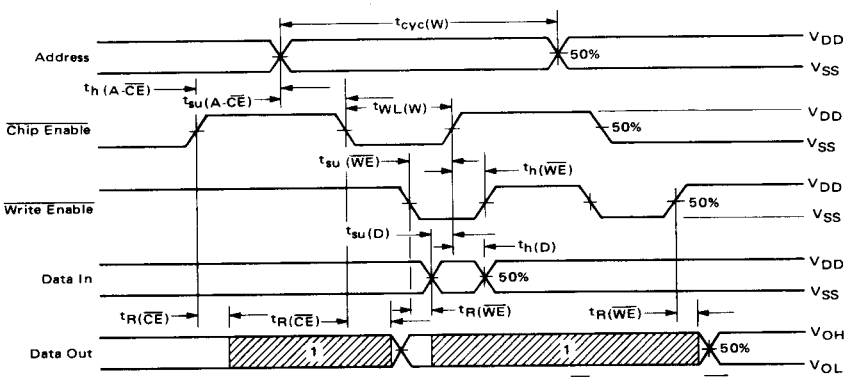
FIGURE 4 – WRITE CYCLE WAVEFORM UTILIZING CHIP ENABLE



Notes:
1 – High impedance output state occurs when $\overline{CE}$ is high or when $\overline{WE}$ is low, for M and $\overline{T}$ maintained in the low state.
2 – Unused $\overline{CE}$'s, $\overline{ST}$, M and $\overline{T}$ are maintained at the logical "0" level.

TRUTH TABLE

Function	$\overline{CE}$ 1	$\overline{CE}$ 2	$\overline{CE}$ 3	$\overline{T}$	$\overline{LE}$	M	$\overline{ST}$	$\overline{WE}$	D_{in}	D_{out}	Comments
Address Changing Valid	X	X	X	X	X	X	1	X	X	R/A	D_{out} will be active if all $\overline{CE}$ = 0, $\overline{T}$ = 0 and $\overline{WE}$ = 1 or if M = 1 and $\overline{T}$ = 0
	X	X	1	X	X	X	X	X	X	R/A	
	X	1	X	X	X	X	X	X	X	R/A	
	1	X	X	X	X	X	X	X	X	R/A	
Address Changing Not Valid	0	0	0	X	X	X	0	X	X	R/A	D_{out} will be active if $\overline{T}$ = 0 and $\overline{WE}$ = 1 or if M = 1 and $\overline{T}$ = 0
D_{out} Disabled (in high resistance state)	X	X	1	X	X	0	X	X	X	R	Disables write circuitry
	X	1	X	X	X	0	X	X	X	R	
	1	X	X	X	X	0	X	X	X	R	
	X	X	X	1	X	X	X	X	X	R	$\overline{T}$ = 1 always disables D_{out}
	X	X	X	X	X	0	X	0	X	R	M = 0 and write operation disables D_{out}
D_{out} Enabled (in active state)	0	0	0	0	X	X	X	1	X	A	Read operation, D_{out} active
	X	X	X	0	X	1	X	X	X	A	Read or write, D_{out} active
Read Addressed Memory Location Into Output Latch	0	0	0	X	0	X	0	X	X	R/A	If $\overline{WE}$ = 0, D_{in} = D_{out}
Disable Reading From Memory	X	X	1	X	X	X	X	X	X	R/A	
	X	1	X	X	X	X	X	X	X	R/A	
	1	X	X	X	X	X	X	X	X	R/A	
	X	X	X	X	X	X	1	X	X	R/A	
	X	X	X	X	X	X	X	0	X	R/A	
Write Into Memory	0	0	0	X	X	X	0	0	A	R/A	
Write Disabled	X	X	1	X	X	X	X	X	X	R/A	
	X	1	X	X	X	X	X	X	X	R/A	
	1	X	X	X	X	X	X	X	X	R/A	
	X	X	X	X	X	X	1	X	X	R/A	
	X	X	X	X	X	X	X	1	X	R/A	
Output Latch Enabled	0	0	0	X	0	X	0	X	X	R/A	
Output Latch Disabled	X	X	1	X	X	X	X	X	X	R/A	
	X	1	X	X	X	X	X	X	X	R/A	
	1	X	X	X	X	X	X	X	X	R/A	
	X	X	X	X	1	X	X	X	X	R/A	
	X	X	X	X	X	X	1	X	X	R/A	

R = High resistance state at D_{out}.
A = An active level of either V_{DD} or V_{SS}
R/A = An R or A condition depending on the don't care condition
X = Don't care condition (must be in the "1" or "0" state)
1 = A high level at V_{DD}
0 = A low level at V_{SS}

FIGURE 5 – 512 WORD x 16 BIT MEMORY BOARD