FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27708-2E

ASSP for Power Supply Application (for secondary battery)

DC/DC Converter IC for Parallel Charging of 3/4 cell Li-ion & NiMH Batteries

MB3879

■ DESCRIPTION

The MB3879 is a DC/DC converter IC for parallel charging of 3/4 cell Li-ion & NiMH batteries, which uses the pulse-width modulation (PWM) for controlling output voltages and output currents independently.
This IC can dynamically control secondary batterie's charge current, which detects voltage dropping in an AC adapter in order to keep its power constant (Dynamically controlled charging). This operation allows quick charging by variable charging current in accordance with operating status of a notebook PC.
Moreover, the total current of the system current and control IC input current are detected, and control of the secondary battery is enabled.
An efficient charge becomes possible because of the charge current comes in changeability according to the operation state of notebook PC by this operation.
The IC also allows parallel charging that charges two batteries simultaneously, reducing charging time dramatically.
The IC, using a built-in output voltage setting resistor, allows high-precision setting of output voltages. With its output-voltage switching function that is ready for both graphite-type and coke-type Li-ion batteries as well as NiMH battery, the IC is best suited to a built-in charger of a notebook PC.
This product is covered by US Patent Number 6,147,477.

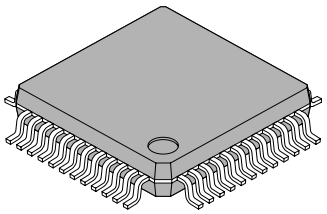
■ FEATURES

- Detecting a voltage dropping in the AC adapter, and dynamically controlling the charge current (Dynamically-controlled charging)
- Detecting total current of system current and control-IC input current (Differential-charging)

(Continued)

■ PACKAGE

48-pin plastic LQFP



(FPT-48P-M05)

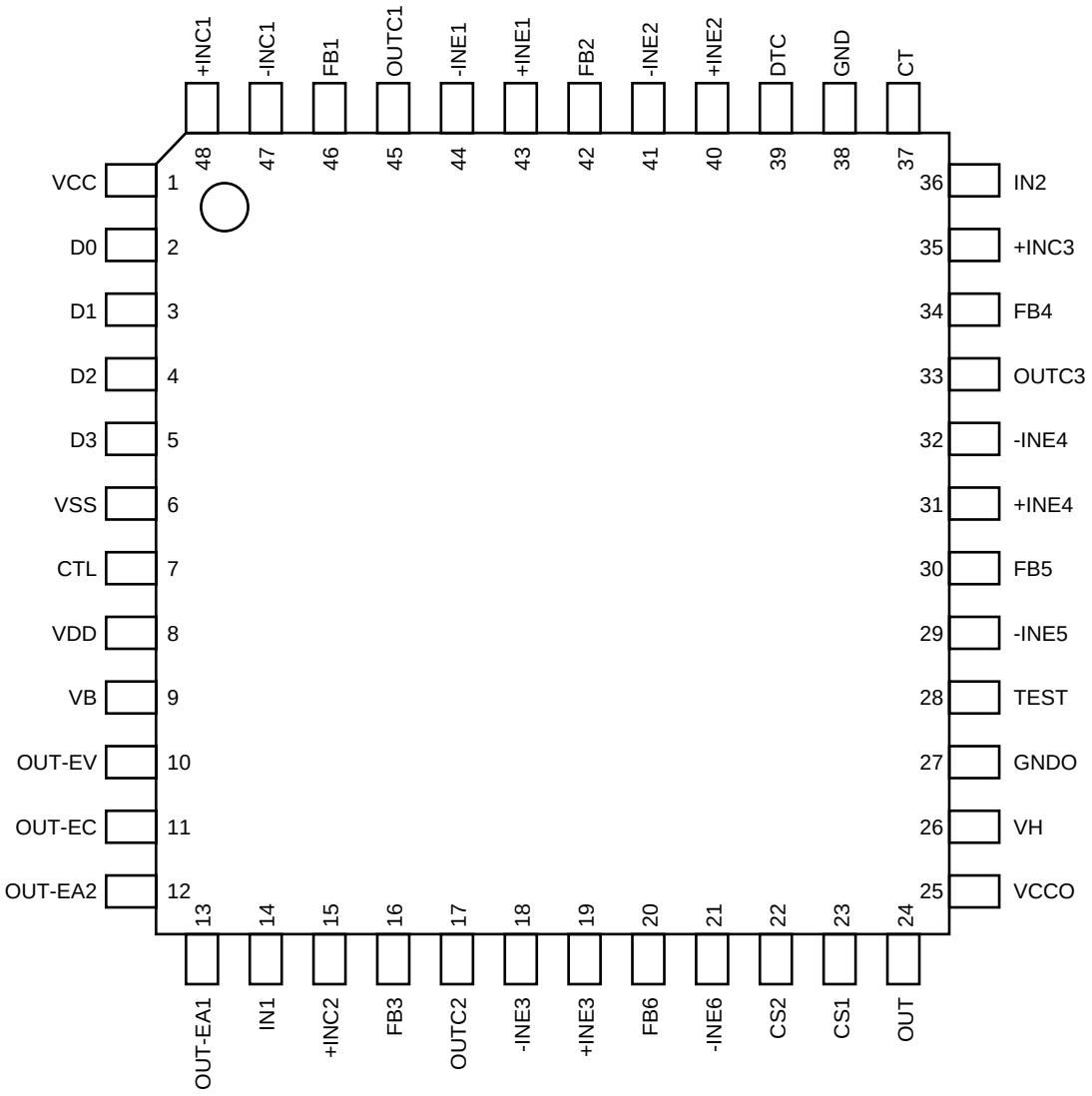
FUJITSU

(Continued)

- Selection of output voltages by 4-bit decoder:
  12.3V (3 cells: 4.1V), 12.6V (3 cells: 4.2V), 16.4V (4 cells: 4.1V), 16.8V (4 cells: 4.2V)
- High efficiency: 94% (using reverse current preventive diode)
- Wide range of power supply voltage: 8 V to 25 V
- Setting precision of output voltage (built-in output voltage setting resistor): ± 0.8% (Ta = +25 °C)
- Setting precision of charge current: ±5%
- Setting of frequency for only external capacitor, using built-in frequency setting resistor.
- Oscillation frequency range: 100 kHz to 500 kHz
- Built-in current detect amplifier with wide range of in-phase input voltages: 0 V to Vcc
- Stand-by current: 0 μA
- Built-in load-independent soft-start circuit
- Built-in charge mode detection function
- Built-in totem-pole outputs supporting Pch MOS FET

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-48P- 05)

■ PIN DESCRIPTION

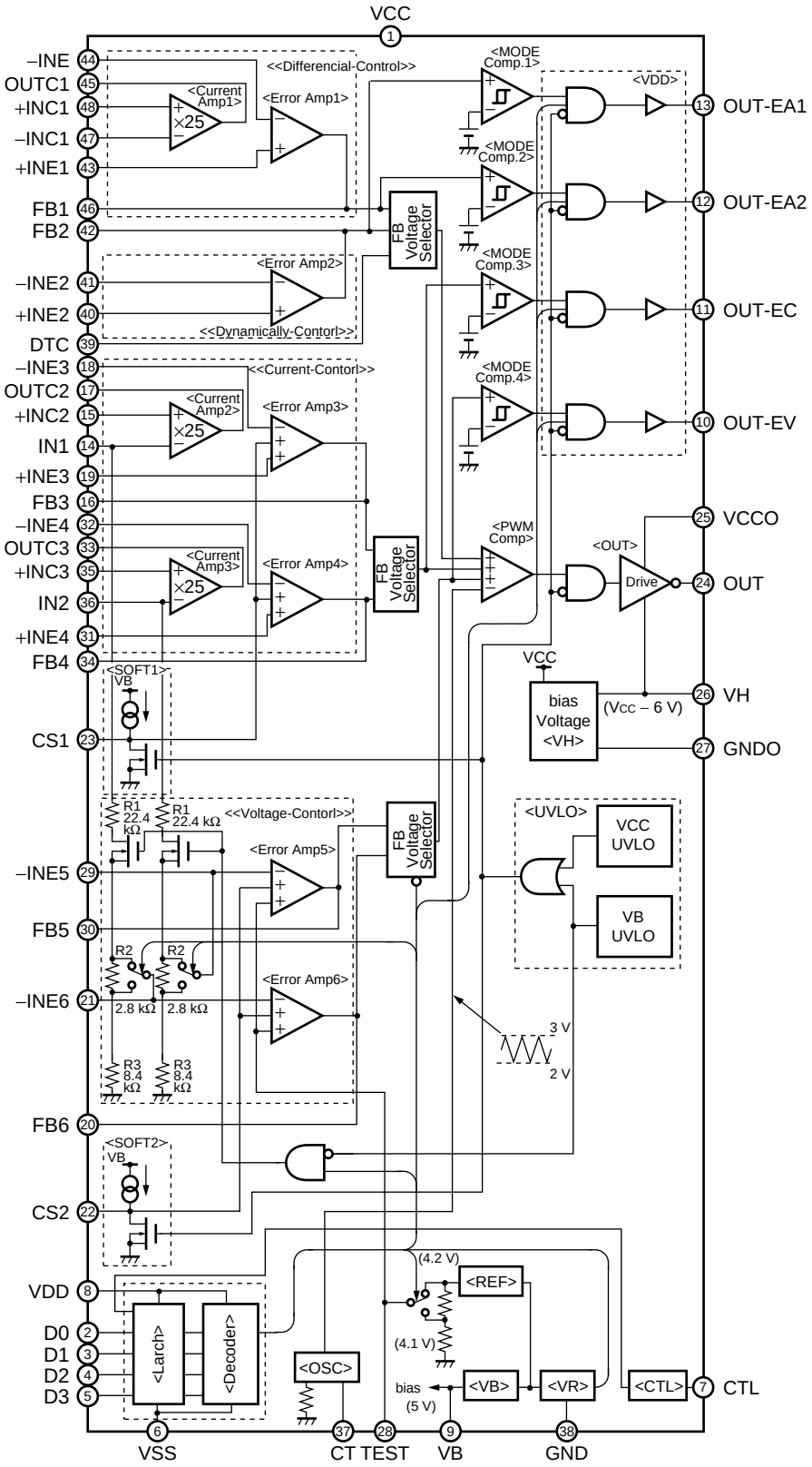
Pin No.	Symbol	I/O	Descriptions
1	VCC	—	Power supply terminal
2	D0	I	VDD logic input terminal
3	D1	I	VDD logic input terminal
4	D2	I	VDD logic input terminal
5	D3	I	VDD logic input terminal
6	VSS	—	VDD logic ground terminal
7	CTL	I	Power supply control terminal. Setting “L” level on CTL terminal places the IC in standby mode.
8	VDD	—	VDD logic power supply terminal
9	VB	O	Reference voltage output terminal
10	OUT-EV	O	Constant-voltage charging distinction signal output terminal H level: Dynamically-controlled charging, Differential charging, or Constant-voltage charging mode L level: BATT1 or BATT2 Constant-voltage charging mode
11	OUT-EC	O	Constant-current charge distinction signal output terminal H level: Dynamically-controlled charging, Differential charging, or Constant-voltage charging mode L level: BATT1 or BATT2 Constant-current charging mode
12	OUT-EA2	O	Differential-charging distinction signal output terminal H level: Dynamically-controlled-charging, Constant-voltaging, or Constant-current charging mode L level: Differential-charging mode
13	OUT-EA1	O	Dynamically-controlled charging distinction signal output terminal H level: Dynamically-controlled charging, Constant-voltage charging, or Constant-current charging mode L level: Dynamically-controlled charging mode
14	IN1	I	<BATT1> Current detection amplifier (Current Amp2) input terminal Output voltage feedback input terminal
15	+INC2	I	<BATT1> Current detection amplifier (Current Amp2) input terminal
16	FB3	O	<BATT1> Error amplifier (Error Amp3) output terminal
17	OUTC2	O	<BATT1> Current detection amplifier (Current Amp2) output terminal
18	–INE3	I	<BATT1> Error amplifier (Error Amp3) inverted input terminal
19	+INE3	I	<BATT1> Error amplifier (Error Amp3) non-inverted input terminal
20	FB6	O	<BATT1> Error amplifier (Error Amp6) output terminal
21	–INE6	I	<BATT1> Error amplifier (Error Amp6) inverted input terminal
22	CS2	—	Soft-start capacitor connection terminal
23	CS1	—	Soft-start capacitor connection terminal
24	OUT	O	External FET gate driving terminal
25	VCCO	—	Driver block power supply terminal

(Continued)

(Continued)

Pin No.	Symbol	I/O	Descriptions
26	VH	O	FET driver circuit power supply terminal (VH = VCC–6V)
27	GND0	—	Ground terminal
28	TEST	O	Internal reference voltage for setting charge voltage
29	–INE5	I	<BATT2> Error amplifier (Error Amp5) inverted input terminal
30	FB5	O	<BATT2> Error amplifier (Error Amp5) output terminal
31	+INE4	I	<BATT2> Error amplifier (Error Amp4) non-inverted input terminal
32	–INE4	I	<BATT2> Error amplifier (Error Amp4) inverted input terminal
33	OUTC3	O	<BATT2> Current detection amplifier (Current Amp3) output terminal
34	FB4	O	<BATT2> Error amplifier (Error Amp4) output terminal
35	+INC3	I	<BATT2> Current detection amplifier (Current Amp3) input terminal
36	IN2	I	<BATT2> Current detection amplifier (Current Amp3) input terminal Output voltage feedback input terminal
37	CT	—	Triangular wave oscillation frequency setting capacitor connection terminal
38	GND	—	Ground terminal
39	DTC	I	External duty control input terminal
40	+INE2	I	Error amplifier (Error Amp2) non-inverted input terminal
41	–INE2	I	Error amplifier (Error Amp2) inverted input terminal
42	FB2	O	Error amplifier (Error Amp2) output terminal
43	+INE1	I	Error amplifier (Error Amp1) non-inverted input terminal
44	–INE1	I	Error amplifier (Error Amp1) inverted input terminal
45	OUTC1	O	Current detection amplifier (Current Amp2) output terminal
46	FB1	O	Error amplifier (Error Amp1) output terminal
47	–INC1	I	Current detection amplifier (Current Amp1) input terminal
48	+INC1	I	Current detection amplifier (Current Amp1) input terminal

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating		Unit
			Min	Max	
Power supply voltage	V_{CC}	VCC and VCCO terminal	—	28	V
	V_{DD}	—	—	17	V
Output current	I_O	OUT terminal	—	60	mA
Peak output current	I_{OP}	OUT terminal Duty ≤ 5% (t = 1/fosc×Duty)	—	700	mA
Power dissipation	P_D	Ta ≤ + 25 °C	—	860*	mW
Storage temperature	Tstg	—	–55	+ 125	°C

* : The package is mounted on the dual-sided epoxy board (10 cm×10 cm) .

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{CC}	VCC and VCCO terminals	8	19	25	V
	V_{DD}	—	2.7	5	7	V
Reference voltage output current	I_B	VB terminal	–1	—	0	mA
VH terminal output current	I_H	VH terminal	0	—	30	mA
Input voltage	V_{INE}	–INE1 to –INE6, +INE1 to +INE4 terminal	0	—	V_{CC}–1.8	V
	V_{INC}	+INC1 to +INC3, –INC1 terminal	0	—	V_{CC}	V
	V_{INC}	IN1 and IN2 terminals	0	—	V_{CC}	V
	V_{DTC}	DTC terminal	0	—	V_{CC}–0.9	V
Output current	I_O	OUT terminal	–45	—	+45	mA
Peak output current	I_{OP}	Duty ≤ 5% (t = 1/fosc×Duty) OUT terminal	–600	—	+600	mA
CTL terminal input voltage	V_{CTL}	CTL terminal	0	—	25	V
Decoder block input voltage	V_{DEC}	D0 to D3 terminals	0	—	V_{DD}	V
Oscillation frequency	f_{OSC}	—	100	300	500	kHz
Timing capacitor	C_T	—	47	100	330	pF
Soft-start capacitor	C_S	—	—	0.022	1.0	µF
VH terminal capacitor	C_H	—	—	0.1	1.0	µF
Reference voltage output capacitor	C_{REF}	—	—	0.1	1.0	µF
Operating ambient temperature	Ta	—	–30	+25	+85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRIC CHARACTERISTICS

(VCC = VCCO = 19 V, VDD = 5 V, Charge mode = Li4C42, Ta = +25 °C)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
1.Reference voltage block [REF]	Output voltage	V_{TEST1}	28	Charge mode = Li4C42, Ta = +25 °C	4.167	4.200	4.233	V
		V_{TEST2}	28	Charge mode = Li4C42, Ta = –30 °C to +85 °C	4.158	4.200	4.242	V
		V_{TEST3}	28	Charge mode = Li4C41, Ta = +25 °C	4.063	4.100	4.137	V
		V_{TEST4}	28	Charge mode = Li4C42, Ta = –30 °C to +85 °C	4.050	4.100	4.150	V
2.Control circuit bias voltage block [VB]	Output voltage	V_{B1}	9	Ta = +25 °C	4.95	5.00	5.05	V
		V_{B2}	9	Ta = –30 °C to +85 °C	4.94	5.00	5.06	V
	Input stability	Line	9	VCC = VCCO = 8 V to 25 V	—	3	10	mV
	Load stability	Load	9	VB = 0 mA to –1 mA	—	1	10	mV
	short-circuit output current	Ios	9	VB = 1 V	–25	–15	–5	mA
3. Under voltage lockout protection circuit block [UVLO]	Threshold voltage	V_{TLH}	1	VCC = VCCO = ↗	6.0	6.2	6.4	V
		V_{THL}	1	VCC = VCCO = ↘	5.0	5.2	5.4	V
	Hysteresis width	V_H	1	—	—	1*1	—	V
	Threshold voltage	V_{TLH}	9	VB = ↗	2.5	2.7	2.9	V
		V_{THL}	9	VB = ↘	2.3	2.5	2.7	V
	Hysteresis width	V_H	9	—	—	0.2*1	—	V
4. Soft-start block [SOFT1, SOFT2]	Charge current	I_{CS}	22, 23	—	–14	–10	–6	µA
5. Triangular oscillator block [OSC]	Oscillation frequency	f_{OSC}	24	C_T = 100 pF	240	300	360	kHz
	Frequency temperature stability	Δf/fdt	24	Ta = –10 °C to +85 °C	—	5*1	—	%
	Frequency temperature stability	Δf/fdt	24	Ta = –30 °C to +85 °C	—	10*1	—	%

*1 : Standard design value

(Continued)

(VCC = VCCO = 19 V, VDD = 5 V, Charge mode = Li4C42, Ta = +25 °C)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
6. Error amplifier block [Error Amp1 to Error Amp6]	Input offset voltage	V_{IO}	18, 19, 31, 32, 40, 41, 43, 44	Error Amp1 to Error Amp4 FB1 to FB4 = 2.5 V	—	1	5	mV
	Input bias current	I_B	18, 19, 31, 32, 40, 41, 43, 44	–INE1 = +INE1 = –INE2 = +INE2 = –INE3 = +INE3 = –INE4 = +INE4 = 0 V	–100	–30	—	nA
	Common mode input voltage range	V_{CM}	16, 34, 42, 46	Error Amp1 to Error Amp2	0	—	V_{CC}–1.8	V
	Voltage gain	A_V	16, 34, 42, 46	DC	—	100*1	—	dB
	Frequency band width	BW	16, 34, 42, 46	A_V = 0 dB	—	2*1	—	MHz
	Output voltage	V_{OH}	16, 20, 30, 34, 42, 46	FB1 to FB6 = –1 mA	4.5	4.7	—	V
		V_{OL}	16, 20, 30, 34, 42, 46	FB1 to FB6 = 1 mA	—	1.0	1.2	V
	Output source current	I_{SOURCE}	16, 20, 30, 34, 42, 46	FB1 to FB6 = 2.5 V	—	–9	–4.5	mA
	Output sink current	I_{SINK}	16, 20, 30, 34, 42, 46	FB1 to FB6 = 2.5 V	4.5	9.0	—	mA
	Threshold voltage	V_{TH1}	20, 30	FB5 = FB6 = 2.5 V, Ta = +25 °C Charge mode = Li4C42, Li3C42	V_{TH}*2× 0.992	V_{TH}× 1.000	V_{TH}× 1.008	V
		V_{TH2}	20, 30	FB5 = FB6 = 2.5 V, Ta = –30 °C to +85 °C Charge mode = Li4C42, Li3C42	V_{TH}*2× 0.990	V_{TH}× 1.000	V_{TH}× 1.010	V
		V_{H3}	20, 30	FB5 = FB6 = 2.5 V, Ta = +25 °C Charge mode = Li4C41, Li3C41	V_{TH}*3× 0.991	V_{TH}× 1.000	V_{TH}× 1.009	V
		V_{TH4}	20, 30	FB5 = FB6 = 2.5 V, Ta = –30 °C to +85 °C Charge mode = Li4C41, Li3C41	V_{TH}*3× 0.989	V_{TH}× 1.000	V_{TH}× 1.011	V

*1 : Standard design value
*2 : 16.8 V (Li4C42) , 12.6 V (Li3C42)
*3 : 16.4 V (Li4C41) , 12.3 V (Li3C41)

(Continued)

(VCC = VCCO = 19 V, VDD = 5 V, Charge mode = Li4C42, Ta = +25 °C)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
6. Error amplifier block [Error Amp1 to Error Amp6]	Input current	I_{INEH1}	14, 36	IN1 = IN2 = 16.8 V Charge mode = Li4C42	—	500	750	µA
		I_{INEH2}	14, 36	IN1 = IN2 = 16.4 V Charge mode = Li4C41	—	488	730	µA
		I_{INL}	14, 36	VCC = VCCO = 0 V, IN1 = IN2 = 16.9 V	—	0	1	µA
	Input resistance	Ra	14, 36	R1+R2 IN1 = IN2 = 16.8 V Charge mode = Li4C42	17.6	25.2	32.8	kΩ
		Rb	21, 29	R3 IN1 = IN2 = 16.8 V Charge mode = Li4C42	5.9	8.4	10.9	kΩ
		Rc	14, 36	R1 IN1 = IN2 = 12.6 V Charge mode = Li3C42	15.7	22.4	29.1	kΩ
		Rd	21, 29	R2+R3 IN1 = IN2 = 12.6 V Charge mode = Li3C42	7.8	11.2	14.6	kΩ
7. Current detection amplifier block [Current Amp1 to Current Amp3]	Input current	I_{+INCH}	15, 35, 48	+INC1 to +INC3 = 3 V to V_{CC}, ΔVin = −100 mV	—	20	30	µA
		I_{-INCH}	47	+INC1 = 3 V to V_{CC}, ΔVin = −100 mV	—	0.1	0.2	µA
		I_{+INCL}	15, 35, 48	+INC1 to +INC3 = 0 V ΔVin = −100 mV	−180	−120	—	µA
		I_{-INCL}	47	+INC1 = 0 V ΔVin = −100 mV	−195	−130	—	µA
	Current detection voltage	V_{OUTC1}	17, 33, 45	+INC1 to +INC3 = 3 V to V_{CC}, ΔVin = −100 mV	2.375	2.500	2.625	V
		V_{OUTC2}	17, 33, 45	+INC1 to +INC3 = 3 V to V_{CC}, ΔVin = −20 mV	0.410	0.530	0.650	V
		V_{OUTC3}	17, 33, 45	+INC1 to +INC2 = 0 V to 3 V, ΔVin = −100 mV	2.25	2.50	2.75	V
		V_{OUTC4}	17, 33, 45	+INC1 to +INC2 = 0 V to 3 V, ΔVin = −20 mV	0.33	0.53	0.73	V

(Continued)

(Continued)

(VCC = VCCO = 19 V, VDD = 5 V, Charge mode = Li4C42, Ta = +25 °C)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
7. Current detection amplifier block [Current Amp1 to Current Amp3]	Common mode input voltage range	V_{CM}	17, 33, 45	—	0	—	Vcc	V
	Voltage gain	A_V	17, 33, 45	+INC1 to +INC3 = 3 V to V_{CC}, ΔVin = –100 mV	23.75	25.00	26.25	V/V
	Frequency band width	BW	17, 33, 45	A_V = 0 dB	—	2.0*1	—	MHz
	Output voltage	V_{OUTCH}	17, 33, 45	—	4.8	4.9	—	V
		V_{OUTCL}	17, 33, 45	—	—	20	200	mV
	Output source current	I_{SOURCE}	17, 33, 45	OUTC1 to OUTC3 = 2 V	—	–2	–1	mA
	Output sink current	I_{SINK}	17, 33, 45	OUTC1 to OUTC3 = 2 V	100	200	—	µA
8.PWM comparator block [PWM Comp.]	Threshold voltage	V_{TL}	24	Duty cycle = 0 %	1.9	2.0	—	V
		V_{TH}	24	Duty cycle = 100 %	—	3.0	3.1	V
9. DTC detection block [DTC]	Input terminal current	I_{DTC}	39	DTC = 2.5 V	–400	–200	—	nA
	Threshold voltage	V_{TL}	24	Duty cycle = 0 %	1.9	2.0	—	V
		V_{TH}	24	Duty cycle = 100 %	—	3.0	3.1	V
10. Output section [OUT]	Output source current	I_{SOURCE}	24	OUT = 14 V, Duty ≤ 5 % (t = 1 / fosc × Duty)	—	–400*1	—	mA
	Output sink current	I_{SINK}	24	OUT = 19 V, Duty ≤ 5 % (t = 1 / fosc × Duty)	—	400*1	—	mA
	Output on resistor	R_{OH}	24	OUT = –45 mA	—	6.5	9.8	Ω
		R_{OL}	24	OUT = 45 mA	—	5.0	7.5	Ω
	Rise time	tr1	24	OUT = 3300 pF (Si4435 equivalent)	—	50*1	—	ns
	Fall time	tf1	24	OUT = 3300 pF (Si4435 equivalent)	—	50*1	—	ns
11. Bias voltage block [VH]	Output voltage	V_H	26	VCC = VCCO = 8 V to 25 V, VH = 0 mA to 30 mA	V_{CC} – 6.5	V_{CC} – 6.0	V_{CC} – 5.5	V

*1 : Standard design value

(Continued)

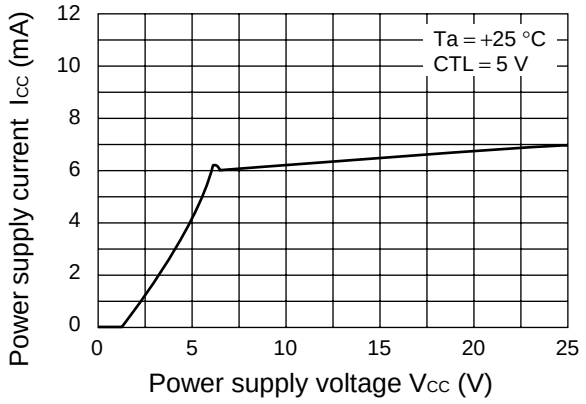
(VCC = VCCO = 19 V, VDD = 5 V, Charge mode = Li4C42, Ta = +25 °C)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
12. Control block [CTL]	CTL input voltage	V_{TH}	7	Operating status	2.0	—	25.0	V
		V_{TL}	7	Standby status	0	—	0.8	V
	Input current	I_{CTLH}	7	CTL = 5 V	—	100	150	µA
		I_{CTLL}	7	CTL = 0 V	—	0	1	µA
	Data output delay time	t_{D0}	24	CTL = "H" level→Start charging	—	—	1	ms
	CTL signal re-input time	t_{RCTL}	7	CTL = "H" level→"L" level→"H" level	2	—	—	ms
13. Decoder block [DEC]	Input voltage	V_{IL}	2, 3, 4, 5	—	0	—	V_{DD} × 0.2	V
		V_{IH}	2, 3, 4, 5	—	V_{DD} × 0.7	—	V_{DD}	V
	Input current	I_H	2, 3, 4, 5	D3 to D0 = 5 V	—	50	75	µA
		I_L	2, 3, 4, 5	D3 to D0 = 0 V	—	—	10	µA
	Data setup time	t_{DS}	2, 3, 4, 5	D3 to D0→CTL	1	—	—	ms
14. Mode detection block [MODE Comp.]	Threshold voltage	V_{TLH}	10, 11, 12, 13	FB1 to FB6 = ⌐	3.2	3.3	3.4	V
		V_{THL}	10, 11, 12, 13	FB1 to FB6 = ¬	2.9	3.0	3.1	V
	Hysteresis width	V_H	10, 11, 12, 13	—	—	0.3*1	—	V
	Output voltage	V_{OL}	10, 11, 12, 13	OUT-EA1 = OUT-EA2 = OUT-EV = OUT-EC = 2 mA	—	—	0.4	V
		V_{OH}	10, 11, 12, 13	OUT-EA1 = OUT-EA2 = OUT-EV = OUT-EC = −0.4 mA	V_{DD} − 0.4	—	—	V
15. VDD power supply	Standby current	I_{DDS}	8	CTL = 0 V	—	0	10	µA
	Power supply current	I_{DD}	8	CTL = 5 V, OUT-EV = "L" level	—	200	300	µA
16. General	Standby current	I_{CCS}	1, 25	CTL = 0 V	—	0	10	µA
	Power supply current	I_{CC}	1, 25	CTL = 5 V	—	8	12	mA

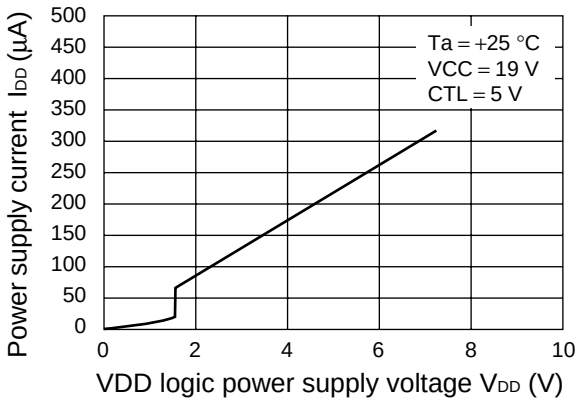
*1 : Standard design value

■ TYPICAL CHARACTERISTICS

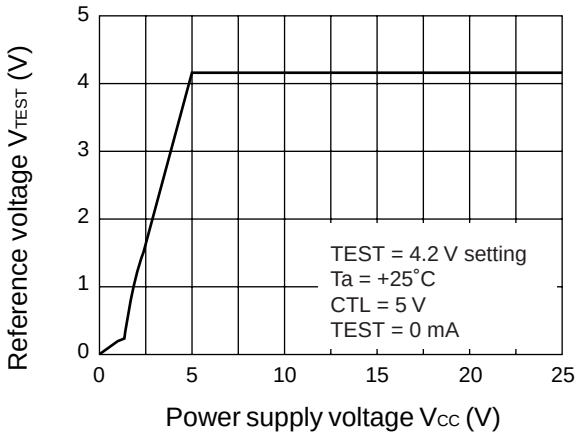
Power supply current vs. Power supply voltage



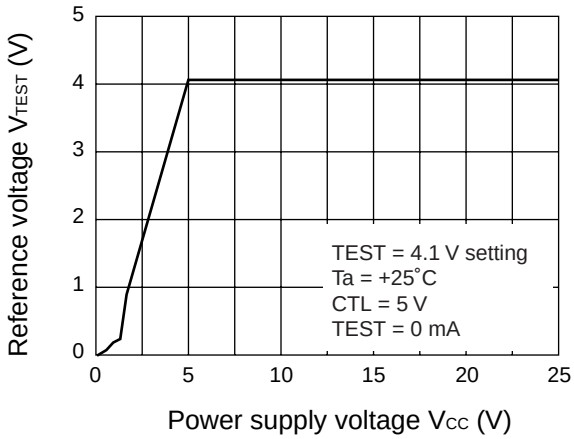
Power current vs. VDD logic block power supply voltage



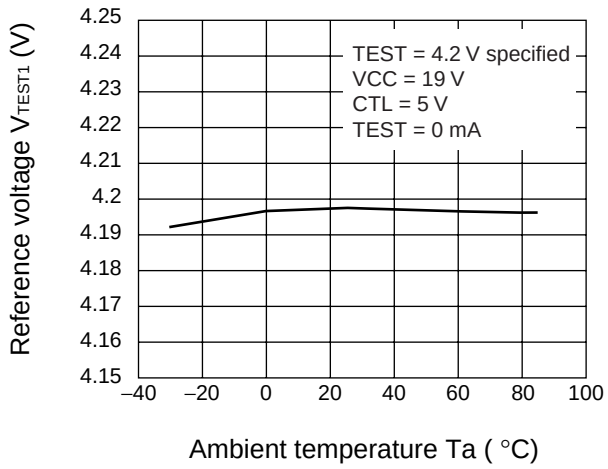
Reference voltage vs. Power supply voltage



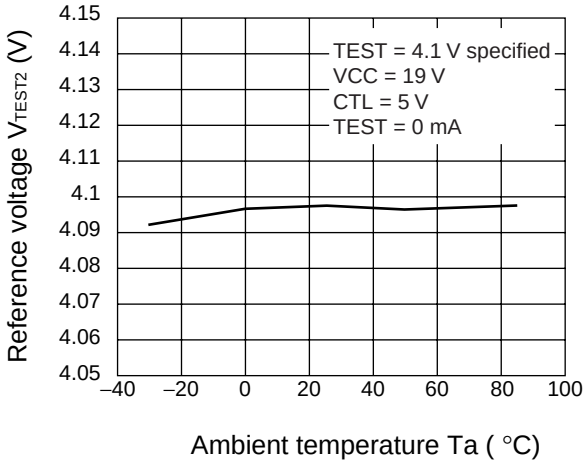
Reference voltage vs. Power supply voltage



Reference voltage vs. Ambient temperature

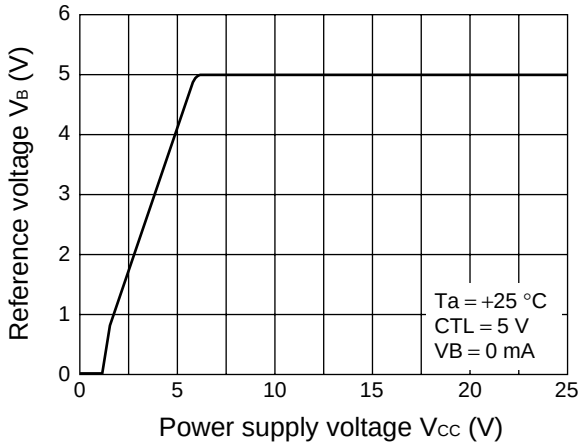


Reference voltage vs. Ambient temperature

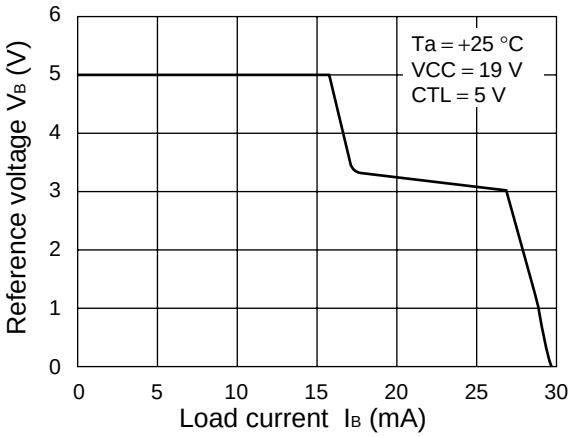


(Continued)

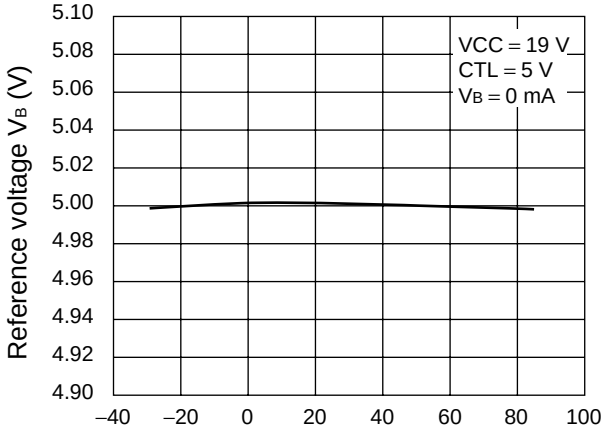
Reference voltage vs. Power supply voltage



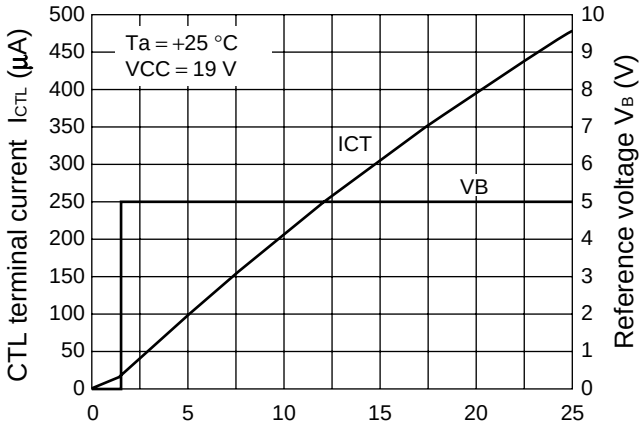
Reference voltage vs. Load current



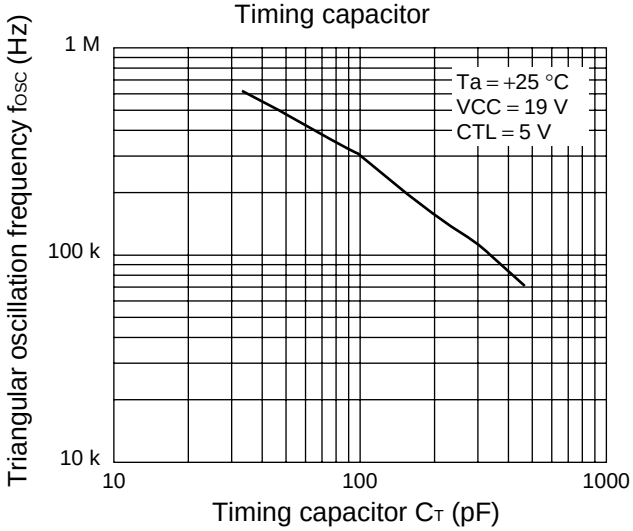
Reference voltage vs. Ambient temperature



CTL terminal current and reference voltage vs. CTL terminal voltage

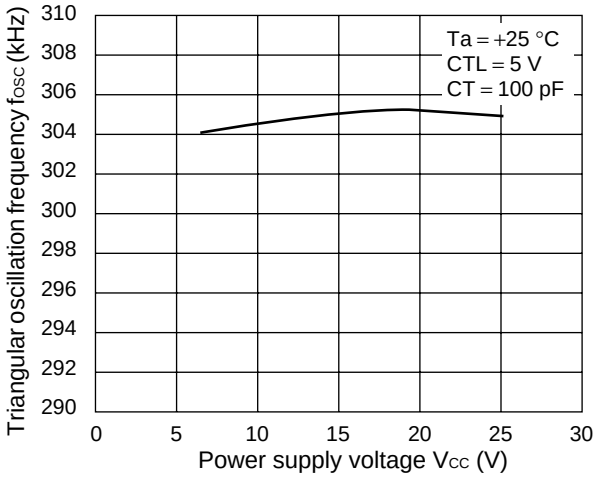


Triangular oscillation frequency vs. Timing capacitor

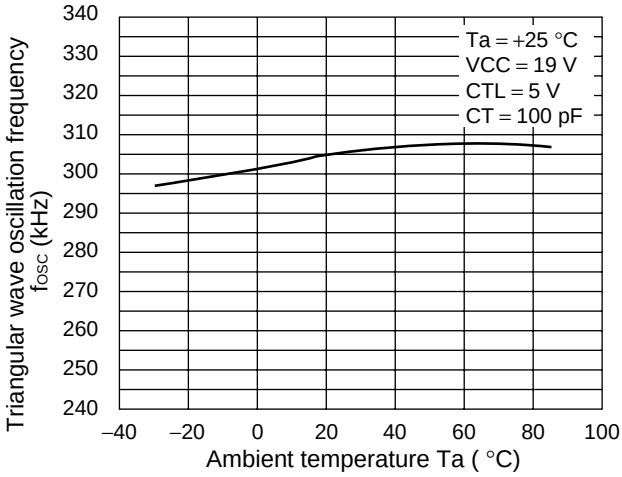


(Continued)

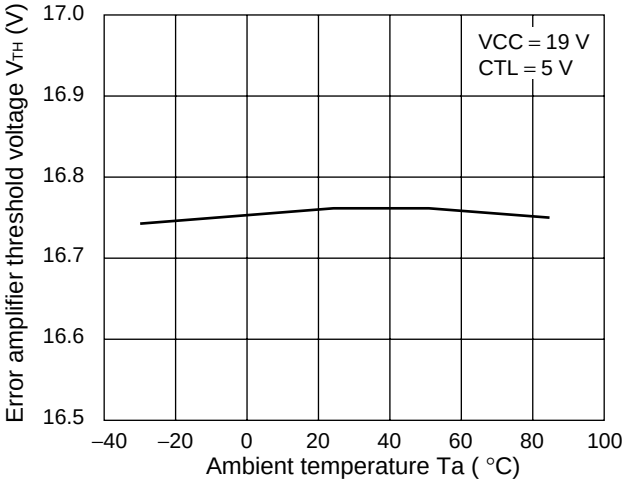
Triangular oscillation frequency vs.
Power supply voltage



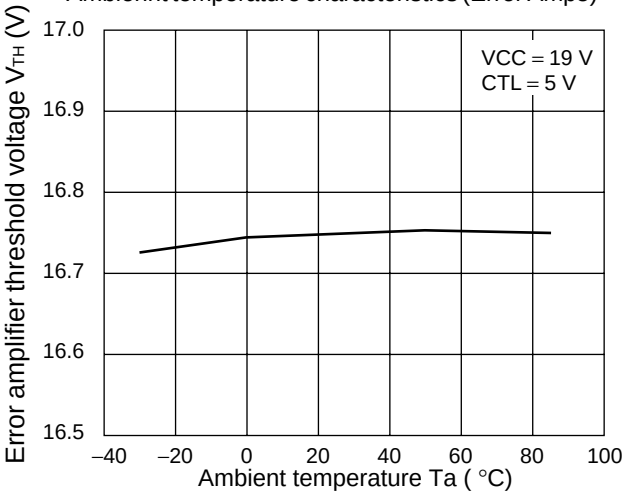
Triangular oscillation frequency vs.
Ambient temperature



Error amplifier threshold voltage vs.
Ambient temperature (Error Amp6)

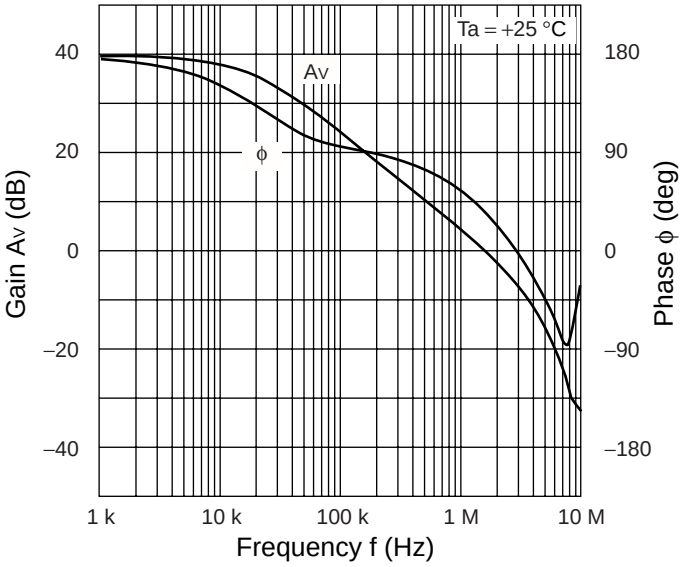


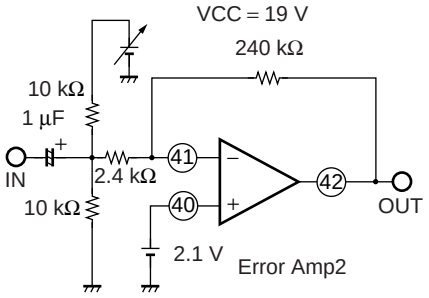
Error amplifier threshold voltage vs.
Ambiennt temperature characteristics (Error Amp5)



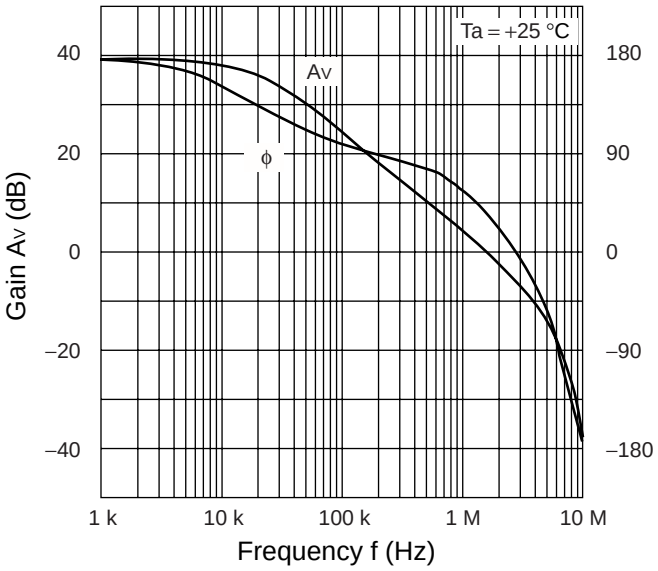
(Continued)

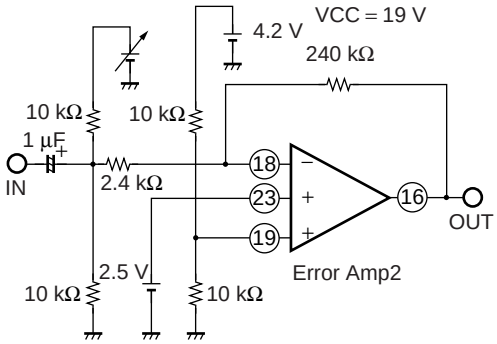
Error amplifier gain, phase vs. Frequency (Error Amp2)





Error amplifier gain, phase vs. Frequency (Error Amp3)

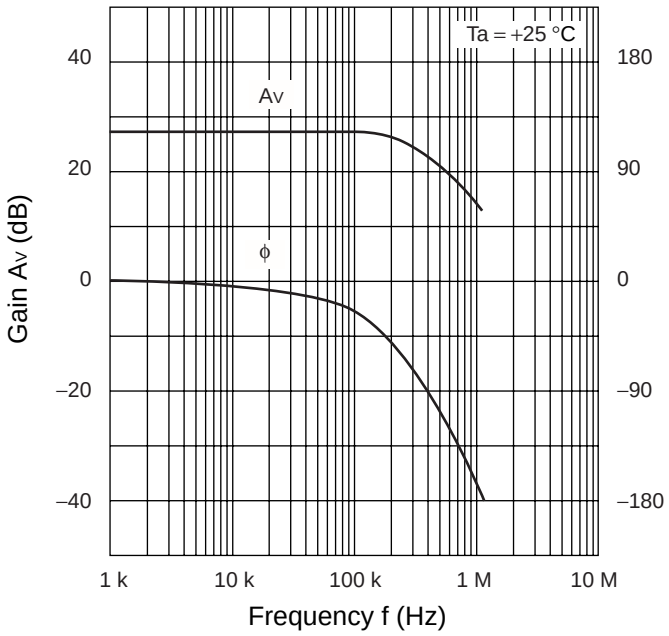


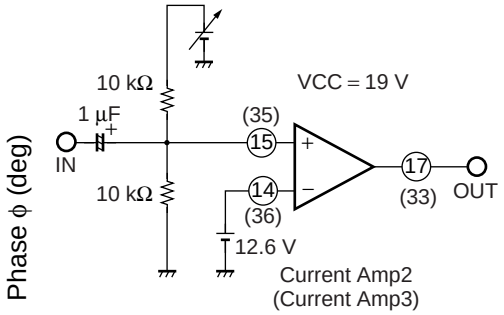


(Continued)

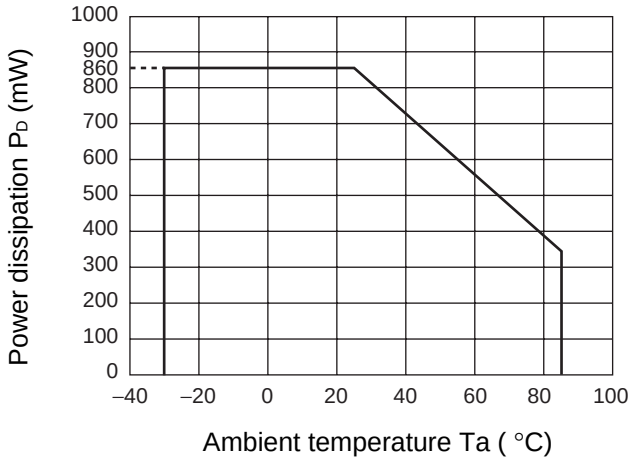
(Continued)

Current detection amplifier, phase vs. Frequency





Power dissipation vs. Ambient temperature



■ FUNCTIONS

1. DC/DC Converter Functions

(1) Reference voltage block (REF)

The reference voltage generator (REF) generates a temperature-compensated reference voltage from the voltage supplied from the VCC terminal (pin 1). The voltage is used as the reference voltage for Error Amp.

(2) Control bias voltage block (VB)

The control bias voltage block (VB) generates a temperature-compensated reference voltage using internal reference voltage (5.0V Typ) from VB terminal. The voltage is used as the reference voltage for the IC's internal circuitry.

The reference voltage can be used to supply a load current of up to 1 mA to an external device through the VB terminal

(3) Triangular waveform oscillator block (OSC)

The triangular wave oscillation frequency setting resistor is built in, and the triangular wave oscillation waveform (amplitude of 1.6 V to 2.6 V) is generated by connecting the triangular wave oscillation frequency setting capacitor with the CT terminal (pin 37) .

The triangular oscillation waveform is input to the PWM comparator on the IC.

(4) Error amplifier block (Error Amp1)

The error amplifier (Error Amp1) controls the charge current with the amplifier which outputs the PWM control signal detecting the total current of the system current and control IC input current. It supports a wide range of common mode input voltages from "0 V to Vcc - 1.8 V".

In addition, an arbitrary loop gain can be set by connecting a feedback resistor and capacitor from FB1 terminal to -INE1 terminal, enabling stable phase compensation to be provided for the system.

This section also outputs signal to mode detection section.

(5) Error amplifier block (Error Amp2)

The error amplifier (Error Amp2) detects the dropping voltage of AC adapter by connecting an external resistor to +INE2 terminal (pin 40), and outputs PWM control signals. It supports a wide range of common mode input voltages from "0 V to Vcc - 1.8 V".

In addition, an arbitrary loop gain can be set by connecting a feedback resistor and capacitor from FB2 terminal (pin 42) to –INE2 terminal (pin 41), enabling stable phase compensation to be provided for the system.

This block also outputs signal to mode detection block.

(6) Error amplifiers block (Error Amp3 and Error Amp4)

The error amplifiers (Error Amp3 and Error Amp4) detect the output voltages of current detection amplifiers (Current Amp2 and Current Amp3) and compare the voltages with ones on +INE3 terminal (pin 19) and +INE4 terminal (pin 31), and then outputting PWM control signal. This block controls charge currents.

In addition, an arbitrary loop gain can be set by connecting a feedback resistor from FB3 terminal (pin 16) to -INE3 terminal (pin 18) and from FB4 terminal (pin 34) to -INE4 terminal (pin 32) and capacitor, enabling stable phase compensation to be provided for the system.

This block also outputs signal to mode detection block.

By connecting a soft-start capacitor to CS1 terminal (pin 23), an inrush current upon power supply startup is prevented. By detecting soft-start with the error amplifier, soft-start time becomes constant, being independent of output loads.

(7) Error amplifiers block (Error Amp5 and Error Amp6)

The error amplifiers (Error Amp5 and Error Amp6) detect the DC/DC converter output voltage and outputs PWM control signals. An on-chip output voltage setting resistor is provided on the IC, external output voltage setting resistor is not needed. A 4-bit decoder selects output voltage among 12.6V (3 cells), 12.3V (3 cells), 16.8V (4 cells), and 16.4V (4 cells), which are applicable to NiMH batteries as well as Li-ion batteries.

In addition, an arbitrary loop gain can be set by connecting a feedback resistor and capacitor from FB5 terminal (pin 30) to -INE5 terminal (pin 29)and from FB6 terminal (pin 20) to -INE6 terminal (pin 21), enabling stable phase compensation to be provided for the system.

This block also outputs signal to mode detection block.

By connecting a soft-start capacitor to CS2 terminal (pin 22), an inrush current upon power supply startup is prevented. By detecting soft-start with the error amplifier, soft-start time becomes constant, being independent of output loads.

(8) Current detection amplifier block (Current Amp1)

The current detection amplifier (Current Amp1) detects voltage dropping occurring across the both sides of output sense resistor (R_{S1}) between +INC1 terminal (pin 48) and -INC1 terminal (pin 47), regarding total current between system current and control IC input current. This block outputs the signal amplified 25 times to next stage error amplifier (Error Amp1).

(9) Current detection amplifier block (Current Amp2 and Current Amp3)

The current detection amplifiers (Current Amp2 and Current Amp3) detect voltage dropping occurring across the both sides of output sense resistor (R_{S2}) between +INC2 terminal (pin 15) and IN1 terminal (pin 14), regarding total current between system current and control IC input current. This block outputs the signal amplified 25 times to next stage error amplifier (Error Amp3).

The current detection amplifier (Current Amp3) detects voltage dropping occurring across the both sides of output sense resistor (R_{S3}) between +INC3 terminal (pin 35) and IN2 terminal (pin 36), and then outputs the signal amplified 25 times to next stage error amplifier (Error Amp3).

(10) PWM comparator block (PWM Comp.)

The PWM comparator is a voltage-to-pulse width converter for controlling the output duty depending on the output voltage of the error amplifiers. The comparator compares the triangular wave generated by the triangular wave oscillator with the output voltage of error amplifier and voltage of DTC terminal (pin 39), and turns on Pch MOS FET when triangular wave voltage is lower than output voltage of error amplifier and voltage of DTC terminal.

(11) Output block (OUT)

The output block is designed in the totem pole configuration, capable of driving an external P-channel MOS FET. Output amplitude is set to "6V (typical)" at "L" level on output stage by using a voltage generated in bias voltage block.

This feature allows higher conversion efficiency and low withstanding voltages on external Pch MOS FET even under wide input voltage range.

(12) Bias voltage block (VH)

The Bias voltage block output a minimum voltage of output circuit, Vcc-6V (typical).

A same voltage as Vcc is output under standby status.

2. VDD Logic Block

(1) Control block (CTL)

The system is placed under standby mode by setting CTL terminal (pin 7) to "L" level (power supply current is a maximum of 10 μA under standby mode). Setting "H" level at CTL terminal generates an internal reference voltage, placing the system under output operation status.

After setting "L" level at CTL terminal, CTL signal reactivation time (t_{RCTL}=2ms(Min)) is required to set the "H" level signal.

(2) Decoder block (DEC)

By applying signals to D0 terminal (pin 2) through D3 terminal (pin 5), the 4-bit decoder section (DEC) selects output voltage among 12.6V (3 cells), 12.3V (3 cells), 16.8V (4 cells), and 16.4V (4 cells). The voltages are applicable not only to Li-ion batteries but also to NiMH batteries that require cancellation of output voltage control. (See "■ DECODER SECTION OUTPUT VOLTAGE SETTING CODES" for details.)

(3) Mode detection block (MODE Comp.)

The mode detection block outputs which charge mode to OUT-EA1 terminal (pin 13), OUT-EA2 terminal (pin 12), OUT EC terminal (pin 11), and OUT-EV terminal (pin 10). For dynamically-controlled charging mode, OUT-EA1 terminal is set to "L" level and OUT-EA2 terminal, OUT-EC terminal, and OUT-EV terminal are set to "H" level. For Differential-charging mode, OUT-EA2 terminal is set to "L" level and OUT-EA1 terminal, OUT-EC terminal, and OUT-EV terminal are set to "H" level. For Constant-current charge mode, OUT-EC terminal is set to "L" level and OUT-EA1 terminal, OUT-EA2 terminal, and OUT-EV terminal are set to "H" level. For Constant-voltage charge mode, OUT-EV terminal is set to "L" level and OUT-EA1 terminal, OUT-EA2 terminal, and OUT-EC terminal are set to "H" level.

Using DTC terminal (pin 39), duty setting from external device is allowed. In such a case, set all of OUT-EA1 terminal, OUT-EA2 terminal, OUT-EC terminal, and OUT-EV terminal to H level when FB terminal voltages of all error amplifiers are higher than DTC terminal voltage.

3. Control Function

Specifies settings of "on" and "off" of outputs with setting conditions of CTL terminal (pin 7).

"On" and "off" settings of outputs

Voltage level of CTL terminal	"On/off" status of output
L	OFF (standby mode)
H	ON (operating mode)

4. Protection Functions

(1) Undervoltage lockout protection circuit block (UVLO)

The transient state or a momentary decrease in power supply voltage (V_{CC}) or internal reference voltage (VB), which occurs when the power supply is turned on, may cause the control IC to malfunction, resulting in breakdown or degradation of the system.

To prevent such malfunctions, the undervoltage lockout protection circuit detects decrease of the internal reference voltage level with respect to the power supply voltage and internal reference voltage, and holds OUT terminal (pin 24) on output terminals at "H" level. The circuit restores the output transistor to normal when the supply voltage and internal reference voltage reach the threshold voltage of the undervoltage lockout protection circuit.

(2) Functions upon operation of protection circuit (UVLO)

The following table summarizes functions upon operation of VCCUVLO and VBUVLO (VCC or VB voltage is below UVLO threshold voltage).

CS1	CS2	OUT	OUT-EA1	OUT-EA2	OUT-EV	OUT-EC
L	L	H	L	L	L	L

5. Soft-start Function

(1) Soft-start block (SOFT1 and SOFT2)

By connecting capacitors to CS1 terminal (pin 23) and CS2 terminal (pin 22), an inrush current upon power supply startup is prevented. By detecting soft-start with the error amplifier, soft-start time becomes constant, being independent of output loads of DC/DC converter.

(See "■ SETTING SOFT-START TIME " for details.)

■ SETTING CHARGE CURRENT

Voltage values of +INE3 terminal (pin 19) and +INE4 terminal (pin 31) specify charge current (output limit current value). If a current exceeding specified current value is about to flow, a charge voltage drops by the setting current value.

+INE3 and +INE4 voltage setting

$+INE3\ (V) = 25 \times I2\ (A) \times R_{S2}\ (\Omega)$

$+INE4\ (V) = 25 \times I3\ (A) \times R_{S3}\ (\Omega)$

+INE3 : Voltage for setting charge current on battery 1

+INE4 : Voltage for setting charge current on battery 2

■ SETTING MAXIMUM CURRENT on AC ADAPTER

Voltage value of +INE1 terminal (pin 43) specifies charge current (output limit current value) so that total current of system current and control IC input current does not exceed maximum current of AC adapter. If a current exceeding specified current value is about to flow, system is placed under Differential-charging mode by the specified current value, and charge current is reduced.

+INE1 voltage setting

$+INE1\ (V) = 25 \times I1\ (A) \times R_{S1}\ (\Omega)$

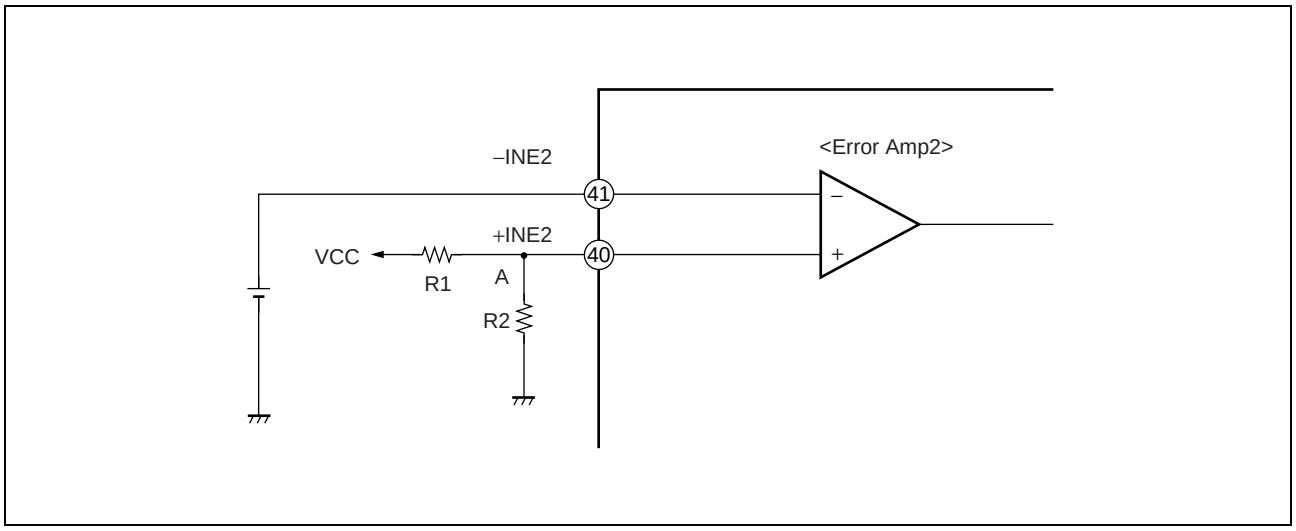
+INE1 : Voltage for setting maximum current of AC adapter

■ SETTING DETECTION VOLTAGE FOR AC ADAPTER VOLTAGE

By connecting an external resistor to +INE2 terminal (pin 40), the system is placed under Dynamically-controlled charging mode when voltage at junction A of AC adapter input voltage (VCC) decreases below - INE2 terminal voltage. This feature decreases charge current to keep on constant power of AC adapter.

AC adapter detection voltage setting : Vth

$Vth = (R1 + R2) / R2 \times -INE2$



■ SETTING TRIANGULAR WAVE OSCILLATION FREQUENCY

Triangular wave oscillation frequency is specified by connecting a timing capacitor (C_T) to CT terminal (pin 37).

Triangular wave oscillation frequency : f_{OSC}

f_{OSC} (kHz) ≒ 30000 / C_T (pF)

■ DECODER BLOCK OUTPUT VOLTAGE SETTING CODES

The following summarizes decoder block output voltage setting codes :

D0	D1	D2	D3	DC/DC output voltage (V) < IN1, IN2 >	Application			Charge mode symbol
					BATT type	Number of cells	Charge voltage (V)	
0	0	0	0	12.3	Li-ion	3	4.1	Li3C41
0	0	0	1	12.6	Li-ion	3	4.2	Li3C42
0	0	1	0	12.3	none	none	none	—
0	0	1	1	12.3	none	none	none	—
0	1	0	0	12.3	none	none	none	—
0	1	0	1	12.3	none	none	none	—
0	1	1	0	16.4	Li-ion	4	4.1	Li4C41
0	1	1	1	16.8	Li-ion	4	4.2	Li4C42
1	0	0	0	12.3	none	none	none	—
1	0	0	1	12.3	none	none	none	—
1	0	1	0	12.3	none	none	none	—
1	0	1	1	12.3	none	none	none	—
1	1	0	0	12.3	none	none	none	—
1	1	0	1	Not controlled	NiMH	10 to 12	—	NiMH
1	1	1	0	12.3	none	none	none	—
1	1	1	1	12.3	none	none	none	—

< Functions of bits >

D0 : Selecting BATT type (Li-ion or NiMH)

D1 and D2 : Selecting the number of cells (3 Cell or 4 Cell)

D3 : Selecting charge voltage (4.1 V or 4.2 V)

■ SETTING SOFT-START TIME

1. Setting Soft-start Time in Constant-current Mode

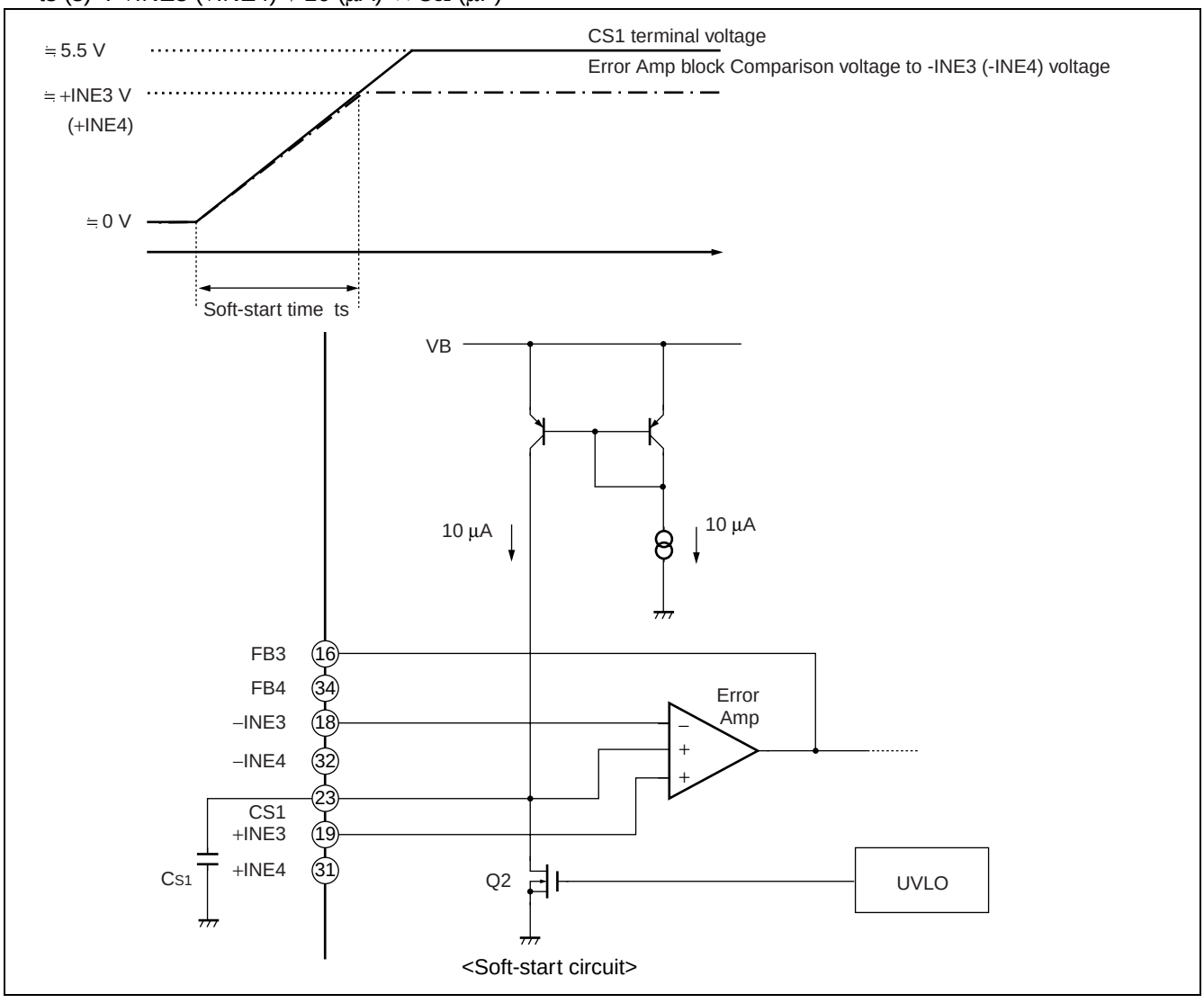
To prevent surge currents when the IC is turned on, you can set a soft-start by connecting a soft-start capacitor (Cs1) to the CS1 terminal (pin 23).

Setting CTL terminal (pin 7) voltage to "H" level to activate the IC (Vcc ≥ UVLO threshold voltage), Q2 is turned off and charging starts on soft-start capacitor (Cs1) connected to the CS1 terminal at 10 μA.

The error amplifier output (FB3 terminal (pin 16) or FB4 terminal (pin 34)) is determined by comparison between the lower one of the potentials at two non-inverted input terminals (+INE3 terminal (pin 19) voltage (+INE4 terminal (pin 31) voltage, and CS1 terminal voltage). The FB3 (FB4) terminal voltage during the soft-start period (CS1 terminal voltage < +INE3 (+INE4)) is therefore determined by comparison between the -INE3 (-INE4) terminal and CS1 terminal voltages. The DC/DC converter output voltage rises in proportion to the CS1 terminal voltage as the soft-start capacitor connected to the CS1 terminal is charged. The soft-start time is obtained from the following equation:

Soft-start time : ts (time to output 100%)

$ts\ (s) \fallingdotseq +INE3\ (+INE4)\ /\ 10\ (\mu A)\ \times C_{S1}\ (\mu F)$



<Soft-start circuit>

2. Setting Soft-start Time in Constant-voltage Mode

To prevent surge currents when the IC is turned on, you can set a soft-start by connecting a soft-start capacitor (C_{S2}) to the CS2 terminal (pin 22).

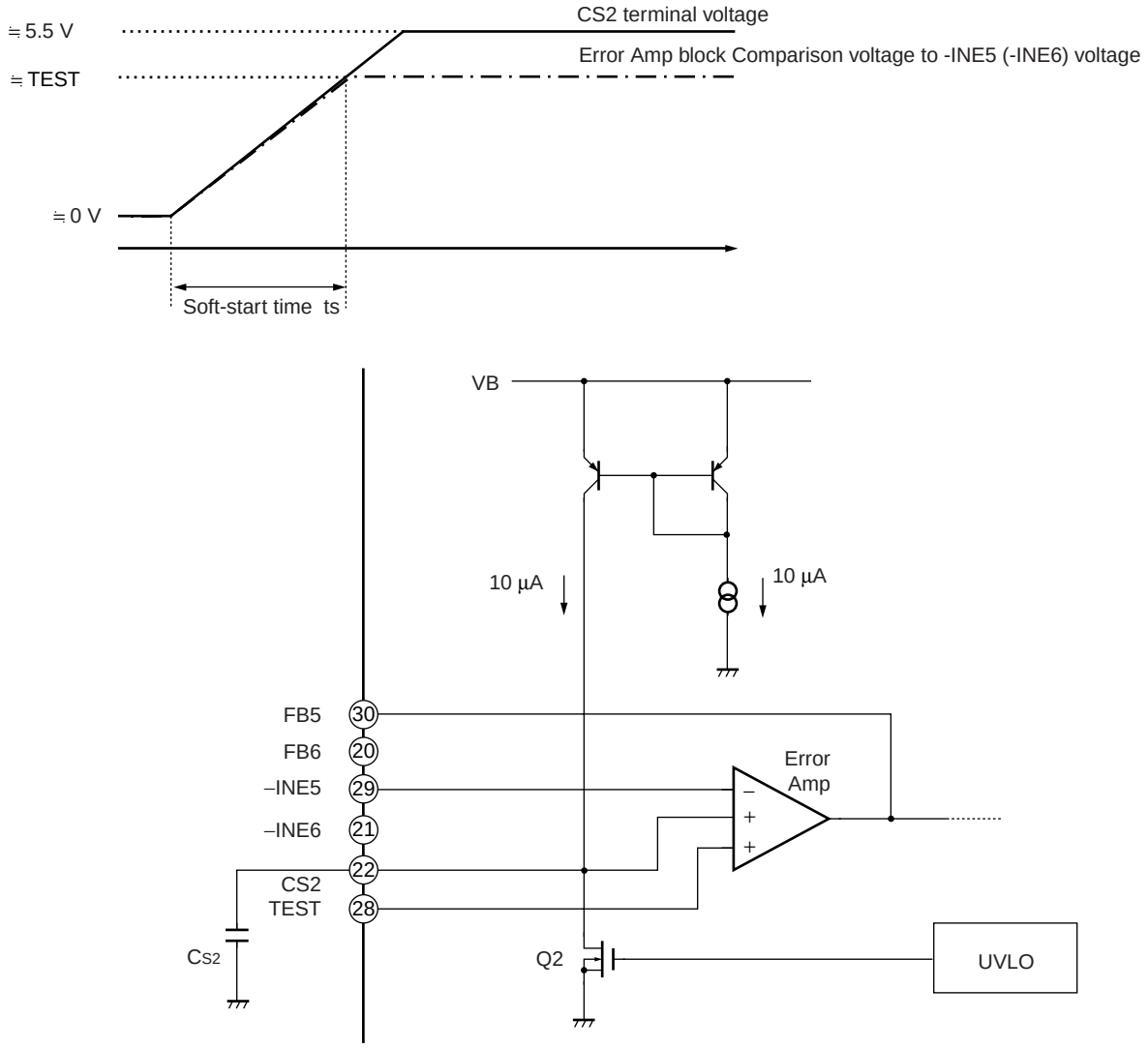
Setting CTL terminal (pin 7) voltage to "H" level to activate the IC (Vcc ≥ UVLO threshold voltage), Q2 is turned off and charging starts on soft-start capacitor (C_{S2}) connected to the CS2 terminal at 10 μA.

The error amplifier output (FB5 terminal (pin 30) or FB6 terminal (pin 20)) is determined by comparison between the lower one of the potentials at two noninverting input terminals (TEST terminal (pin 28) voltage and CS2 terminal voltage). The FB5 (FB6) terminal voltage during the soft-start period (CS2 terminal voltage < TEST) is therefore determined by comparison between the -INE5 (-INE6) terminal and CS2 terminal voltages.

The DC/DC converter output voltage rises in proportion to the CS2 terminal voltage as the soft-start capacitor connected to the CS2 terminal is charged. The soft-start time is obtained from the following equation:

Soft-start time : ts (time to output 100%)

$ts\ (s) \fallingdotseq TEST\ (V) / 10\ (\mu A) \times C_{S2}\ (\mu F)$



<Soft-start circuit>

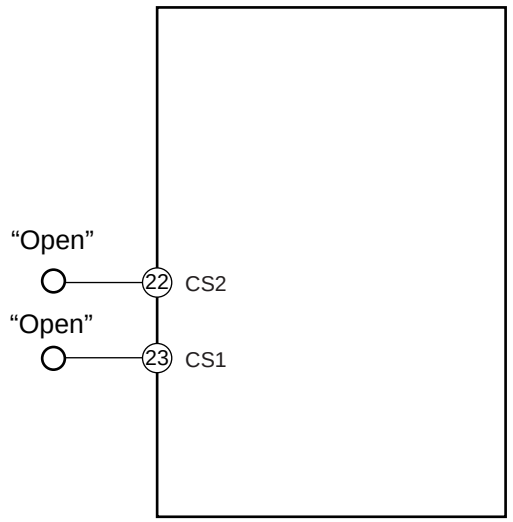
■ USING WITH SHORT-CIRCUIT CS1 AND CS2 TERMINAL

By making a short circuit CS1 terminal (pin 23) and CS2 terminal (pin 22), the start-up of constant current charging mode and constant voltage charging mode is allowed at the same time.

A capacitor to be connected must have a charging current at 20 μA.

■ TREATMENT WITHOUT USING THE CSCP TERMINAL

If the soft-start function is not used, open CS1 terminal (pin 23) and CS2 terminal (pin 22).

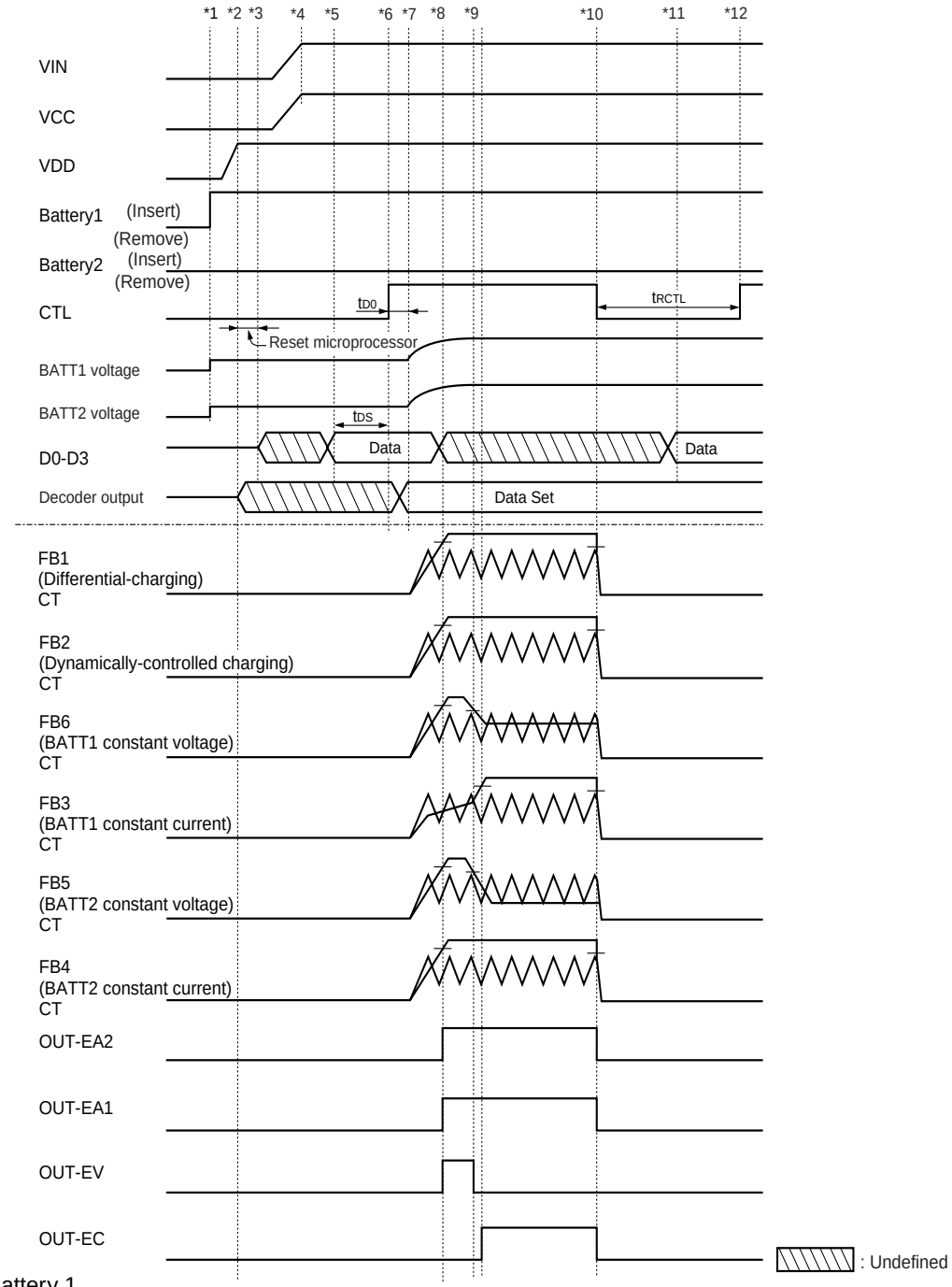


<Treatment without using the CSCP terminal>

■ OPERATING SEQUENCE

1. Sequence of Normal Power Supply Startup and Charge Startup Completion

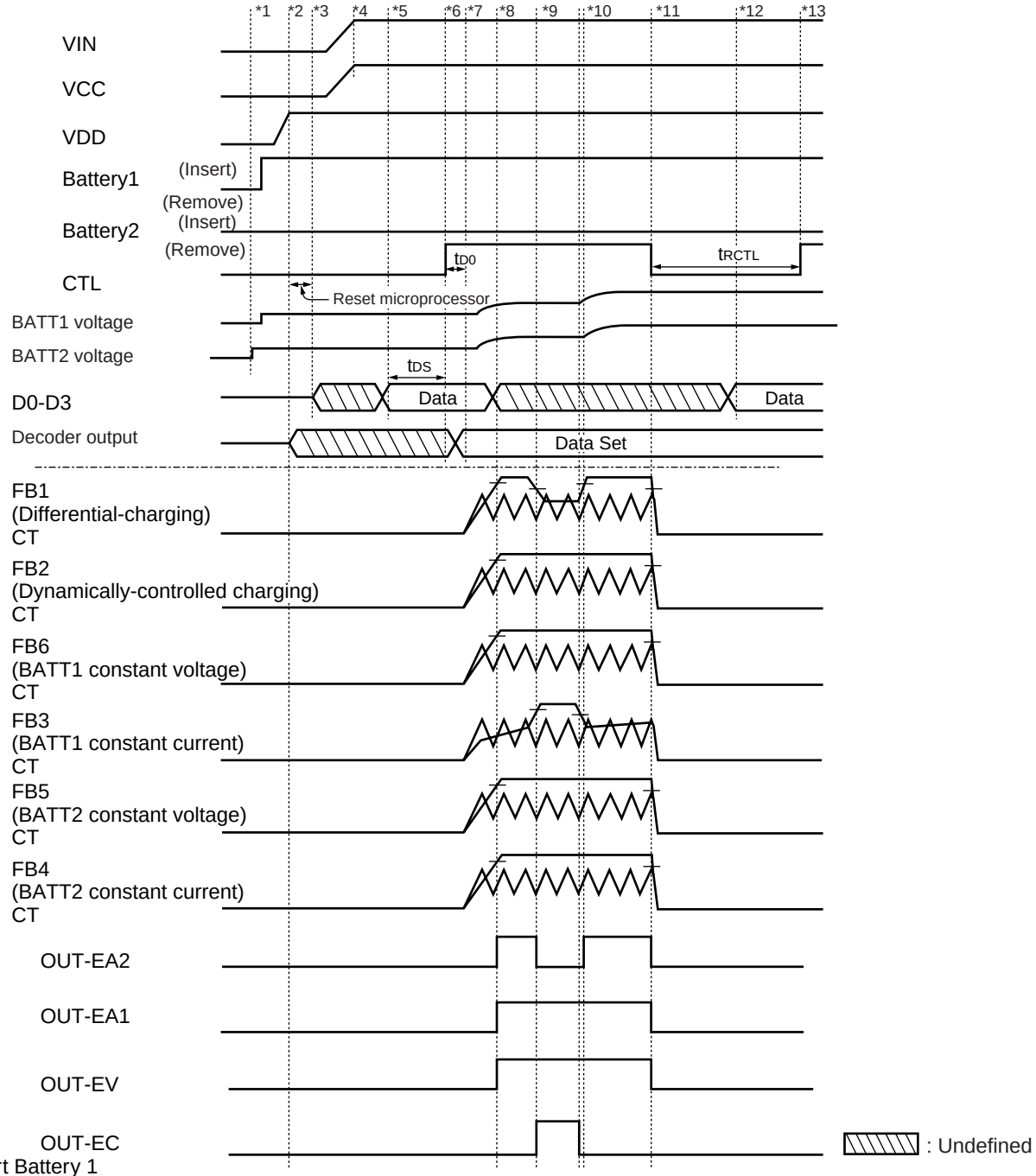
<AC adapter is connected with Battery 1 inserted>



*1 :Insert Battery 1
*2 :VDD rises. OUT-EA1, OUT-EA2, OUT-EV, and OUT-EC = “L” level
*3 :CTL signal is “L” level after resetting microprocessor (CTL = “HiZ” until microprocessor is reset) .
*4 :VIN and VCC rises by connecting AC adapter.
*5 :Charge voltage data is set by microprocessor.
*6 :CTL signal is turned on after data setup time (t_{DS}) .
*7 :Upon detecting CTL signal at “H” level, decoder data is set after data output delay time (t_{D0}) .
*8 :Shift to constant current mode. OUT-EA1, OUT-EA2, and OUT-EV = “H” level.
*9 :Shift from constant current charge control to constant voltage change control. OUT-EC = “H”level, OUT-EV = “L”level.
*10:With CTL signal “L” level, OUT-EA1, OUT-EA2, OUT-EV, and OUT-EC=“L” level.
*11:Data set after turning off CTL signal.
*12:After CTL signal set at “L” level, CTL signal reactivation time (t_{RCTL}=2 ms (Min)) or longer time is required.

2. Sequence that Limitation (Differential Control) Activates by Input Current during Constant Current Charging on BATT1

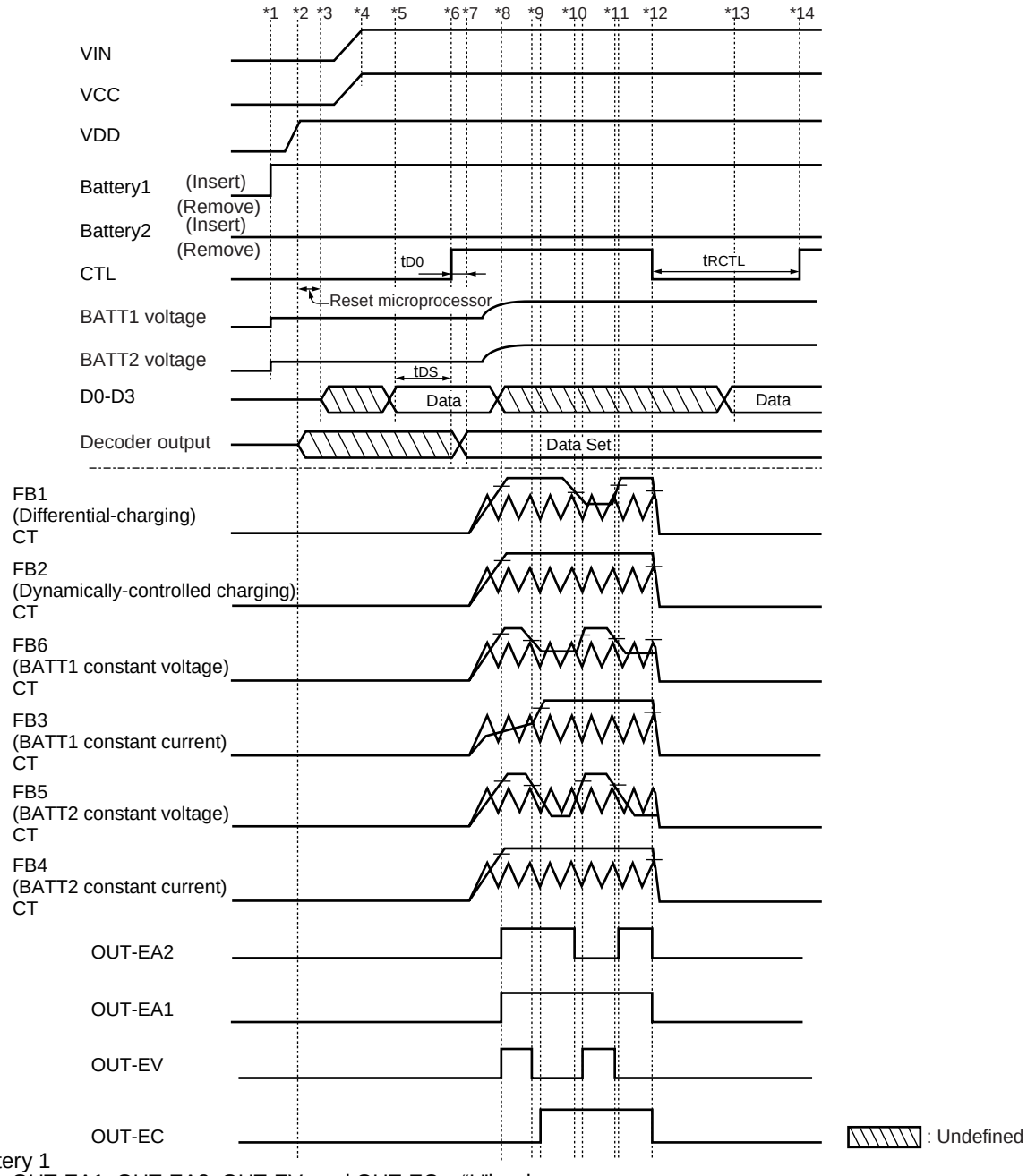
<AC adapter is connected with Battery 1 inserted, and exceeding input current>



*1:Insert Battery 1
*2:VDD rises. OUT-EA1, OUT-EA2, OUT-EV, and OUT-EC = “L” level
*3:CTL signal is “L” level after resetting microprocessor (CTL = “HiZ”until microprocessor is reset) .
*4:VIN and VCC rises by connecting AC adapter.
*5:Charge voltage data is set by microprocessor.
*6:CTL signal is turned on after data setup time (t_{DS}) .
*7:Upon detecting CTL signal at “H” level, decoder data is set after data output delay time (t_{D0}) .
*8:Shift to constant current mode. OUT-EA1, OUT-EA2, and OUT-EV = “H”level.
*9:Shift from constant current charge control to differential charge control by exceeding input current. OUT-EA1 = “L” level, OUT-EC = “H” level.
*10:Returning to input current level within allowable range, shift to constant current charge control. OUT-EA1 = “H” level, OUT-EC = “L” level.
*11:After CTL signal set at “L” level, OUT-EA1, OUT-EA2, OUT-EV, and OUT-EC = “L” level.
*12:Data set after turning off CTL signal.
*13:After CTL signal set at "L" level, CTL signal reactivation time (t_{RCTL} = 2 ms (Min)) or longer time is required.

3. Sequence that Limitation (Differential Control) Activates by Input Current during Constant Voltage Charging on BATT1

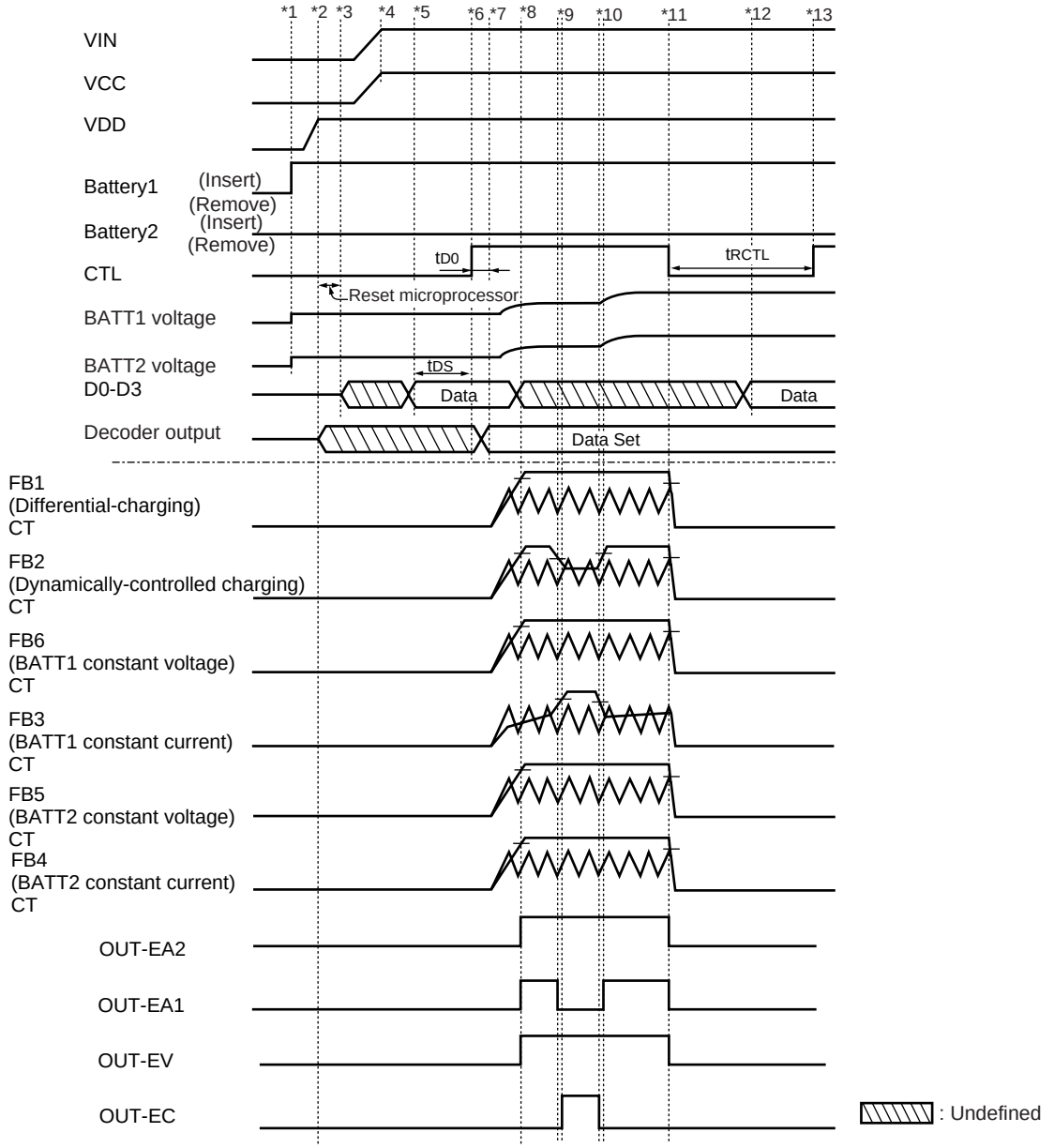
<AC adapter is connected with Battery 1 inserted, exceeding input current>



*1:Insert Battery 1
*2:VDD rises. OUT-EA1, OUT-EA2, OUT-EV, and OUT-EC = “L”level
*3:CTL signal is “L”level after resetting microprocessor (CTL = “HiZ” until microprocessor is reset) .
*4:VIN and VCC rises by connecting AC adapter.
*5:Charge voltage data is set by microprocessor.
*6:CTL signal is turned on after data setup time (t_{DS}) .
*7:Upon detecting CTL signal at “H” level, decoder data is set after data output delay time (t_{D0}) .
*8:Shift to constant current mode. OUT-EA1, OUT-EA2, and OUT-EV = “H”level.
*9:Shift from constant current charge control to constant voltage charge control. OUT-EC = “H”level, OUT-EV = “L”level.
*10:Shift to differential charge control by exceeding input current. OUT-EA1 = “L” level, OUT-EV = “H” level.
*11:Returning to input current level within allowable range, shift to constant voltage charge control. OUT-EA1 = “H”level, OUT-EV = “L”level
*12:After CTL signal set at“L” level, OUT-EA1, OUT-EA2, OUT-EV, and OUT-EC = “L” level.
*13:Data set after turning off CTL signal.
*14:After CTL signal set at“L” level, CTL signal reactivation time (t_{RCTL} = 2 ms (Min)) or longer time is required.

4. Sequence that Limitation (Dynamically-controlled Charging) Activates by Dropping Input Current during Constant Current Charging on BATT1

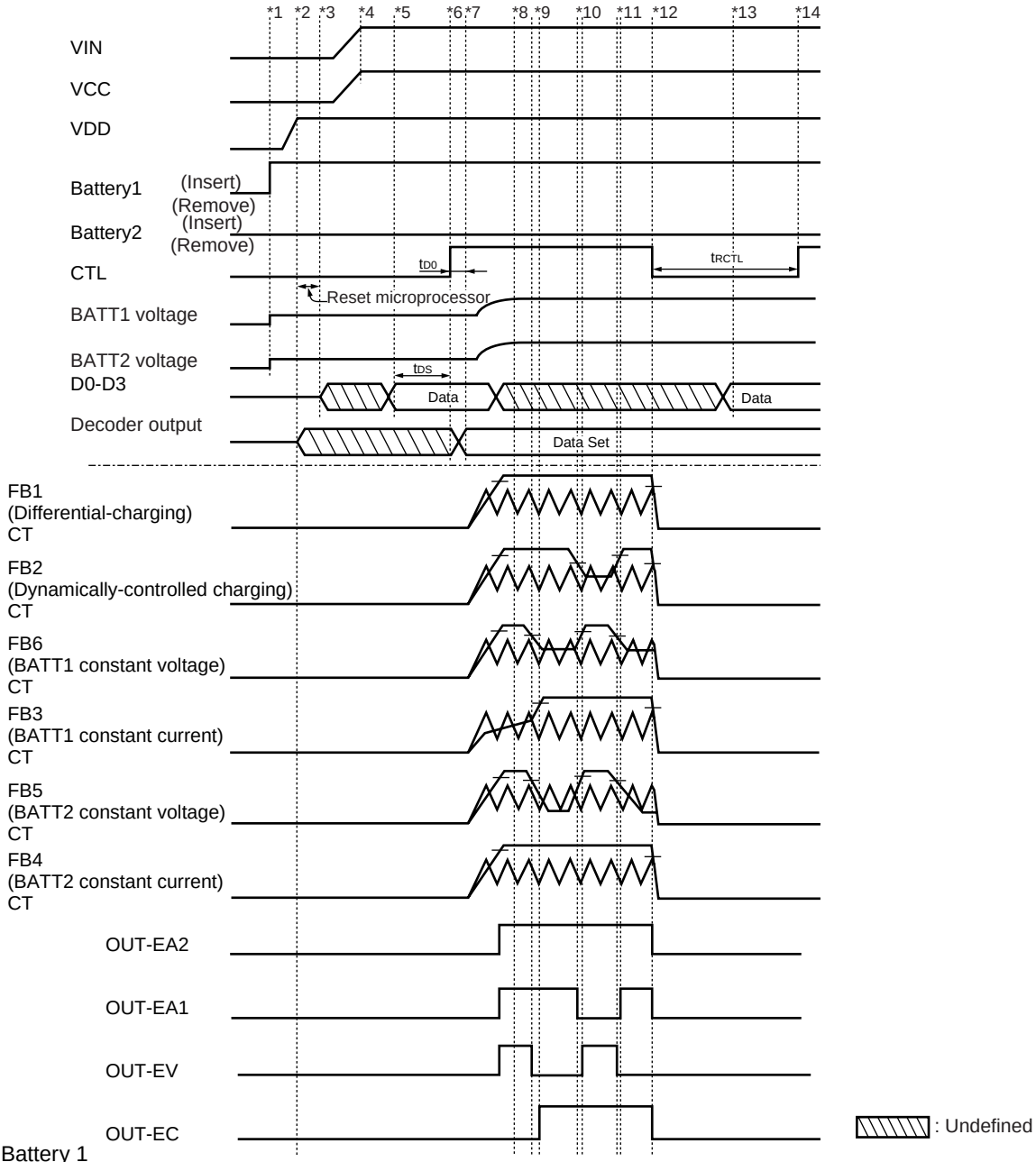
<AC adapter is connected with Battery 1 inserted, under dropping input current>



*1:Insert Battery 1
*2:VDD rises. OUT-EA1, OUT-EA2, OUT-EV, and OUT-EC = “L” level
*3:CTL signal is “L” level after resetting microprocessor (CTL = “HiZ” until microprocessor is reset) .
*4:VIN and VCC rises by connecting AC adapter.
*5:Charging voltage data is set by microprocessor.
*6:CTL signal is turned on after data setup time (t_{DS}) .
*7:Upon detecting CTL signal at “H” level, decoder data is set after data output delay time (t_{D0}) .
*8:Shift to constant current mode. OUT-EA1, OUT-EA2, and OUT-EV = “H” level.
*9:Shift from constant current charge control to dynamically-controlled charge control due to dropping input voltage. OUT-EA2 = “L” level, OUT-EC = “L” level
*10:Returning to input voltage level within allowable range, shift to constant current charge control. OUT-EA2 = “H” level, OUT-EC = “L” level.
*11:After CTL signal set at “L” level. OUT-EA1, OUT-EA2, OUT-EV, and OUT-EC = “L” level.
*12:Data set after turning off CTL signal.
*13:After CTL signal set at “L” level, CTL signal reactivation time (t_{RCTL} = 2 ms (Min)) or longer time is required.

5. Sequence that Limitation (Dynamically-controlled Charging) Activates by Dropping Input Voltage during Constant Voltage Charging on BATT1

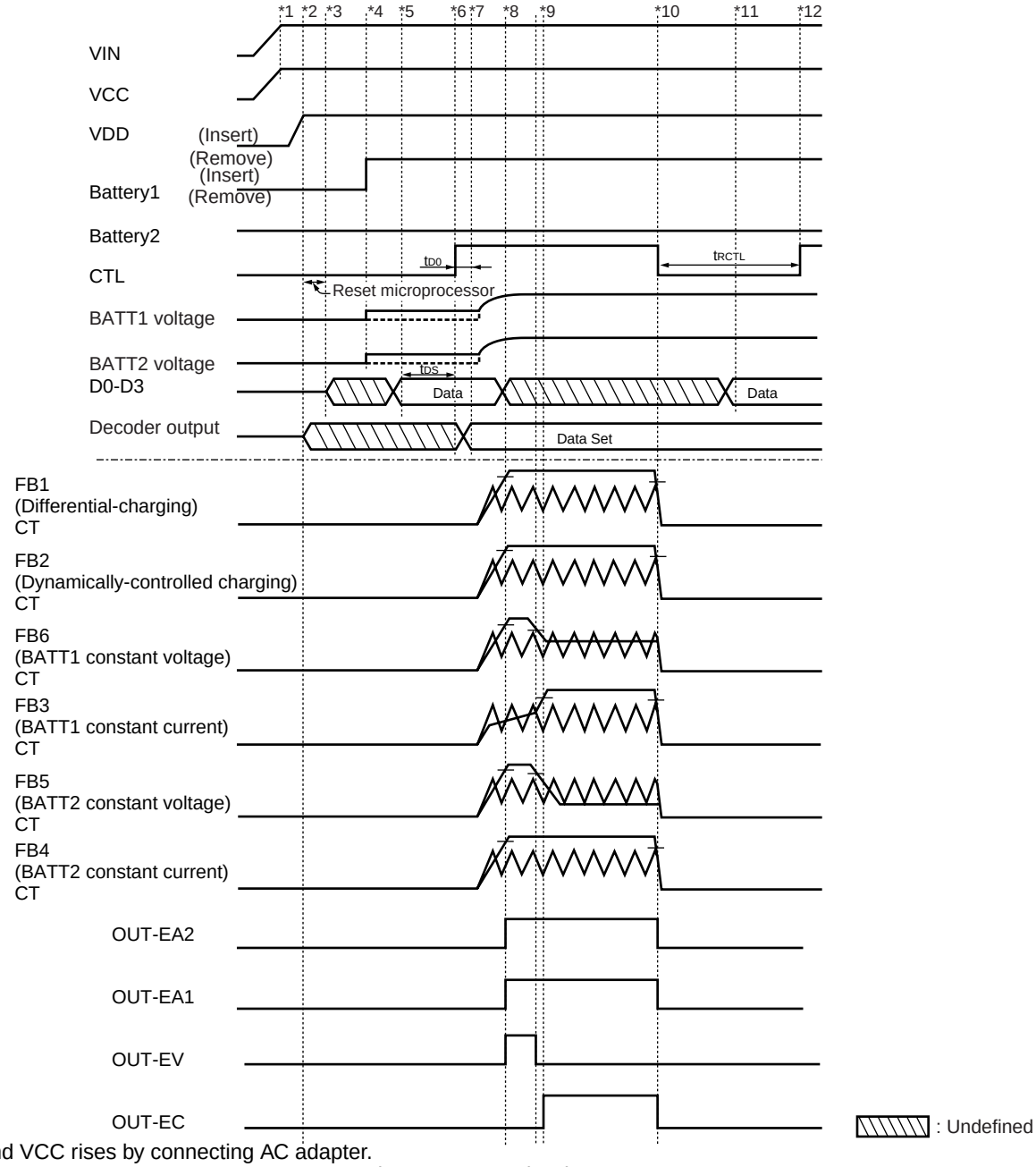
<AC adapter is connected with Battery 1 inserted, under dropping input voltage>



*1:Insert Battery 1
*2:VDD rises. OUT-EA1, OUT-EA2, OUT-EV, and OUT-EC = “L” level
*3:CTL signal is “L” level after resetting microprocessor (CTL = “HiZ” until microprocessor is reset) .
*4:VIN and VCC rises by connecting AC adapter.
*5:Charge voltage data is set by microprocessor.
*6:CTL signal is turned on after data setup time (t_{DS}) .
*7:Upon detecting CTL signal at “H” level, decoder data is set after data output delay time (t_{D0}) .
*8:Shift to constant current mode. OUT-EA1, OUT-EA2, and OUT-EV = “H” level.
*9:Shift from constant current mode to constant voltage charge control. OUT-EC = “H” level, OUT-EV = “L” level.
*10:Shift to dynamically-controlled charge control due to dropping input voltage.
OUT-EA2 = “L” level, OUT-EV = “H” level.
*11:Returning to input voltage level within allowable range, shift to constant voltage charge control. OUT-EA2 = “H” level, OUT-EV = “L”level
*12:After CTL signal set at “L” level, OUT-EA1, OUT-EA2, OUT-EV, and OUT-EC = “L” level
*13:Data set after turning off CTL signal.
*14:After CTL signal set at “L” level, CTL signal reactivation time (t_{RCTL} = 2 ms (Min)) or longer time is required.

6. Sequence of Normal Power Supply Startup and Charge Startup Completion

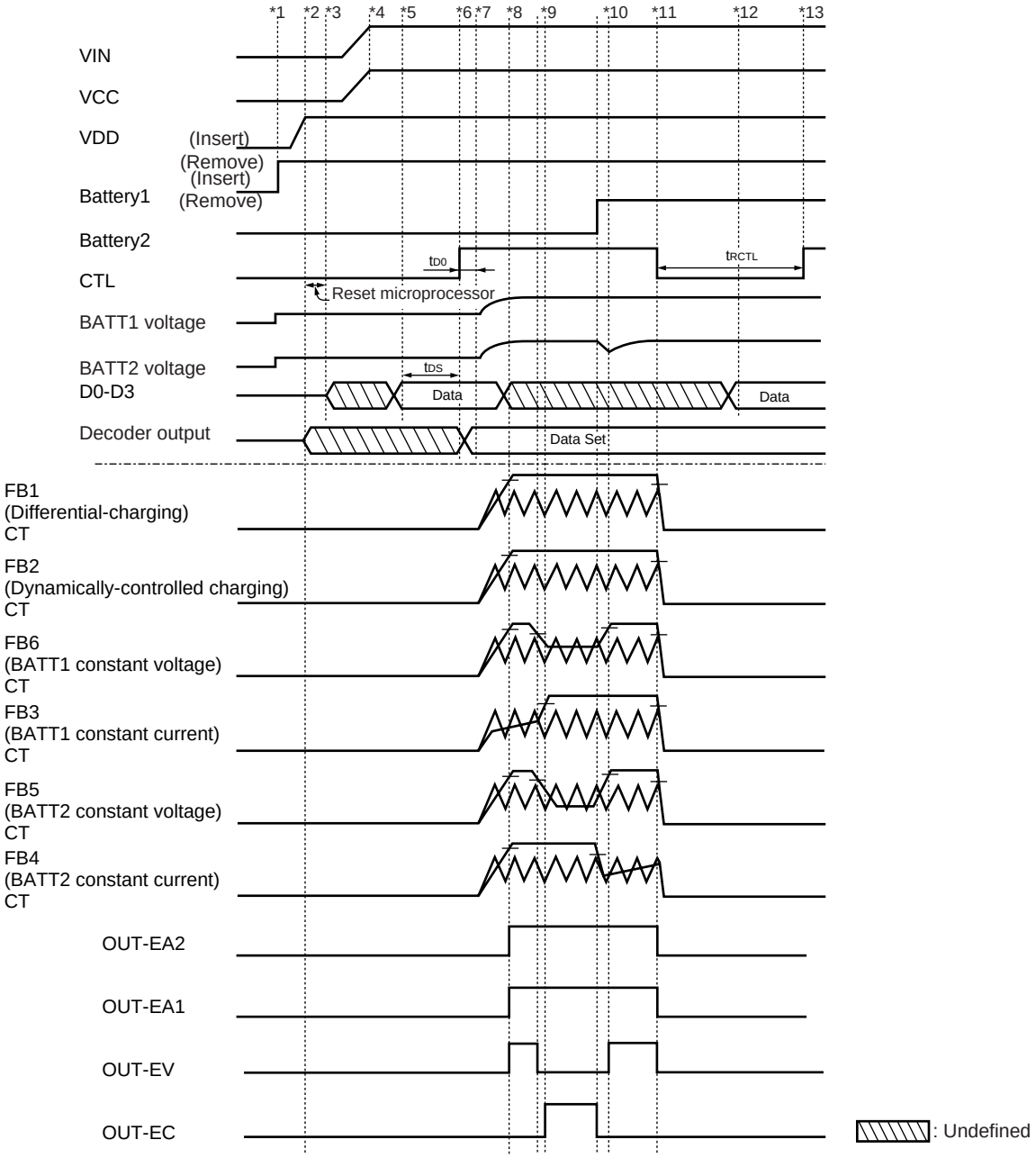
<Battery 1 is inserted with AC adapter is connected, or with "0V" battery voltage, AC adapter is connected and then Battery 1 is inserted>



*1:VIN and VCC rises by connecting AC adapter.
*2:VDD rises. OUT-EA1, OUT-EA2, OUT-EV, and OUT-EC = “L” level.
*3:CTL signal is “L” level after resetting microprocessor (CTL = “HiZ” until microprocessor is reset) .
*4:Insert Battery 1
*5:Charging voltage data is set by microprocessor.
*6:CTL signal is turned on after data setup time (t_{DS}) .
*7:Upon detecting CTL signal at “H” level, decoder data is set after data output delay time (t_{D0})
*8:Shift to constant current mode. OUT-EA1, OUT-EA2, and OUT-EV = “H” level.
*9:Shift from constant current charge control to constant voltage change control. OUT-EC = “H” level, OUT-EV = “L”level.
*10:With CTL signal“L” level, OUT-EA1, OUT-EA2, OUT-EV, and OUT-EC = “L” level.
*11:Data set after turning off CTL signal.
*12:After CTL signal set at “L” level, CTL signal reactivation time (t_{RCTL} = 2 ms (Min)) or longer time is required.

7. Sequence when Battery 2 (almost empty) is inserted during BATT1 is being charged constant voltage , and shifting to constant current charge mode

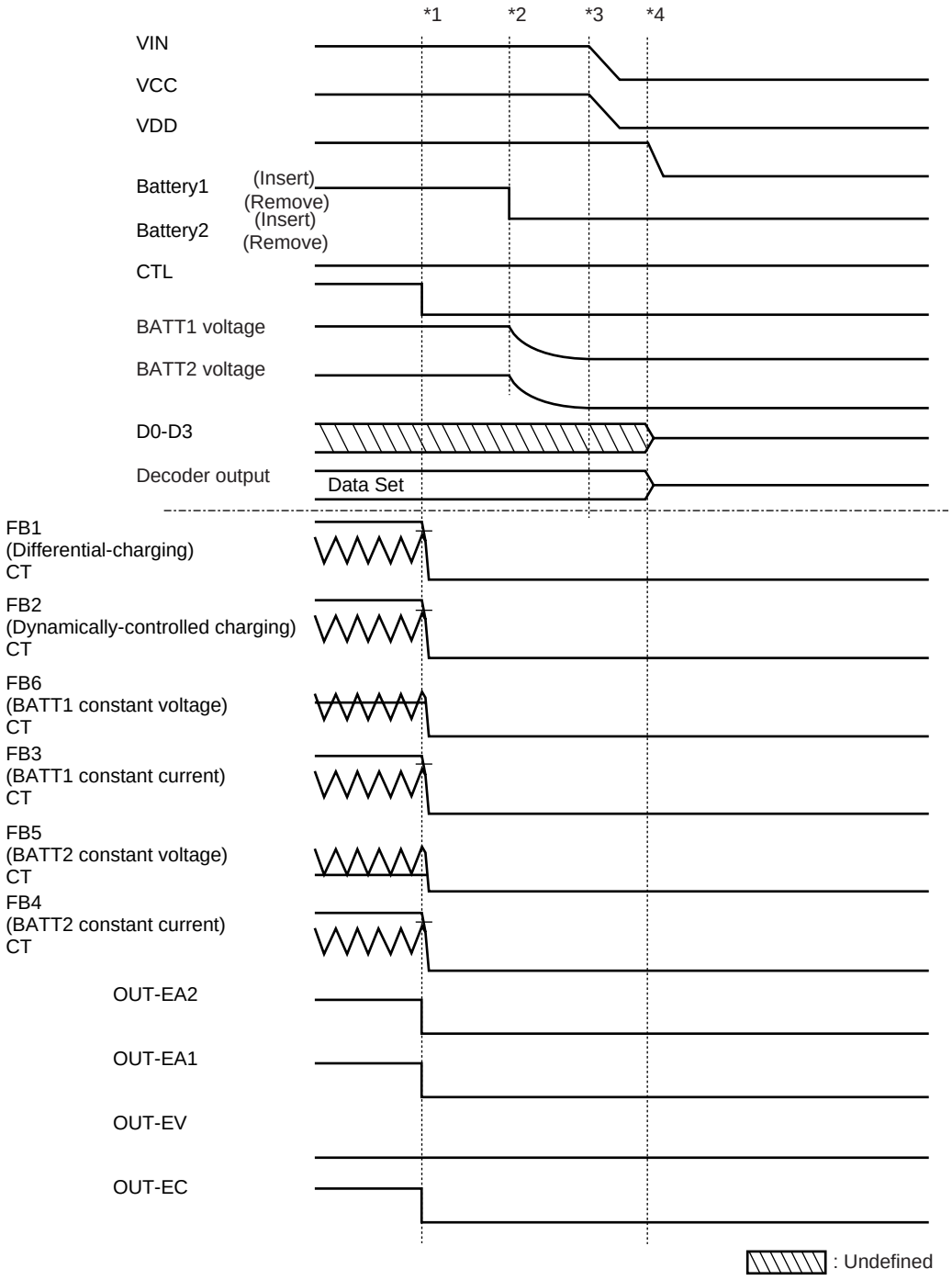
<Battery 2 (almost empty) is inserted when AC adapter is connected and Battery 1 is inserted >



*1:Insert Battery 1.
*2:VDD rises. OUT-EA1, OUT-EA2, OUT-EV, and OUT-EC = “L” level.
*3:CTL signal is “L” level after resetting microprocessor (CTL = “HiZ” until microprocessor is reset) .
*4:VIN and VCC rises by connecting AC adapter.
*5:Charging voltage data is set by microprocessor.
*6:CTL signal is turned on after data setup time (t_{DS}) .
*7:Upon detecting CTL signal at “H” level, decoder data is set after data output delay time (t_{D0}) .
*8:Shift to constant current mode. OUT-EA1, OUT-EA2, and OUT-EV = “H” level.
*9:Shift from BATT1 constant current charge control to constant voltage change control. OUT-EC = “H” level, OUT-EV = “L” level.
*10:Battery2 (almost empty) is inserted. Controlled by FB4 (BATT2 constant current charge) . OUT-EC = “L” level.
*11:With CTL signal “L” level, OUT-EA1, OUT-EA2, OUT-EV, and OUT-EC = “L” level.
*12:Data set after turning off CTL signal.
*13:After CTL signal set at “L” level, CTL signal reactivation time (t_{RCTL} = 2 ms (Min)) or longer time is required.

8. Sequence of Normal Power Supply Shutoff and Completion of Charging

<Battery 1 is removed and then AC adapter is removed.>



*1:With CTL signal “L” level, OUT-EA1, OUT-EA2, OUT-EV, and OUT-EC = “L” level.

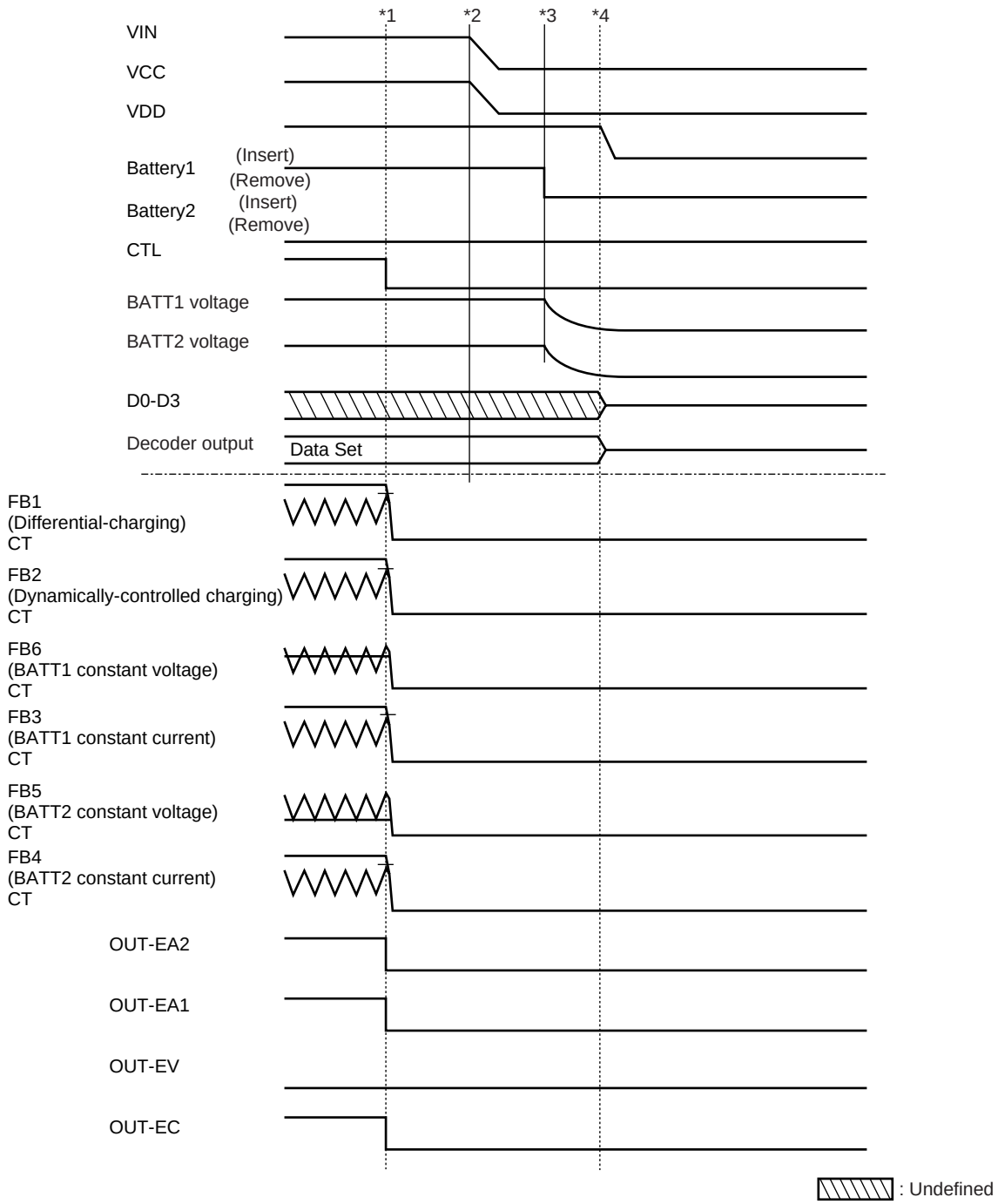
*2:Voltages of BATT1 and BATT2 fall by removing Battery 1.

*3:VIN and VCC power supply falls by removing AC adapter.

*4:VDD falls. CTL, OUT-EA1, OUT-EA2, OUT-EV, and OUT-EC = HiZ

9. Sequence of Normal Power Supply Shutoff and Completion of Charging

< AC adapter is removed and then Battery 1 is removed.>



*1:With CTL signal “L” level, OUT-EA1, OUT-EA2, OUT-EV, and OUT-EC = “L” level.

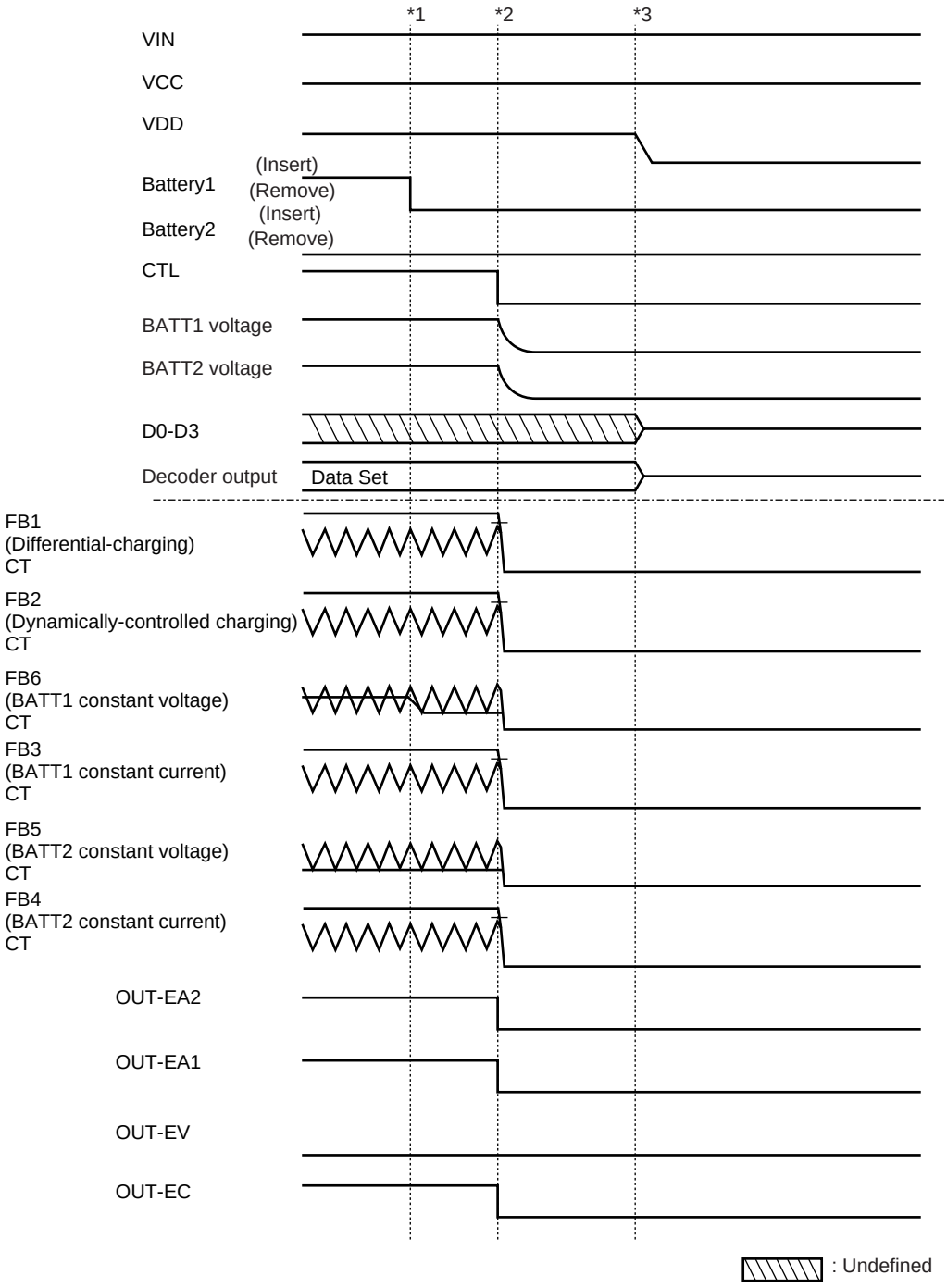
*2:VIN and VCC power falls by removing AC adapter.

*3:Voltages of BATT1 and BATT2 falls by removing Battery 1.

*4:VDD falls. CTL, OUT-EA1, OUT-EA2, OUT-EV, and OUT-EC = HiZ

10. Sequence of Normal Power Supply Shutoff and Completion of Charging

< Battery 1 and 2 are removed during charge operation.>



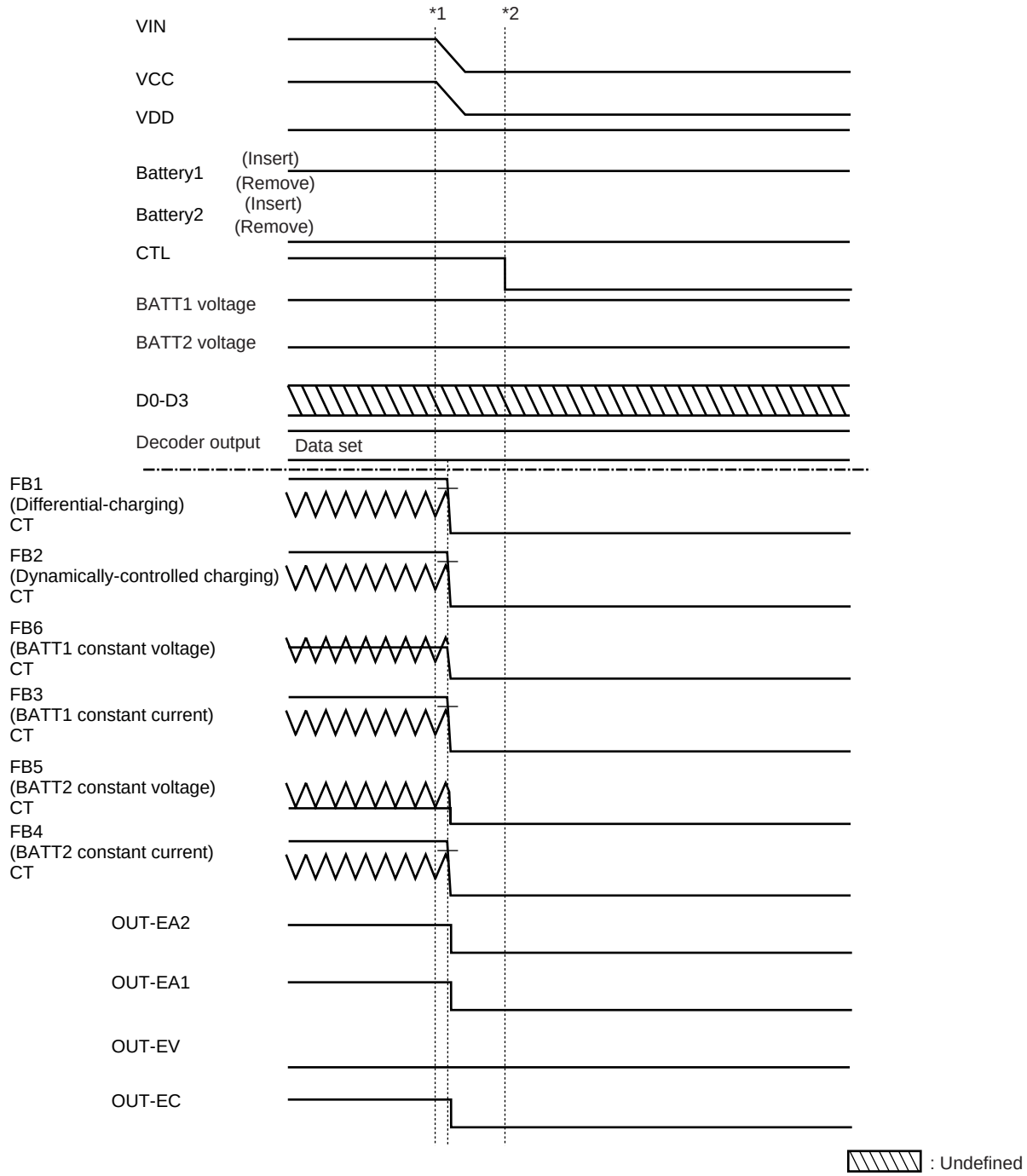
*1:Stopping charge operation by removing Battery 1.

*2:With CTL signal “L” level, OUT-EA1, OUT-EA2, OUT-EV, and OUT-EC=“L” level.

*3:VDD falls. CTL, OUT-EA1, OUT-EA2, OUT-EV, and OUT-EC =HiZ

11. Sequence of Normal Power Supply Shutoff and Completion of Charging

<AC adapter is removed during charge operation.>

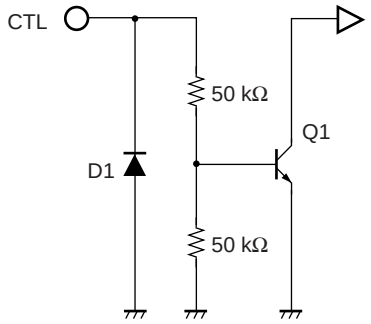


*1:Fall of VIN and VCC voltages due to removal of AC adapter. OUT-EA1, OUT-EA2, OUT-EV, and OUT-EC = “L” level.

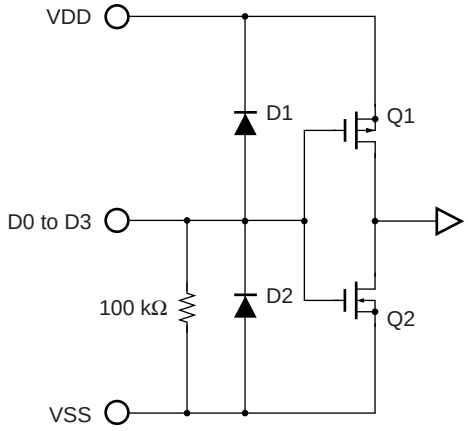
*2:CTL signal is “L” level.

■ EQUIVALENT CIRCUIT DIAGRAM FOR CTL, D0 to D3, OUT-EA1, EA2, EV, EC TERMINALS

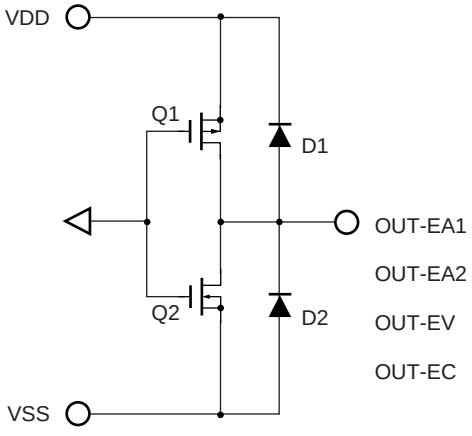
- CTL terminal



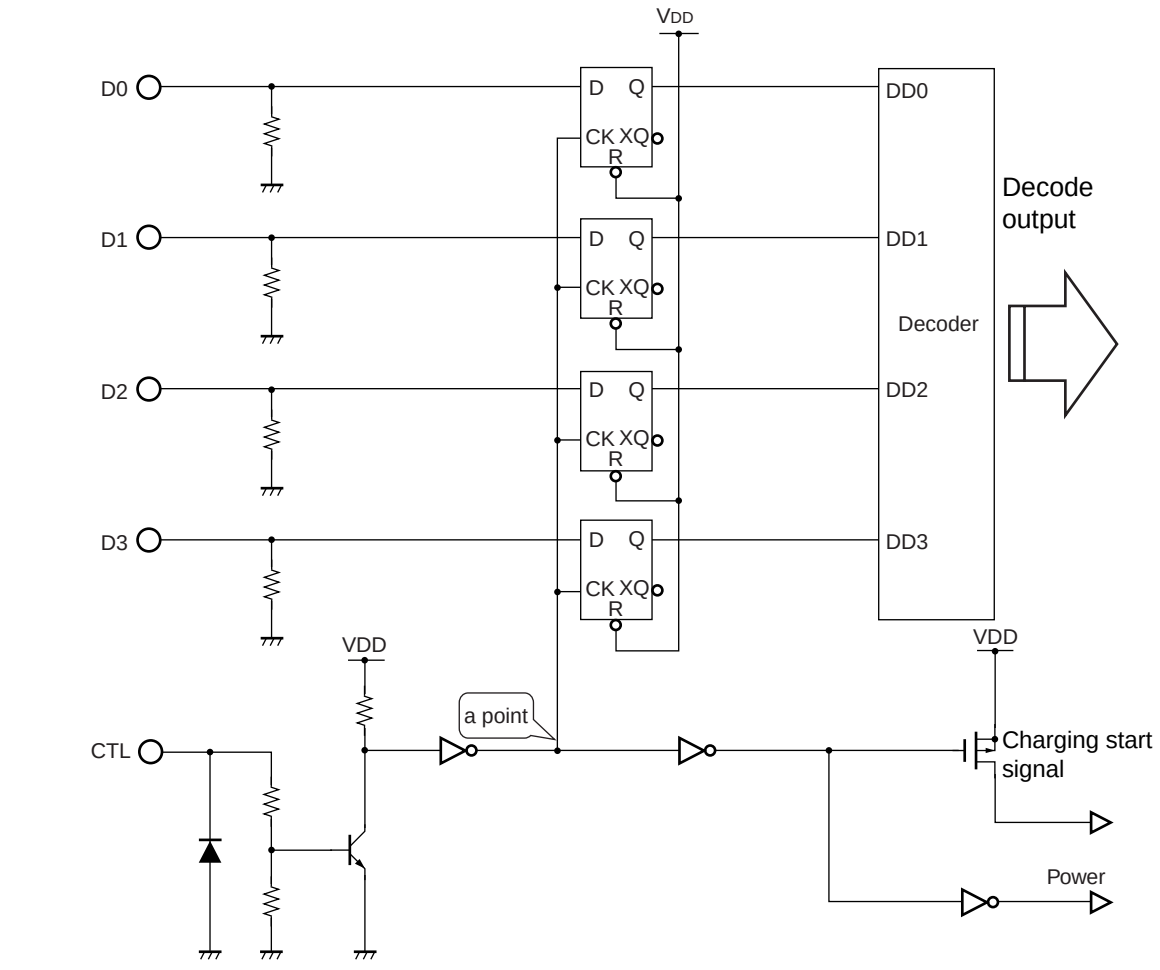
- D0 to D3 terminals

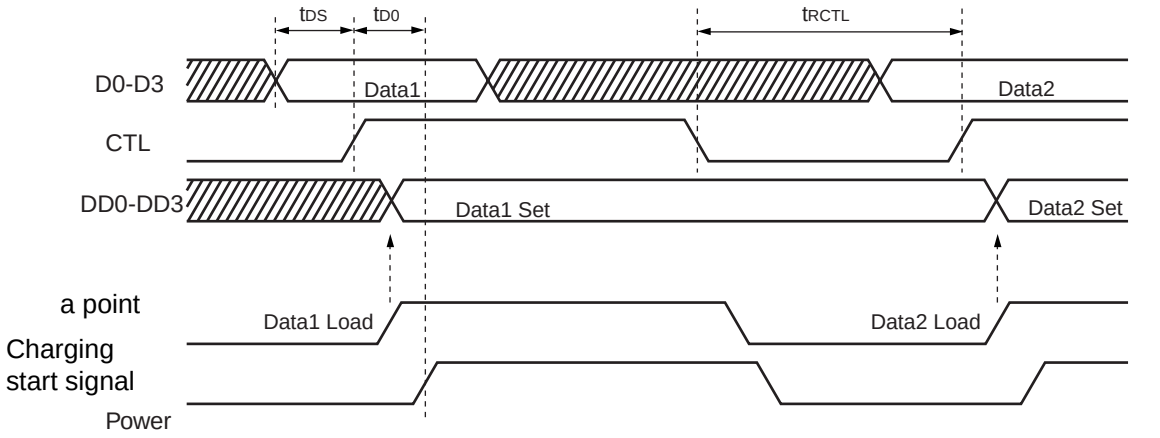


- OUT-EA1 to OUT-EC terminal



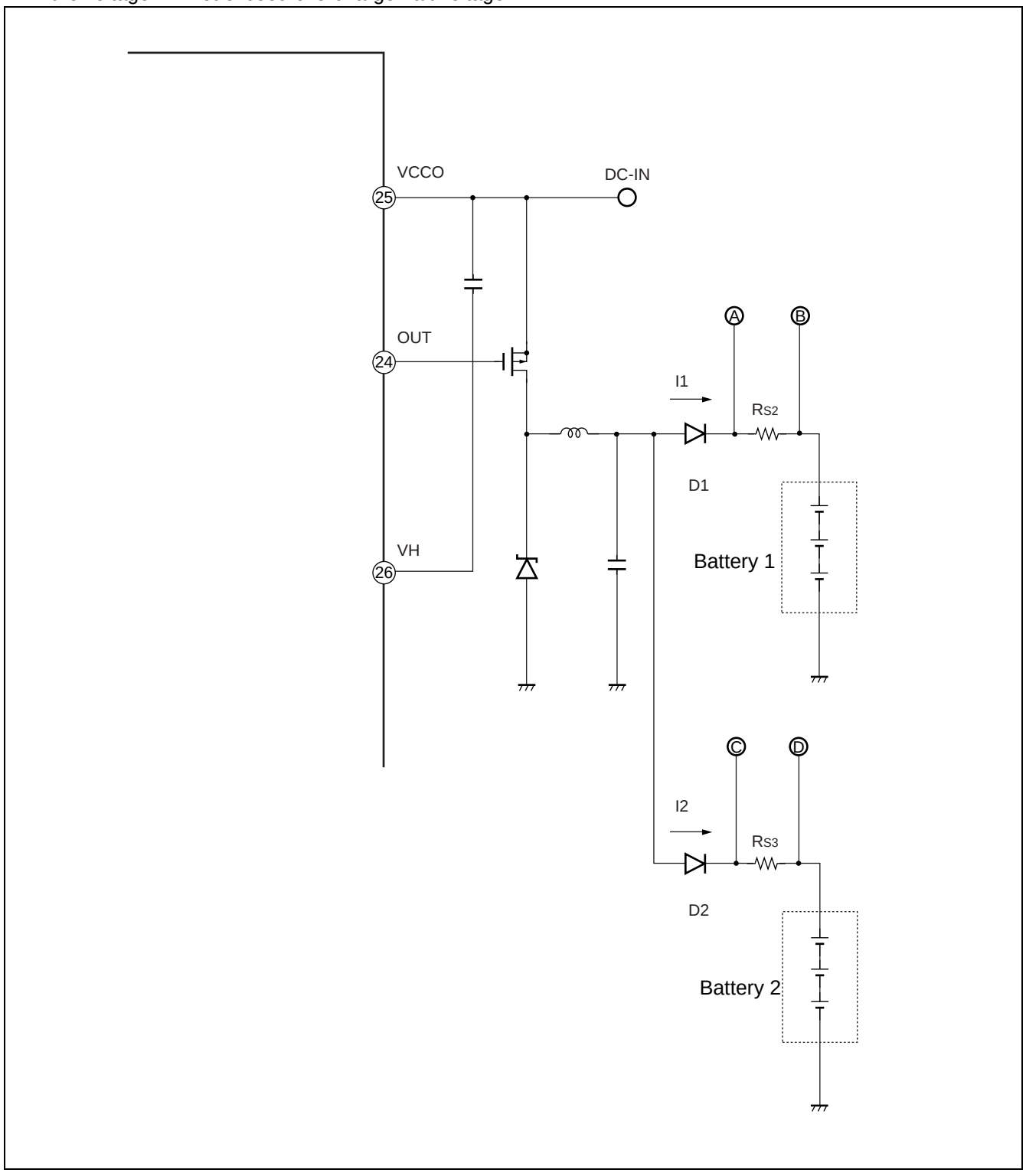
■ EQUIVALENT CIRCUIT DIAGRAM FOR DECODER BLOCK



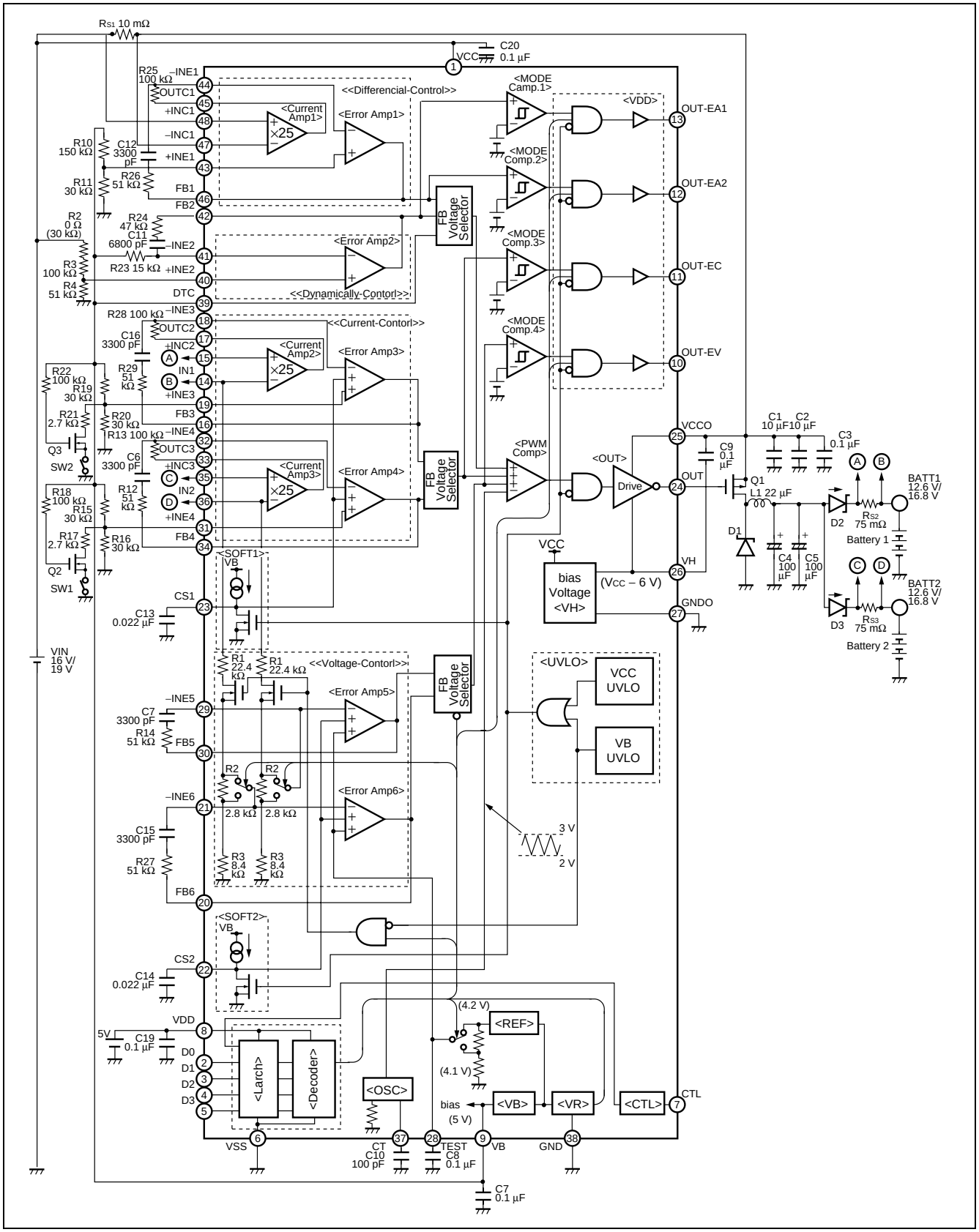


■ NOTES ON USING REVERSE CURRENT PROTECTION DIODE

- If charging currents (I1 and I2) are imbalance under constant voltage control, voltages are controlled on the basis of a lower battery voltage. Therefore, battery voltage on either side is higher for the potential occurring on reverse current protection diodes (D1 and D2) and sense resistors (R_{S2} and R_{S3}).
- Take notes and voltage and current characteristics of reverse current protection diodes (D1 and D2) so that the voltage will not exceed overcharge halt voltage.



■ APPLICATION CIRCUIT EXAMPLE



■ PARTS LIST

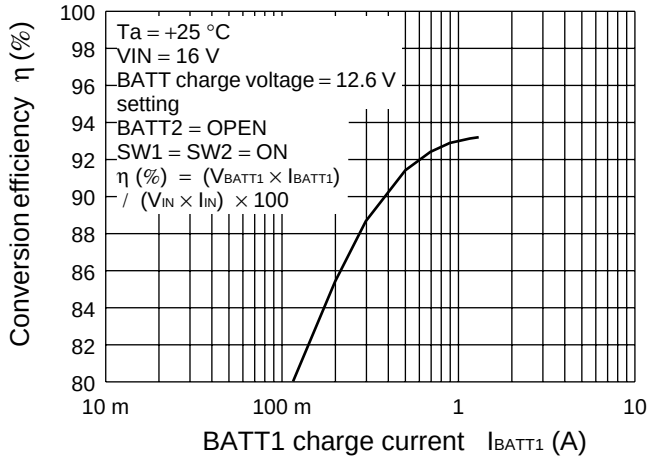
COMPONENT	ITEM	SPECIFICATION		VENDOR	PARTS No.
Q1 Q2, Q3	FET FET	VDS = 30 V, Qg = 43 nC (Typ) VDS = 60 V		TOSHIBA VISHAY SILICONIX	TPC8102 2N7002E
D1 to D3	Diode	With VF = 0.42 V (Max) and IF = 3 A		ROHM	RB053L-30
L1	Inductor	22 µH	3.5 A, 31.6 mΩ	TDK	SLF12565T-220M3R5
C1, C2	Ceramics Condenser	10 µF	25 V	TDK	C3225JF1E106Z
C3	Ceramics Condenser	0.1 µF	50 V	TDK	C1608JB1H104K
C4, C5	Electrolytic Condenser	100 µF	25 V	SANYO	25CV100AX
C6, C7	Ceramics Condenser	3300 pF	50 V	MURATA	GRM39B322K50
C8, C9	Ceramics Condenser	0.1 µF	50 V	TDK	C1608JB1H104K
C10	Ceramics Condenser	100 pF	50 V	TDK	C1608CH1H101J
C11	Ceramics Condenser	6800 pF	50 V	MURATA	GRM39B682K50
C12, C15, C16	Ceramics Condenser	3300 pF	50 V	MURATA	GRM39B332K50
C13,C14	Ceramics Condenser	0.022 µF	50 V	TDK	C1608JB1H223K
C17, C19, C20	Ceramics Condenser	0.1 µF	50 V	TDK	C1608JB1H104K
R_{S1}	Resistor	10 mΩ	1 %	KOA	SL1TE10mF
R2	Jumper	0 Ω	50 mΩ Max	KOA	RK73ZJ1J
	Resistor*	30 kΩ	0.5 %	ssm	RR0816P303D
R3	Resistor	100 kΩ	0.5 %	ssm	RR0816P104D
R4	Resistor	51 kΩ	0.5 %	ssm	RR0816P513D
R_{S2},R_{S3}	Resistor	75 mΩ	1 %	KOA	SL1TE75mF
R10	Resistor	150 kΩ	0.5 %	ssm	RR0816P154D
R11	Resistor	30 kΩ	0.5 %	ssm	RR0816P303D
R12, R14	Resistor	51 kΩ	0.5 %	ssm	RR0816P513D
R13	Resistor	100 kΩ	0.5 %	ssm	RR0816P104D
R15, R16	Resistor	30 kΩ	0.5 %	ssm	RR0816P303D
R17, R21	Resistor	2.7 kΩ	0.5 %	ssm	RR0816P272D
R18, R22	Resistor	100 kΩ	0.5 %	ssm	RR0816P104D
R19, R20	Resistor	30 kΩ	0.5 %	ssm	RR0816P303D
R23	Resistor	15 kΩ	0.5 %	ssm	RR0816P153D
R24	Resistor	47 kΩ	0.5 %	ssm	RR0816P473D
R25, R28	Resistor	100 kΩ	0.5 %	ssm	RR0816P104D
R26, R27, R29	Resistor	51 kΩ	0.5 %	ssm	RR0816P513D

* : 30 kΩ for 4 cells

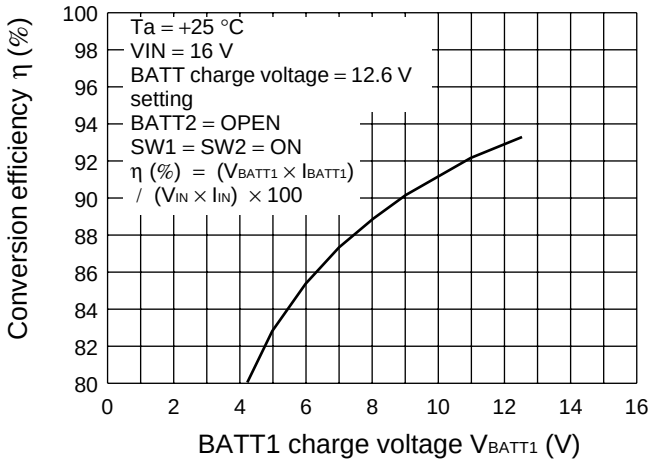
Notes : TOSHIBA : Toshiba Corporation
ROHM : ROHM CO., LTD.
TDK : TDK Corporation
SANYO : SANYO Electric Co., Ltd.
MURATA : Murata Manufacturing Co., Ltd.
KOA : KOA Corporation
ssm : SUSUMU Co., Ltd.

■ REFERENCE DATA

Conversion efficiency – Charge current
(constant voltage mode Li3C42)

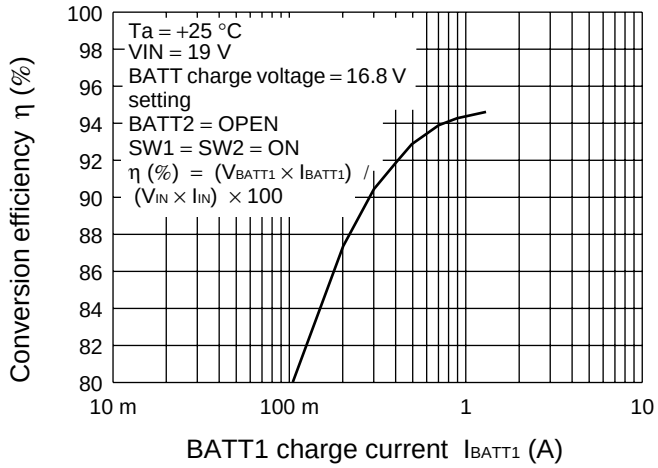


Conversion efficiency – Charge current
(constant current mode Li3C42)

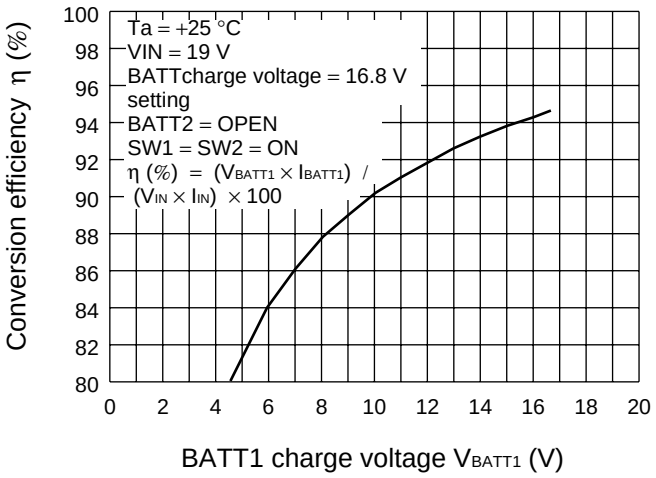


(Continued)

Conversion efficiency – Charge current
(constant current mode Li4C42)

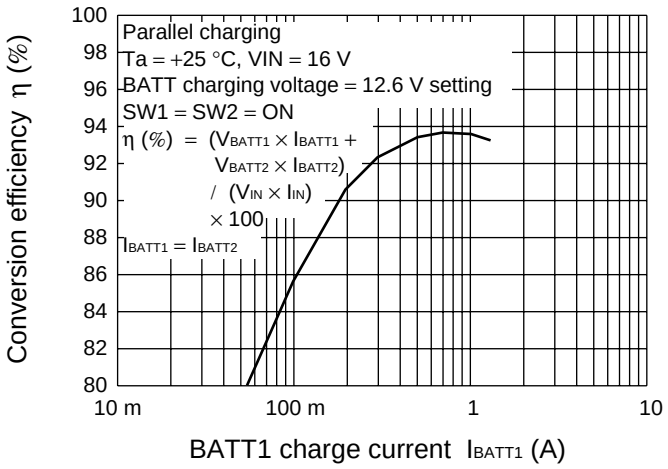


Conversion efficiency – Charge current
(constant current mode Li4C42)

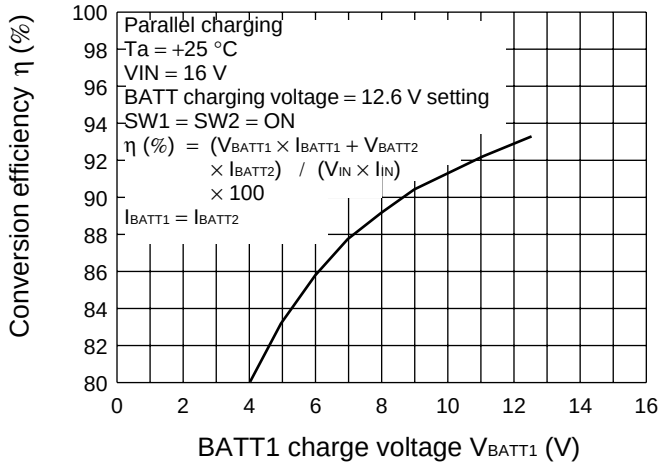


(Continued)

Conversion efficiency – Charge current
(constant voltage mode Li3C42)

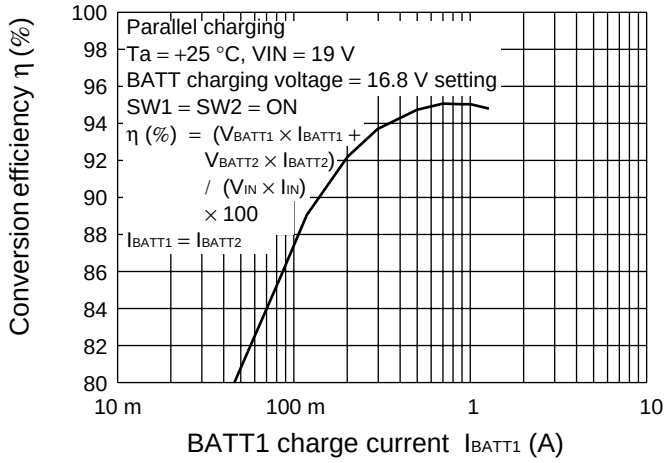


Conversion efficiency – Charge current
(constant current mode Li3C42)

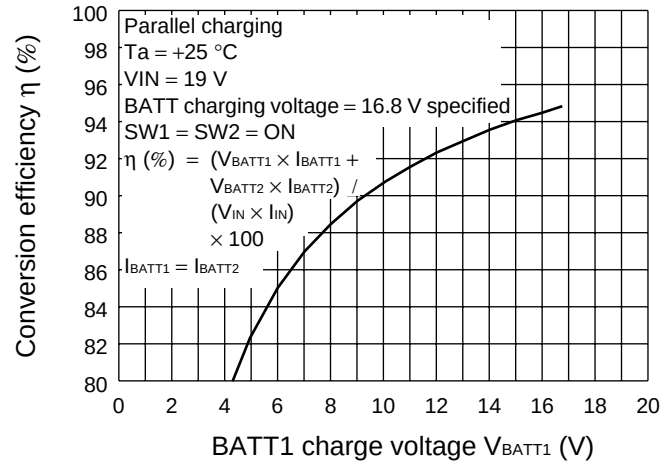


(Continued)

Conversion efficiency – Charge current
(constant voltage mode Li4C42)

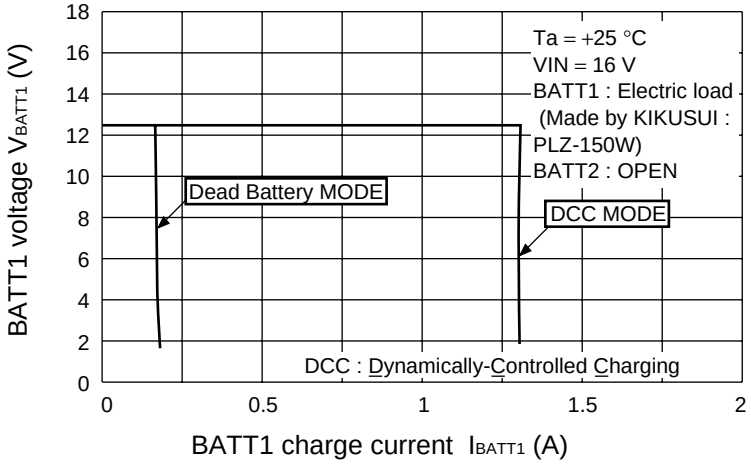


Conversion efficiency – Charge current
(constant current mode Li4C42)

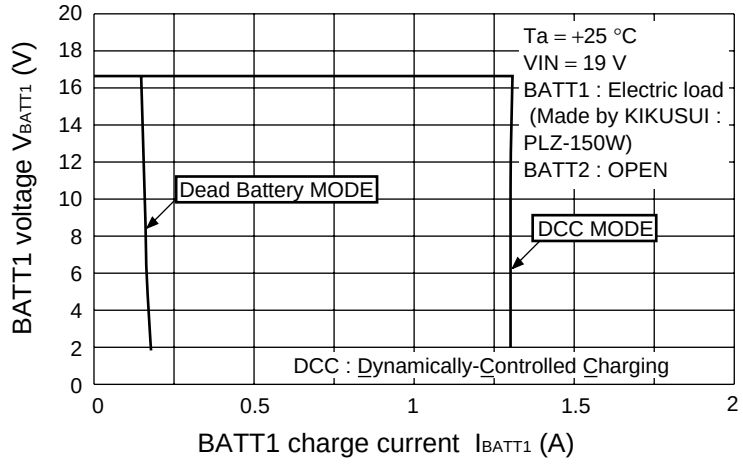


(Continued)

BATT voltage – BATT charge current
(Li3C42)

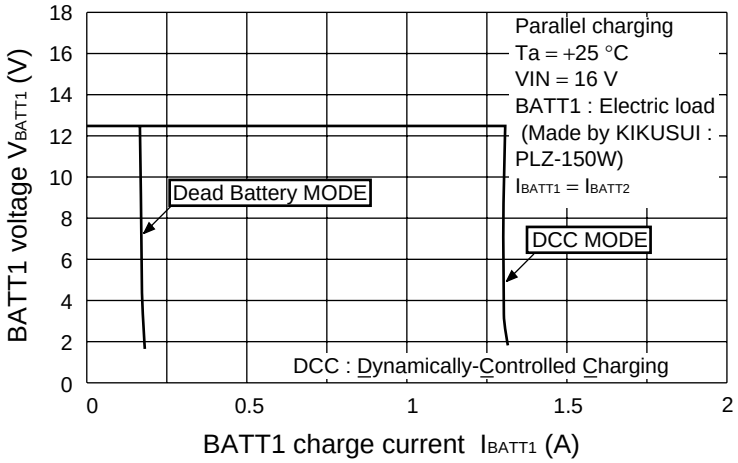


BATT voltage – BATT charge current
(Li4C42)

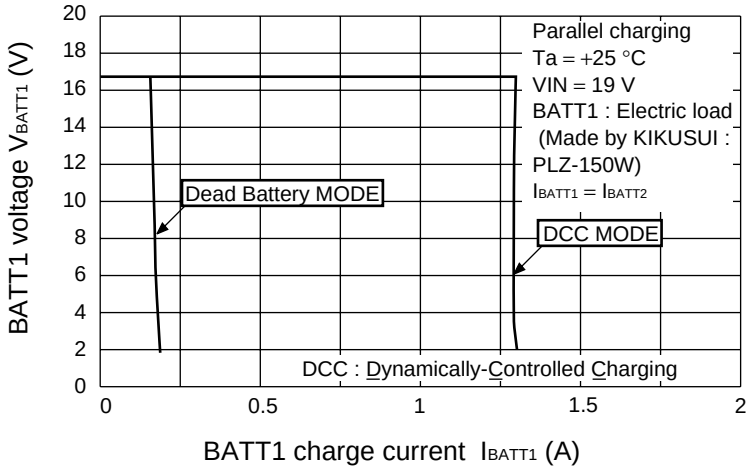


(Continued)

BATT voltage – BATT charge current
(Li3C42)

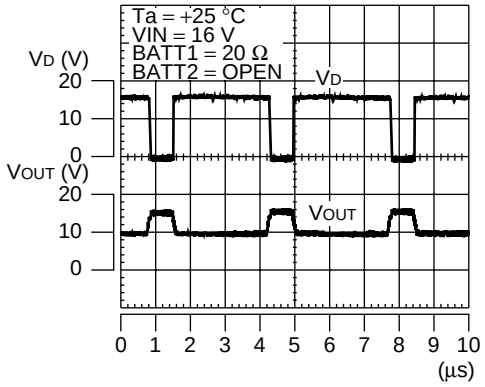


BATT voltage – BATT charge current
(Li4C42)

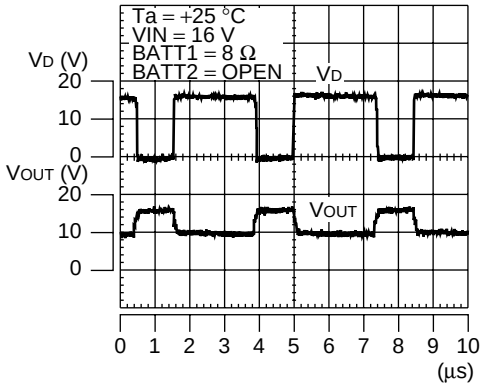


(Continued)

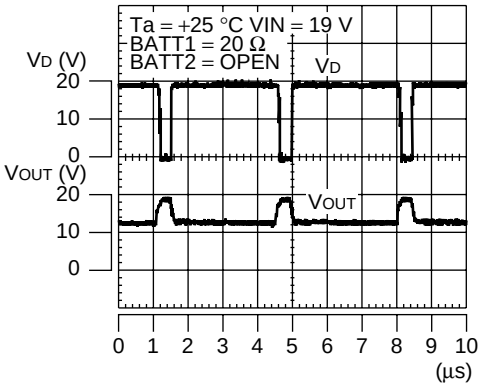
Switching waveform voltage mode (Li3C42)



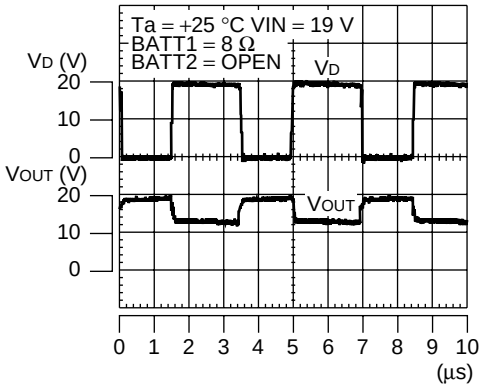
Switching waveform current mode (Li3C42)



Switching waveform voltage mode (Li4C42)



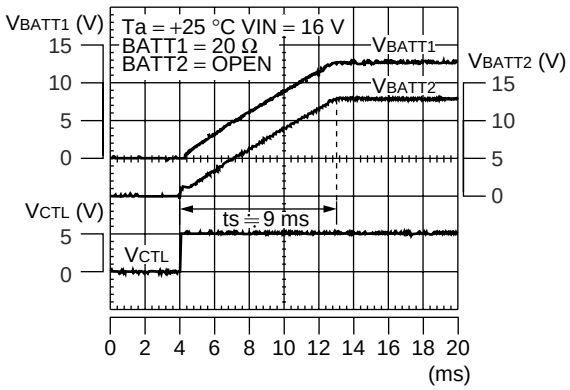
Switching waveform current mode (Li4C42)



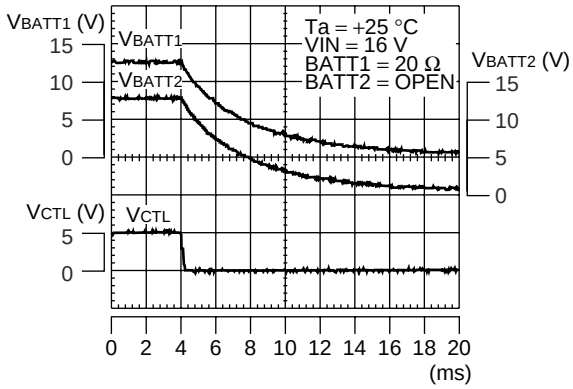
(Continued)

(Continued)

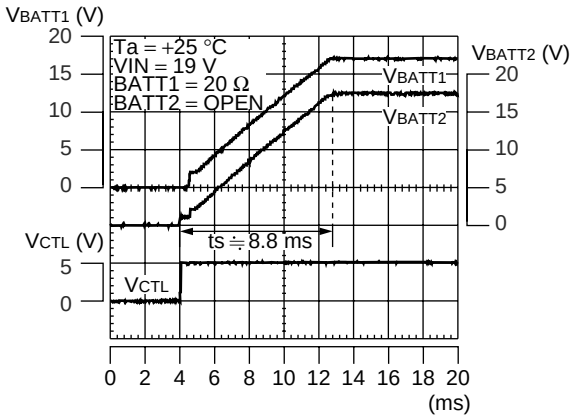
Soft-start operation waveform voltage mode (Li3C42)



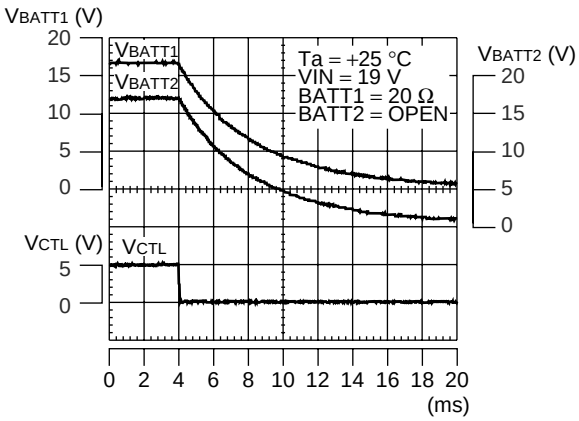
Discharge operation waveform current mode (Li3C42)



Soft-start operation waveform voltage mode (Li4C42)



Discharge operation waveform current mode (Li4C42)



■ NOTES ON USE

- **Design ground lines on printed circuit with regard to common impedance.**
- **Be sure to take measures against electrostatics.**
  - Use static protection products or conductive containers for storing semiconductor devices.
  - Use conductive bag or conductive containers for storing or carrying printed boards with semiconductor devices mounted.
  - Be sure to connect ground lines of work table, tools and measurement devices.
  - Establish a ground for human body of a worker using a resistor of 250 kΩ to 1 MΩ serially connected between the body and the ground.
- **Do not apply a negative voltage.**
  - If a negative voltage lower than -0.3V, a parasitic transistor may appear on LSI, causing malfunction.

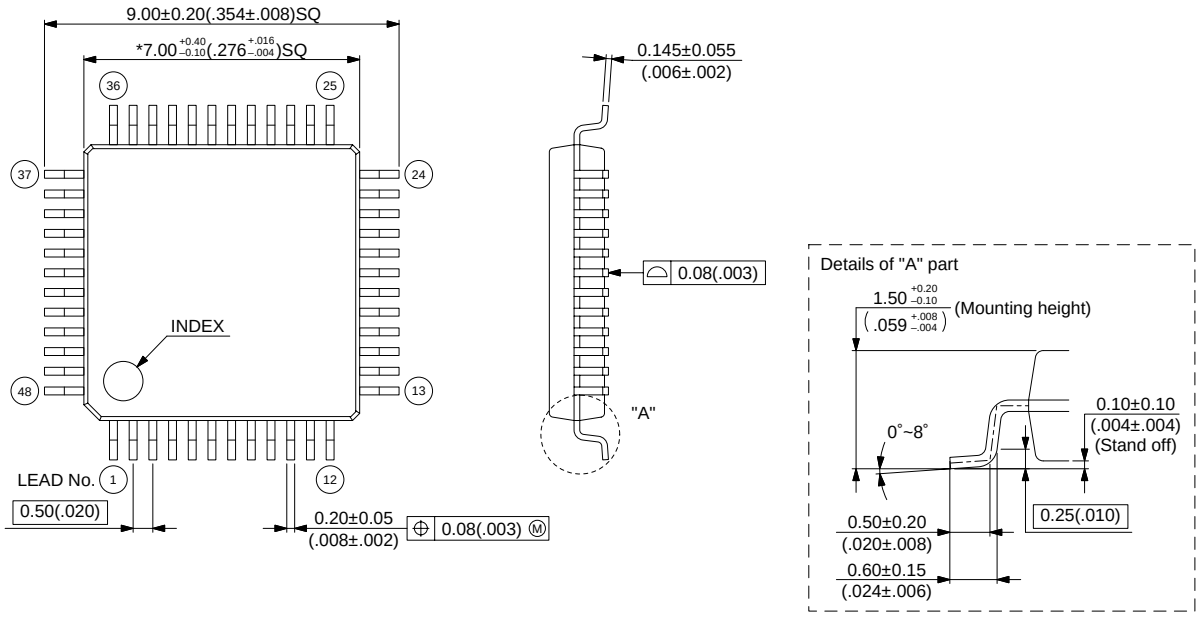
■ ORDERING INFORMATION

Part number	Package	Remarks
MB3879PFV	48-pin Plastic LQFP (FPT-48P-M05)	

■ PACKAGE DIMENSION

48-pin Plastic LQFP
(FPT-48P-M05)

Note 1) * : These dimensions include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.



© 2002 FUJITSU LIMITED F48013S-c-5-9

Dimensions in mm (inches)

FUJITSU LIMITED

All Rights Reserved.

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document are presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).
Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.

F0209
© FUJITSU LIMITED Printed in Japan