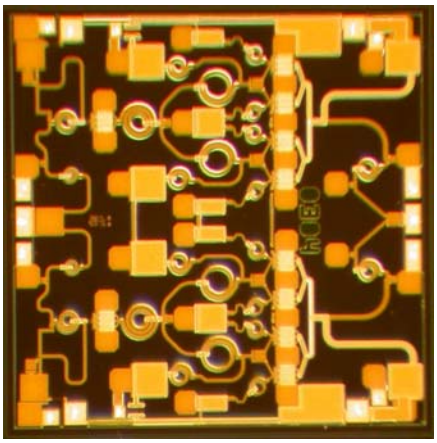
Amplifier, Power, 2.0 W 6.5—9.5 GHz

MAAPGM0064-DIE
Rev —
Preliminary Information

Features

- 2 Watt Saturated Output Power Level
- Variable Drain Voltage (4-10V) Operation
- MSAG™ Process
- High Performance Ceramic Bolt Down Package



Description

The MAAPGM0064-DIE is a 2-stage 2 W power amplifier with on-chip bias networks. This product is fully matched to 50 ohms on both the input and output. It can be used as a power amplifier stage or as a driver stage in high power applications.

Each device is 100% RF tested to ensure performance compliance. The part is fabricated using M/A-COM's GaAs Multifunction Self-Aligned Gate Process.

M/A-COM's MSAG™ process features robust silicon-like manufacturing processes, planar processing of ion implanted transistors and multiple implant capability enabling power, low-noise, switch and digital FETs on a single chip. The use of refractory metals and the absence of platinum in the gate metal formulation prevents hydrogen poisoning when employed in hermetic packaging.

Primary Applications

- Multiple Band Point-to-Point Radio
- SatCom
- ISM Band

Also Available in:

		SAMPLES	
Description	**Ceramic Package**	**Sample Board (Die)**	**Mechanical Sample (Die)**
Part Number	MAAPGM0064	MAAP-000064-SMB004	Not Available

Electrical Characteristics: T_B = 40°C[1], Z_0 = 50 Ω, V_{DD} = 8V, I_{DQ} ≈ 600 mA[2], P_{in} = 18 dBm, R_G ≈ 120Ω

Parameter	Symbol	Typical	Units
Bandwidth	f	6.5-9.5	GHz
Output Power	POUT	34.5	dBm
Power Added Efficiency	PAE	30	%
1-dB Compression Point	P1dB	32	dBm
Small Signal Gain	G	20	dB
Input VSWR	VSWR	1.8:1	
Output VSWR	VSWR	3.0:1	
Gate Supply Current	I_{GG}	< 5	mA
Drain Supply Current	I_{DD}	< 1	mA
Noise Figure	NF	9.5	dB
2nd Harmonic	2f	-20	dBc
3rd Harmonic	3f	-45	dBc
Output Third Order Intercept	OTOI	41	dBm
3rd Order Intermodulation Distortion, Single Carrier Level = 20 dBm	IM3	-10	dBm
5th Order Intermodulation Distortion, Single Carrier Level = 20 dBm	IM5	-25	dBm

1. T_B = MMIC Base Temperature
2. Adjust V_{GG} between –2.6 and –1.2V to achieve specified Idq.

• **North America** Tel: 800.366.2266 / Fax: 978.366.2266
• **Europe** Tel: 44.1908.574.200 / Fax: 44.1908.574.300
• **Asia/Pacific** Tel: 81.44.844.8296 / Fax: 81.44.844.8298

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Maximum Ratings [3]

Parameter	Symbol	Absolute Maximum	Units
Input Power	P_{IN}	23.0	dBm
Drain Supply Voltage	V_{DD}	+12.0	V
Gate Supply Voltage	V_{GG}	-3.0	V
Quiescent Drain Current (No RF, 40% Idss)	I_{DQ}	950	mA
Quiescent DC Power Dissipated (No RF)	P_{DISS}	7.9	W
Junction Temperature	T_J	170	°C
Storage Temperature	T_{STG}	-55 to +150	°C

3. Operation beyond these limits may result in permanent damage to the part.

Recommended Operating Conditions[4]

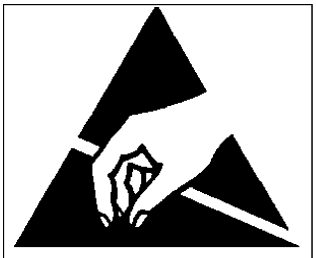
Characteristic	Symbol	Min	Typ	Max	Unit
Drain Supply Voltage	V_{DD}	4.0	8.0	10.0	V
Gate Supply Voltage	V_{GG}	-2.4	-2.0	-1.3	V
Input Power	P_{IN}		18.0	21.0	dBm
Thermal Resistance	Θ_{JC}		12.4		°C/W
Package Base Temperature	T_B			Note 5	°C

4. Operation outside of these ranges may reduce product reliability.
5. MMIC Base Temperature = 170°C — Θ_{JC}* V_{DD} * I_{DQ}

Operating Instructions

This device is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply V_{GG} = -2.7 V, V_{DD}= 0 V.
2. Ramp V_{DD} to desired voltage, typically 8.0 V.
3. Adjust V_{GG} to set I_{DQ}, (approximately @ –2.0 V).
4. Set RF input.
5. Power down sequence in reverse. Turn V_{GG} off last.



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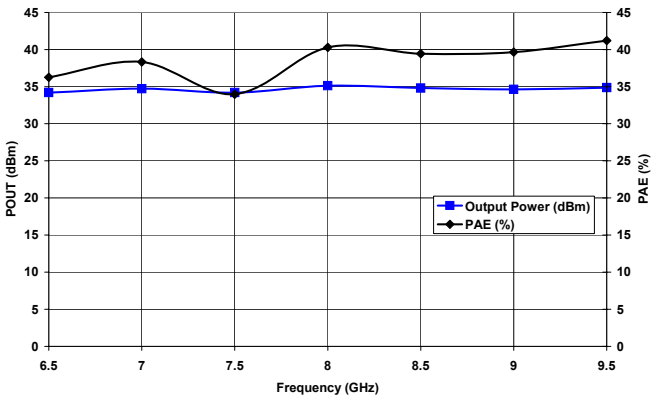

Figure 1. Output Power and Power Added Efficiency vs. Frequency @ P_{IN}=18.0 dBm, V_{DD}=8V, I_{DQ}=600 mA

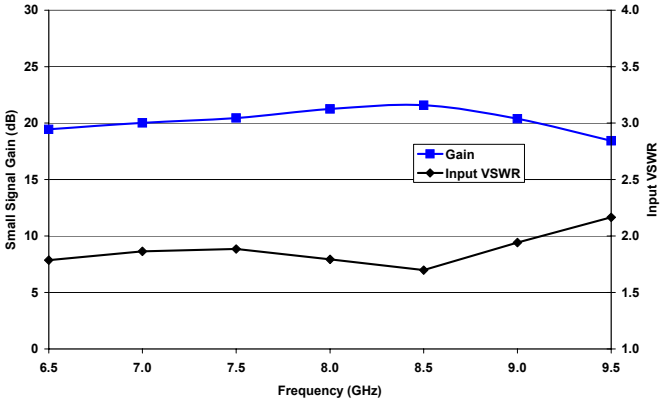

Figure 2. Gain and Input VSWR vs. Frequency (V_{DD}=8 V, I_{DQ}=600 mA)

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Mechanical Information

Chip Size: 2.95 x 2.95 x 0.075 mm (116 x 116 x 3 mils)

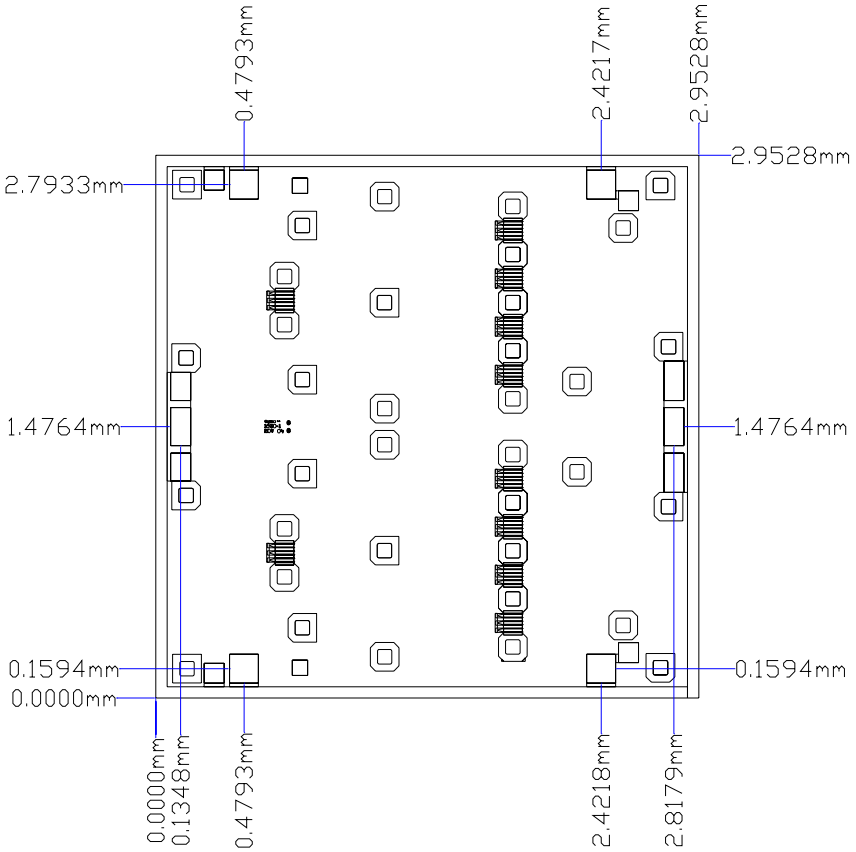

Figure 3. Die Layout

Bond Pad Dimensions

Pad	Size (µm)	Size (mils)
RF In and Out	100 x 200	4 x 8
DC Drain Supply Voltage VDD	200 x 150	8 x 6
DC Gate Supply Voltage VGG	150 x 150	6 x 6

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Assembly and Bonding Diagram

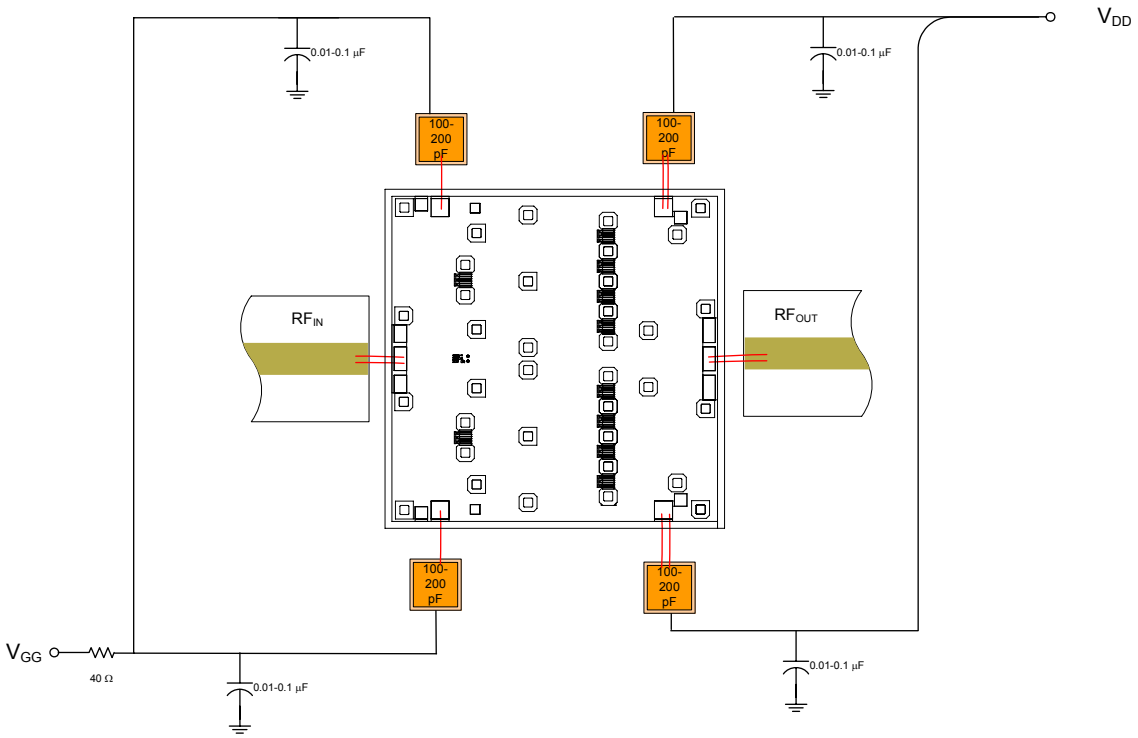


Figure 4. Recommended operational configuration. Wire bond as shown.

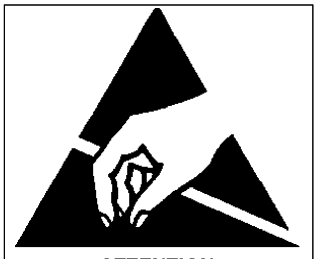
Die Handling:

Refer to Application Note AN3016.

Assembly Instructions:

Die Attach: Use AuSn (80/20) 1 mil. preform solder. Limit time @ 310 °C to less than 7 minutes. Refer to Application Note AN3017 for more detailed information.

Wirebonding: Bond @ 160 °C using standard ball or thermal compression wedge bond techniques. For DC pad connections, use either ball or wedge bonds. For best RF performance, use wedge bonds of shortest length, although ball bonds are also acceptable.



Biasing Note: Must apply negative bias to V_{GG} before applying positive bias to V_{DD} to prevent damage to amplifier.

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