

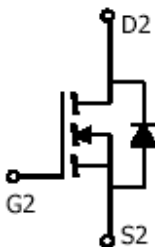
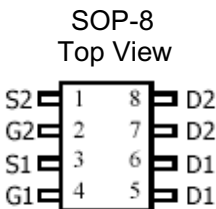
ELM14600AA Complementary Enhancement Mode Power MOS FET

General Description

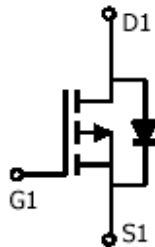
The ELM14600AA uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs form a high-speed power inverter, suitable for a multitude of applications.

Features

n-channel	p-channel
$V_{DS} (V) = 30V$	-30V
$I_D = 6.9A$	-5A
$R_{DS(ON)}$	
< 27m Ω ($V_{GS} = 10V$)	< 49m Ω ($V_{GS} = -10V$)
< 32m Ω ($V_{GS} = 4.5V$)	< 64m Ω ($V_{GS} = -4.5V$)
< 50m Ω ($V_{GS} = 2.5V$)	< 120m Ω ($V_{GS} = -2.5V$)



n-channel



p-channel

Absolute Maximum Ratings $T_A=25^{\circ}C$ unless otherwise noted				
Parameter	Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage	V_{DS}	30	-30	V
Gate-Source Voltage	V_{GS}	± 12	± 12	V
Continuous Drain Current ^A	$T_A=25^{\circ}C$	6.9	-5	A
	$T_A=70^{\circ}C$	5.8	-4.2	
Pulsed Drain Current ^B	I_{DM}	40	-30	
Power Dissipation	$T_A=25^{\circ}C$	2	2	W
	$T_A=70^{\circ}C$	1.44	1.44	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^{\circ}C$

Thermal Characteristics: n-channel and p-channel					
Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$t \leq 10s$	$R_{\theta JA}$	48	62.5	$^{\circ}C/W$
Maximum Junction-to-Ambient ^A	Steady-State		74	110	$^{\circ}C/W$
Maximum Junction-to-Lead ^C	Steady-State	$R_{\theta JL}$	35	40	$^{\circ}C/W$

p-channel MOSFET Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-24V, V _{GS} =0V T _J =55°C			-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±12V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-0.7	-1	-1.4	V
I _{D(ON)}	On state drain current	V _{GS} =-4.5V, V _{DS} =-5V	-25			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-5A T _J =125°C		42.5	49	mΩ
		V _{GS} =-4.5V, I _D =-4A		54	64	mΩ
		V _{GS} =-2.5V, I _D =-1A		80	120	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-5A	7	11		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.75	-1	V
I _S	Maximum Body-Diode Continuous Current				-3	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-15V, f=1MHz		952		pF
C _{oss}	Output Capacitance			103		pF
C _{rss}	Reverse Transfer Capacitance			77		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		5.9		Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =-4.5V, V _{DS} =-15V, I _D =-5A		9.5		nC
Q _{gs}	Gate Source Charge			2		nC
Q _{gd}	Gate Drain Charge			3.1		nC
t _{D(on)}	Turn-On Delay Time	V _{GS} =-10V, V _{DS} =-15V, R _L =3Ω, R _{GEN} =6Ω		12		ns
t _r	Turn-On Rise Time			4		ns
t _{D(off)}	Turn-Off Delay Time			37		ns
t _f	Turn-Off Fall Time			12		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-5A, dI/dt=100A/μs		21		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-5A, dI/dt=100A/μs		13		nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any a given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D: The static characteristics in Figures 1 to 6,12,14 are obtained using 80 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

n-channel MOSFET Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=24\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^{\circ}\text{C}$			1 5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 12\text{V}$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	0.7	1	1.4	V
$I_{D(ON)}$	On state drain current	$V_{GS}=4.5\text{V}$, $V_{DS}=5\text{V}$	25			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=6.9\text{A}$ $T_J=125^{\circ}\text{C}$		22.6 33	27 40	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$, $I_D=6.0\text{A}$		27	32	$\text{m}\Omega$
		$V_{GS}=2.5\text{V}$, $I_D=5\text{A}$		42	50	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=5\text{A}$	12	16		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$		0.71	1	V
I_S	Maximum Body-Diode Continuous Current				3	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=15\text{V}$, $f=1\text{MHz}$		858		pF
C_{oss}	Output Capacitance			110		pF
C_{rss}	Reverse Transfer Capacitance			80		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		1.24		Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	$V_{GS}=4.5\text{V}$, $V_{DS}=15\text{V}$, $I_D=6.9\text{A}$		9.6		nC
Q_{gs}	Gate Source Charge			1.65		nC
Q_{gd}	Gate Drain Charge			3		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}$, $V_{DS}=15\text{V}$, $R_L=2.2\Omega$, $R_{GEN}=6\Omega$		5.7		ns
t_r	Turn-On Rise Time			13		ns
$t_{D(off)}$	Turn-Off DelayTime			37		ns
t_f	Turn-Off Fall Time			4.2		ns
t_{rr}	Body Diode Reverse Recovery time	$I_F=5\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		15.5		ns
Q_{rr}	Body Diode Reverse Recovery charge	$I_F=5\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		7.9		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The value in any a given application depends on the user's specific board design. The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using 80 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The SOA curve provides a single pulse rating.

TYPICAL P-CHANNEL ELECTRICAL AND THERMAL CHARACTERISTICS

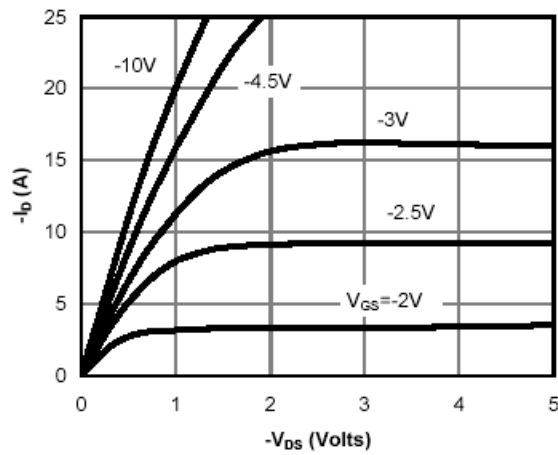


Fig 1: On-Region Characteristics

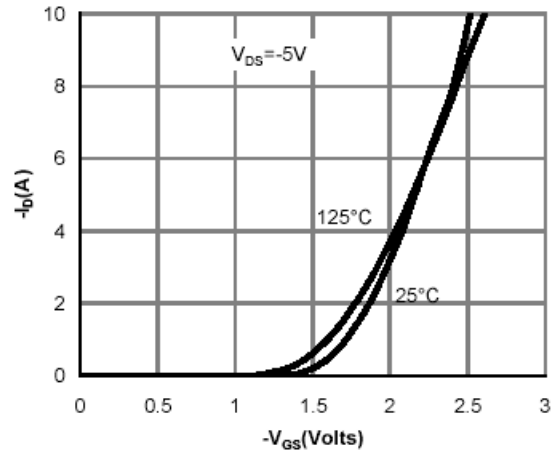


Figure 2: Transfer Characteristics

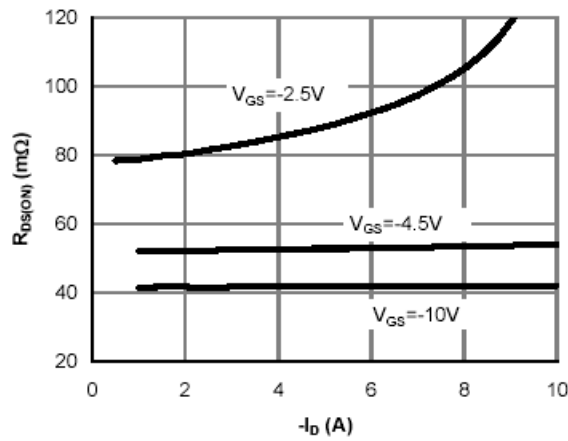


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

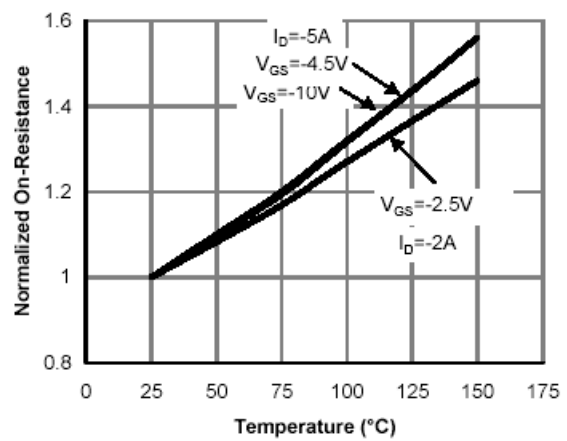


Figure 4: On-Resistance vs. Junction Temperature

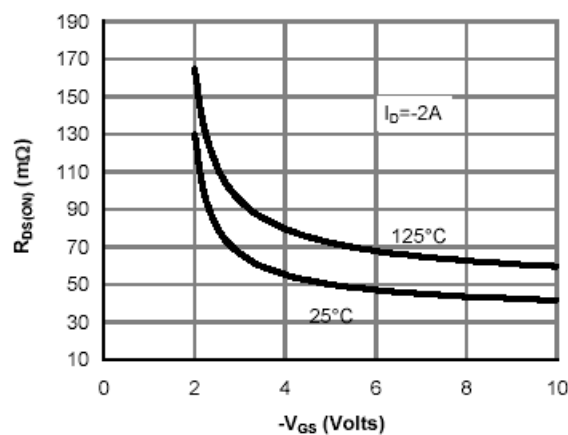


Figure 5: On-Resistance vs. Gate-Source Voltage

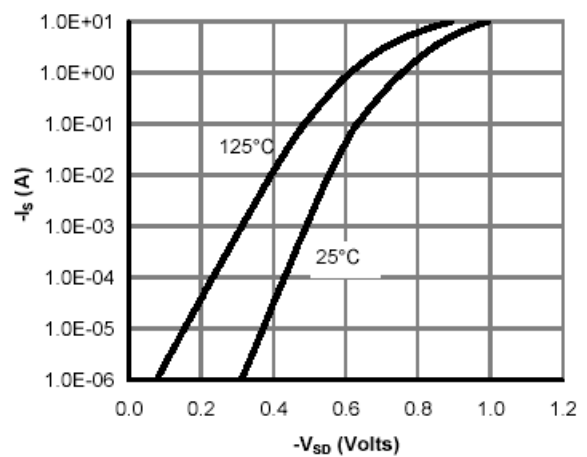


Figure 6: Body-Diode Characteristics

TYPICAL P-CHANNEL ELECTRICAL AND THERMAL CHARACTERISTICS

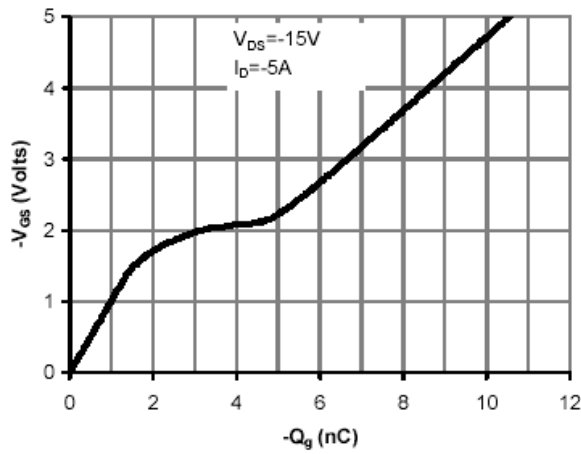


Figure 7: Gate-Charge Characteristics

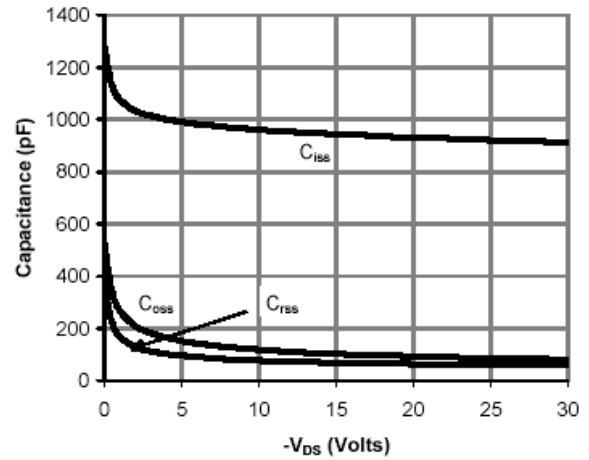


Figure 8: Capacitance Characteristics

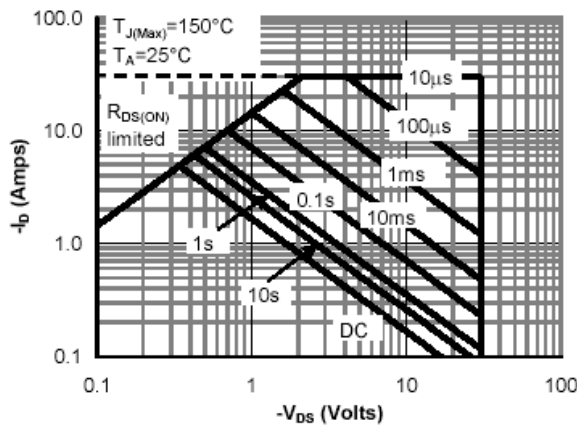


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

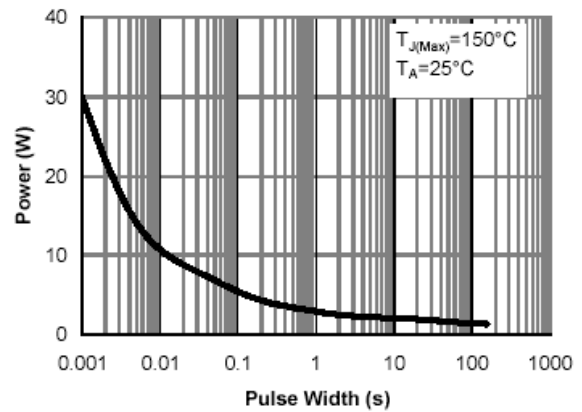


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

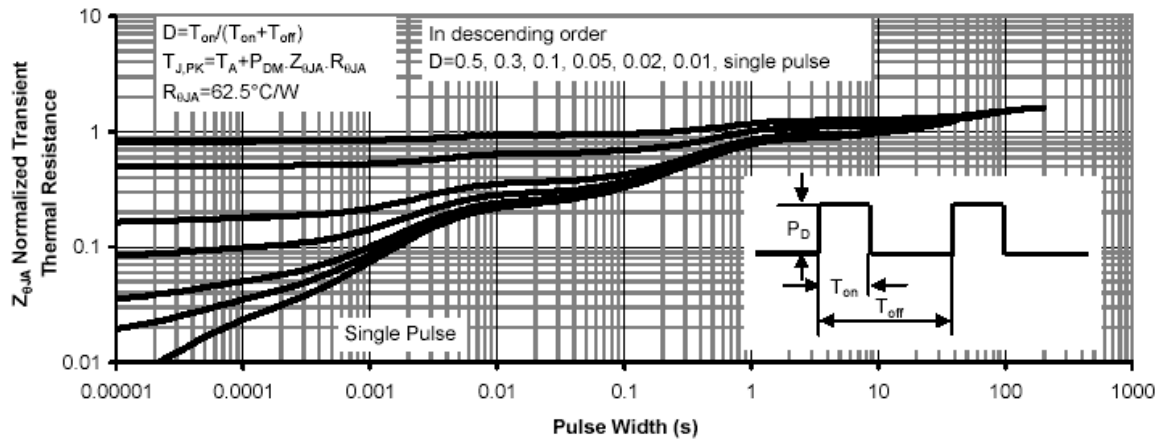


Figure 11: Normalized Maximum Transient Thermal Impedance

TYPICAL N-CANNEL ELECTRICAL AND THERMAL CHARACTERISTICS

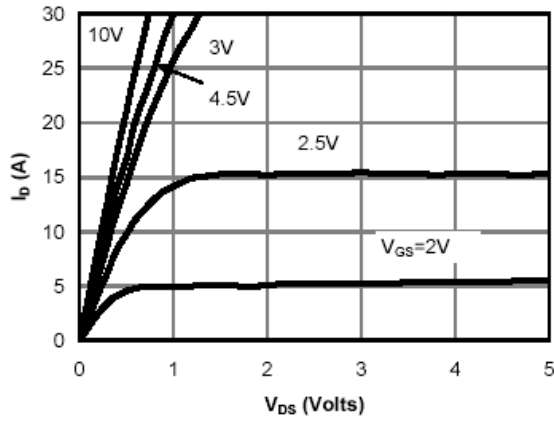


Fig 1: On-Region Characteristics

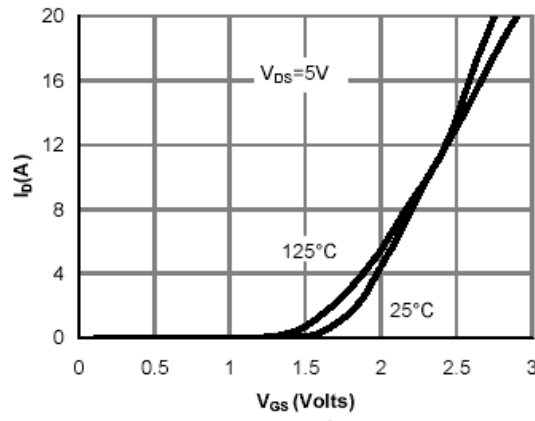


Figure 2: Transfer Characteristics

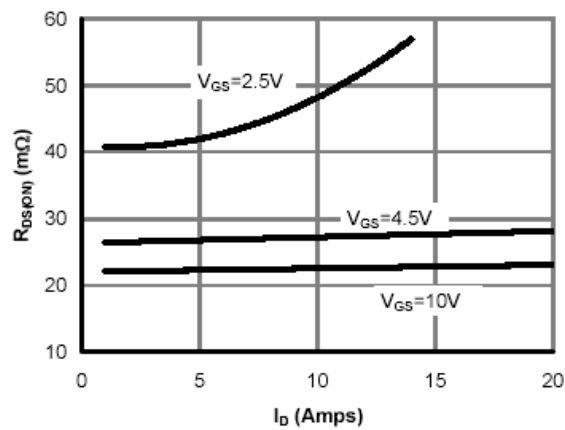


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

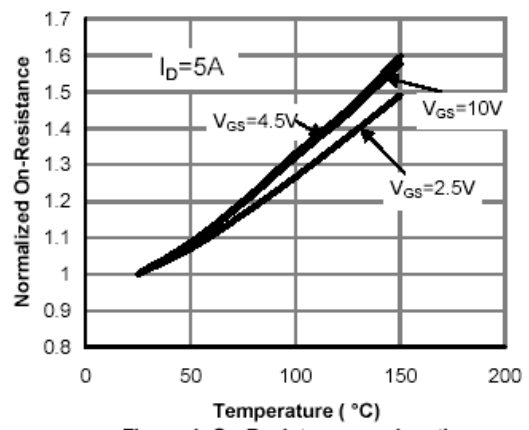


Figure 4: On-Resistance vs. Junction Temperature

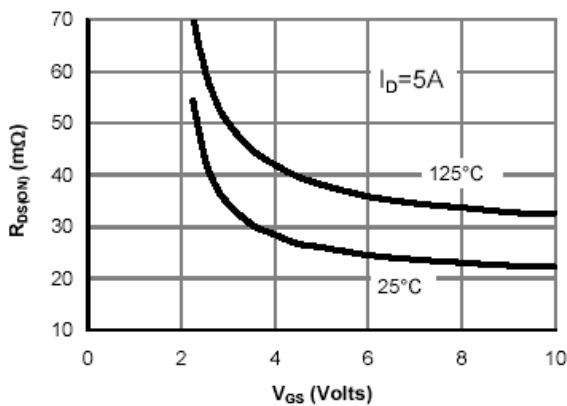


Figure 5: On-Resistance vs. Gate-Source Voltage

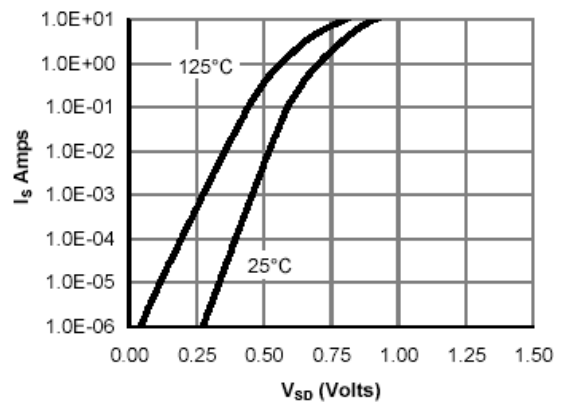


Figure 6: Body diode characteristics

TYPICAL N-CHANNEL ELECTRICAL AND THERMAL CHARACTERISTICS

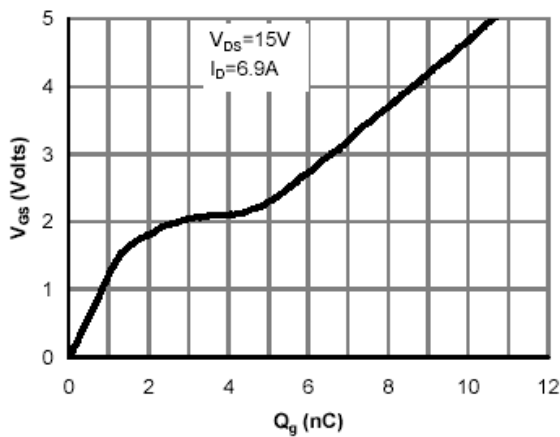


Figure 7: Gate-Charge characteristics

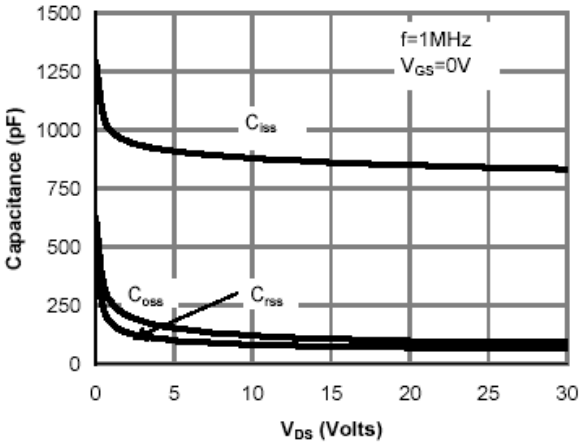


Figure 8: Capacitance Characteristics

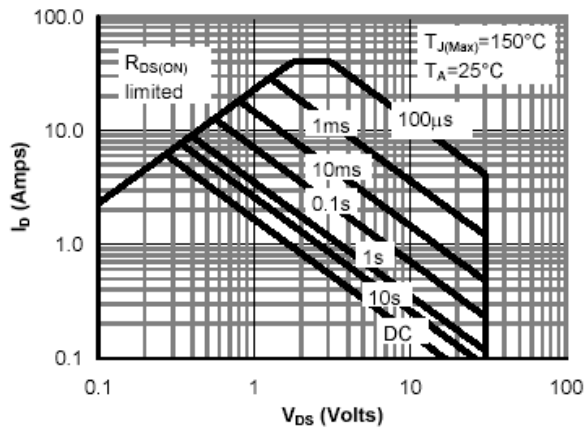


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

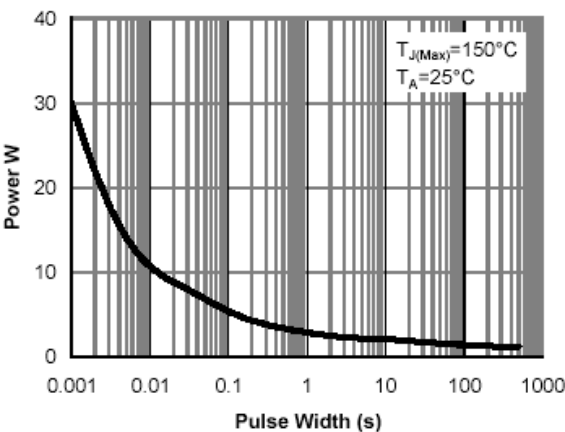


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

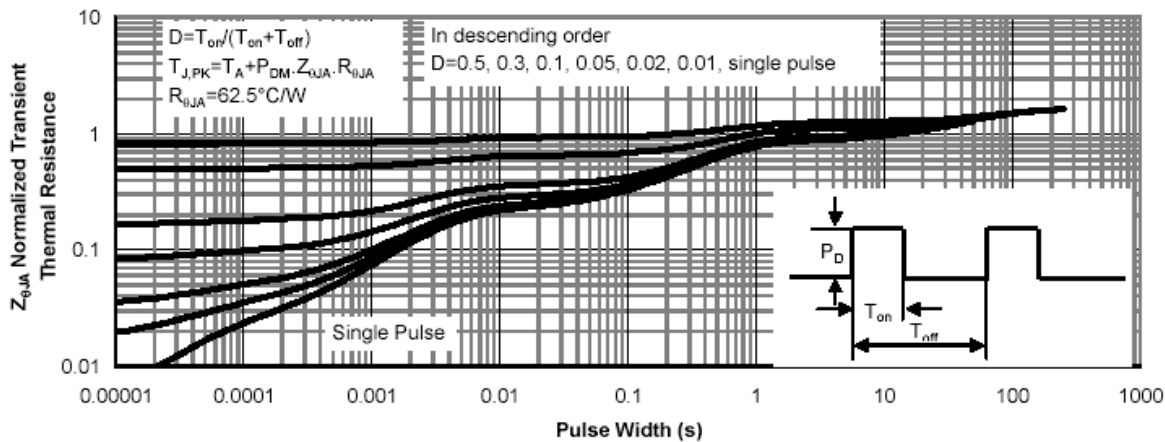


Figure 11: Normalized Maximum Transient Thermal Impedance