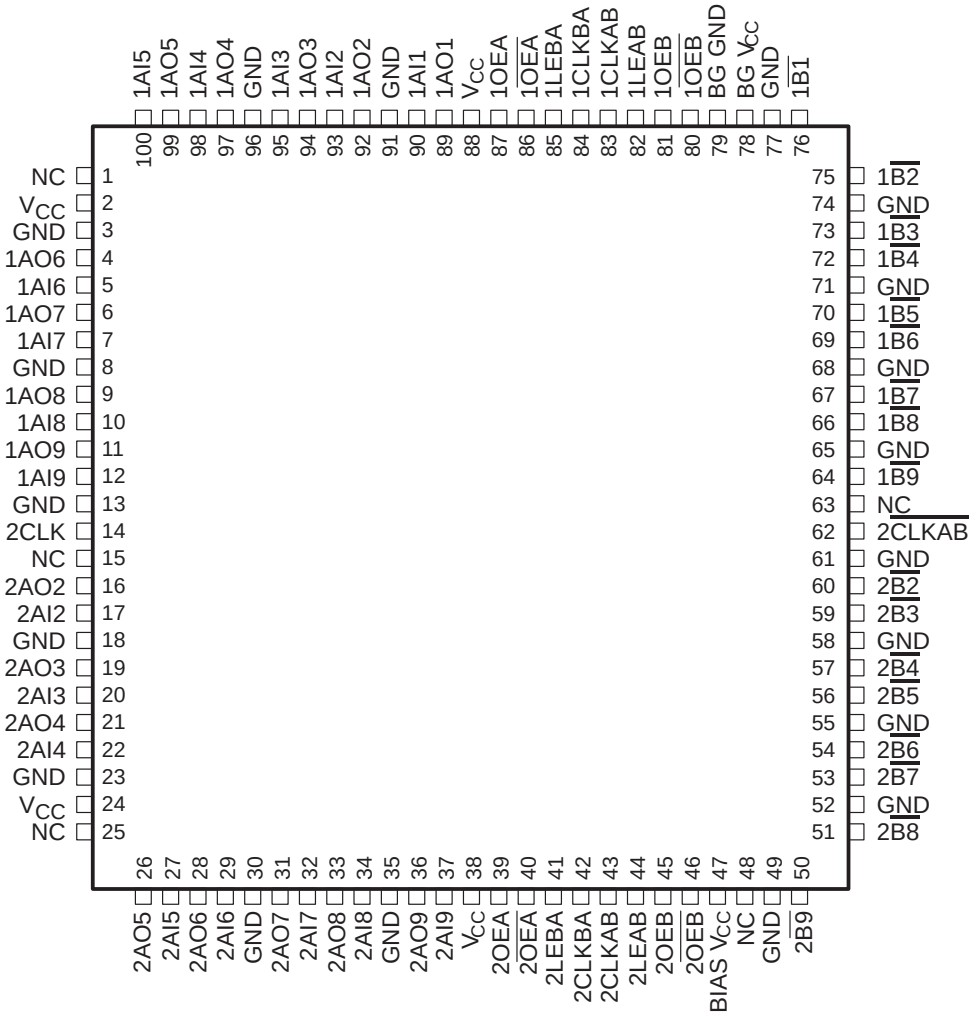
- **Compatible With IEEE Std 1194.1-1991 (BTL)**
- **TTL A Port, Backplane Transceiver Logic (BTL) $\overline{B}$ Port**
- **Open-Collector $\overline{B}$-Port Outputs Sink 100 mA**
- **BIAS $V_{CC}$ Minimizes Signal Distortion During Live Insertion or Withdrawal**
- **High-Impedance State During Power Up and Power Down**
- **$\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage**
- **TTL-Input Structures Incorporate Active Clamping to Aid in Line Termination**

**PCA PACKAGE**
**(TOP VIEW)**




NC − No internal connection

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## description/ordering information

The SN74FB1651 contains an 8-bit and 9-bit transceiver with a buffered clock. The clock and the transceivers are designed to translate signals between TTL and backplane transceiver-logic (BTL) environments. The device is designed specifically to be compatible with IEEE Std 1194.1-1991.

The $\overline{B}$ port operates at BTL-signal levels. The open-collector $\overline{B}$ ports are specified to sink 100 mA. Two output enables (OEB and $\overline{OEB}$) are provided for the $\overline{B}$ outputs. When OEB is low, $\overline{OEB}$ is high, or $V_{CC}$ is less than 2.1 V, the $\overline{B}$ port is turned off.

The A port operates at TTL-signal levels. The A outputs reflect the inverse of the data at the $\overline{B}$ port when the A-port output enable (OEA) is high. When OEA is low or when $V_{CC}$ is less than 2.1 V, the A outputs are in the high-impedance state.

BIAS $V_{CC}$ establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when $V_{CC}$ is not connected.

BG $V_{CC}$ and BG GND are the supply inputs for the bias generator.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| 0°C to 70°C | TQFP − PCA | Tube | SN74FB1651PCA | FB1651 |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

### Function Tables

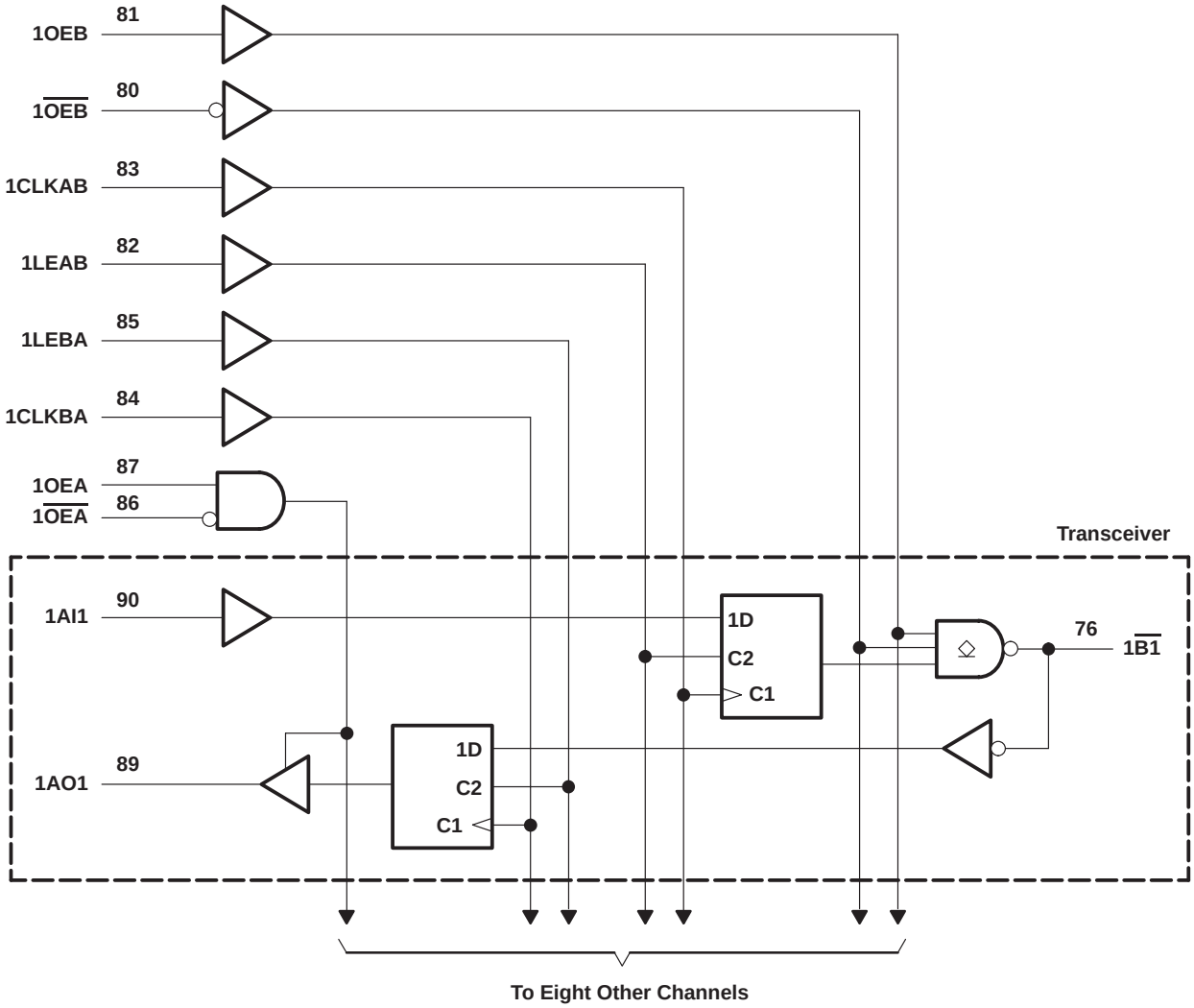
**TRANSCEIVER**

| INPUTS | | | | FUNCTION |
|---|---|---|---|---|
| $\overline{OEA}$ | OEA | OEB | $\overline{OEB}$ | |
| X | X | H | L | $\overline{A}$ data to B bus |
| L | H | X | X | $\overline{B}$ data to A bus |
| L | H | H | L | $\overline{A}$ data to B bus, $\overline{B}$ data to A bus |
| X | X | L | X | B-bus isolation |
| X | X | X | H | |
| H | X | X | X | A-bus isolation |
| X | L | X | X | |

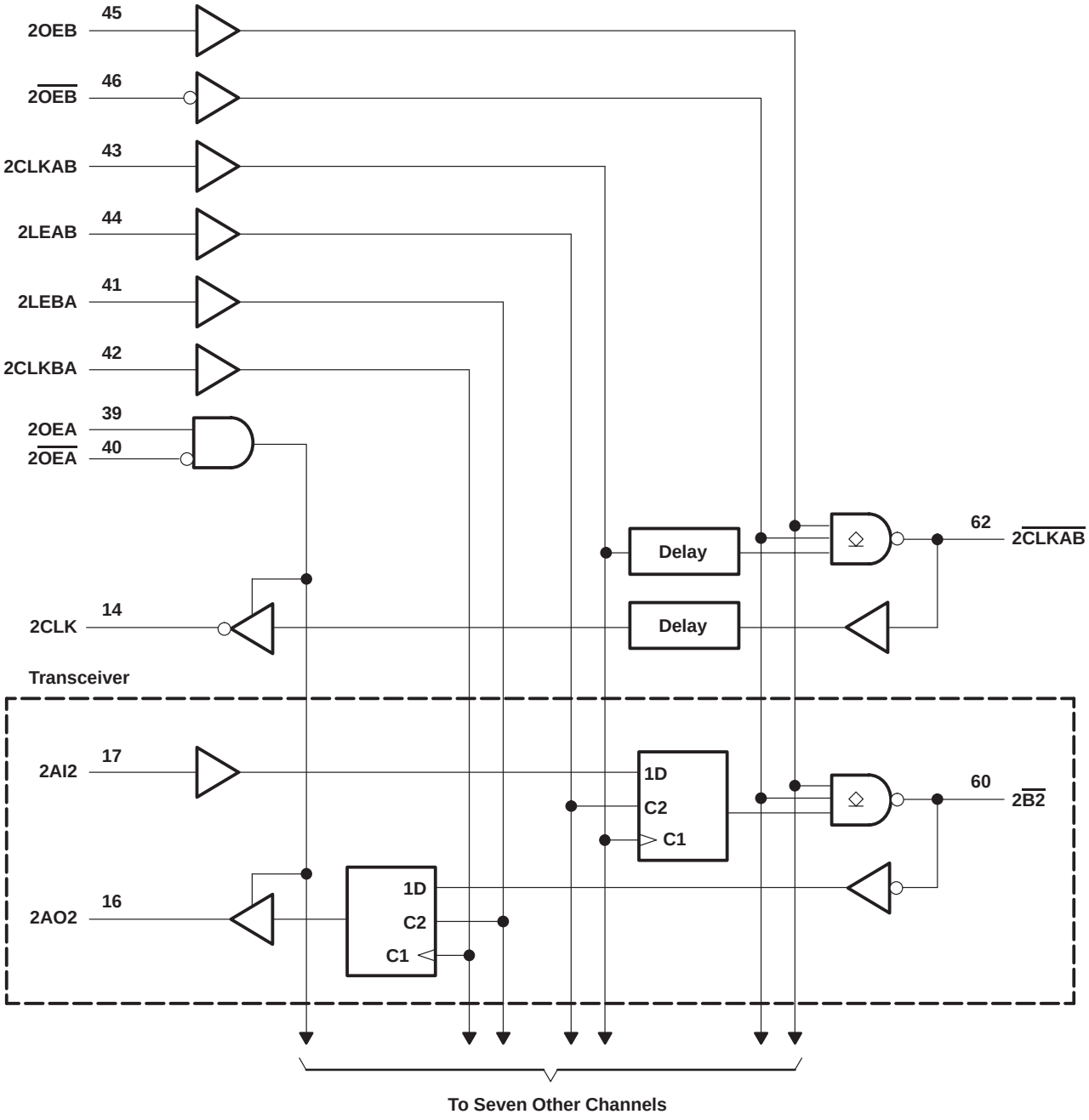
**STORAGE MODE**

| INPUTS | | FUNCTION |
|---|---|---|
| LE | CLK | |
| H | X | Transparent |
| L | ↑ | Store data |
| L | L | Storage |

## functional block diagram



## functional block diagram (continued)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$, BIAS $V_{CC}$, BG $V_{CC}$ . . . . . −0.5 V to 7 V
Input voltage range, $V_I$: Except $\overline{B}$ port . . . . . −1.2 V to 7 V
$\overline{B}$ port . . . . . −1.2 V to 3.5 V
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state, $V_O$ . . . . . −0.5 V to 3.5 V
Voltage range applied to any output in the high state, $V_O$ . . . . . −0.5 V to $V_{CC}$
Input clamp current, $I_{IK}$: Except $\overline{B}$ port . . . . . −40 mA
$\overline{B}$ port . . . . . −18 mA
Current applied to any single output in the low state, $I_O$: A port . . . . . 48 mA
$\overline{B}$ port . . . . . 200 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1) . . . . . 22°C/W
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 2)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$, BG $V_{CC}$, BIAS $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $\overline{B}$ port | 1.62 | | 2.3 | V |
| | | Except $\overline{B}$ port | 2 | | | |
| $V_{IL}$ | Low-level input voltage | $\overline{B}$ port | 0.75 | | 1.47 | V |
| | | Except $\overline{B}$ port | | | 0.8 | |
| $I_{IK}$ | Input clamp current | | | | −18 | mA |
| $I_{OH}$ | High-level output current | A port | | | −3 | mA |
| $I_{OL}$ | Low-level output current | A port | | | 24 | mA |
| | | $\overline{B}$ port | | | 100 | |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

NOTE 2: To ensure proper device operation, all unused inputs must be terminated as follows: A and control inputs to $V_{CC}$(5 V) or GND, and B inputs to GND only. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | $\overline{B}$ port | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | V |
| | Except $\overline{B}$ port | $V_{CC}$ = 4.5 V, | $I_I$ = −40 mA | | | −0.5 | |
| $V_{OH}$ | AO port | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −3 mA | 2.5 | 3.3 | | V |
| $V_{OL}$ | AO port | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 24 mA | | 0.35 | 0.5 | V |
| | $\overline{B}$ port | $V_{CC}$ = 4.5 V | $I_{OL}$ = 80 mA | 0.75 | | 1.1 | |
| | | | $I_{OL}$ = 100 mA | | | 1.15 | |
| $I_I$ | Except $\overline{B}$ port | $V_{CC}$ = 5.5 V, | $V_I$ = 5.5 V | | | 50 | µA |
| $I_{IH}$‡ | Except $\overline{B}$ port | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 50 | µA |
| $I_{IL}$‡ | Except $\overline{B}$ port | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −50 | µA |
| | $\overline{B}$ port | $V_{CC}$ = 5.5 V, | $V_I$ = 0.75 V | | | −100 | |
| $I_{OZH}$ | AO port | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | µA |
| $I_{OZL}$ | AO port | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | −50 | µA |
| $I_{OZPU}$ | AO port | $V_{CC}$ = 0 to 2.1 V, | $V_O$ = 0.5 V to 2.7 V | | | 50 | µA |
| $I_{OZPD}$ | AO port | $V_{CC}$ = 2.1 V to 0, | $V_O$ = 0.5 V to 2.7 V | | | −50 | µA |
| $I_{OH}$ | $\overline{B}$ port | $V_{CC}$ = 0 to 5.5 V, | $V_O$ = 2.1 V | | | 100 | µA |
| $I_{OS}$§ | A port | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −30 | | −150 | mA |
| $I_{CC}$ | A port to $\overline{B}$ port | $V_{CC}$ = 5.5 V, | $I_O$ = 0 | | | 100 | mA |
| | $\overline{B}$ port to A port | | | | | 120 | |
| $C_i$ | AI port | $V_I$ = 0.5 V or 2.5 V | | | 5.5 | | pF |
| | Control inputs | | | | 5.5 | | |
| $C_o$ | AO ports | $V_O$ = 0.5 V or 2.5 V | | | 5.5 | | pF |
| $C_{io}$ | $\overline{B}$ port per IEEE Std 1194.1-1991 | $V_{CC}$ = 0 to 5.5 V | | | | 5.5 | pF |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ For I/O ports, the parameters $I_{IH}$ and $I_{IL}$ include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## live-insertion specifications over recommended operating free-air temperature range

| PARAMETER | | TEST CONDITIONS | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ (BIAS $V_{CC}$) | | $V_{CC}$ = 0 to 4.5 V | $V_B$ = 0 to 2 V, | $V_I$ (BIAS $V_{CC}$) = 4.5 V to 5.5 V | | 450 | µA |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | | | 10 | |
| $V_O$ | $\overline{B}$ port | $V_{CC}$ = 0, | $V_I$ (BIAS $V_{CC}$) = 5 V | | 1.62 | 2.1 | V |
| $I_O$ | $\overline{B}$ port | $V_{CC}$ = 0 , | $V_B$ = 1 V, | $V_I$ (BIAS $V_{CC}$) = 4.5 V to 5.5 V | −1 | | µA |
| | | $V_{CC}$ = 0 to 2.2 V, | OEB = 0 to 5 V | | | 100 | |
| | | $V_{CC}$ = 0 to 5.5 V, | OEB = 0 to 0.8 V | | | 1 | mA |

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)**

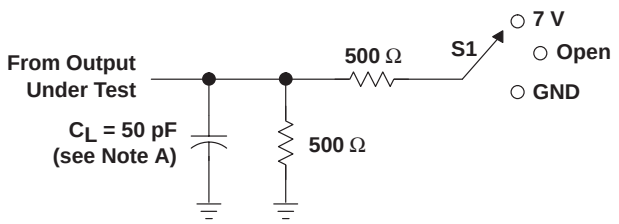
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | | | |
| $f_{clock}$ | Clock frequency | | | 150 | | 150 | MHz |
| $t_w$ | Pulse duration | CLK or LE | 3.3 | | 3.3 | | ns |
| $t_{su}$ | Setup time | Data before LE | 4.8 | | 4.8 | | ns |
| | | Data before CLK↑ | 4.9 | | 4.6 | | |
| $t_h$ | Hold time | Data after LE | 1.8 | | 1.8 | | ns |
| | | Data after CLK↑ | 1.1 | | 1.1 | | |

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)**

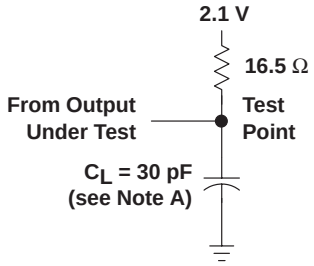
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | 150 | | | 150 | | MHz |
| $t_{PLH}$ | AI | $\overline{B}$ | 1.8 | 3.7 | 5.3 | 1.8 | 6.2 | ns |
| $t_{PHL}$ | | | 2.9 | 4.4 | 6 | 2.9 | 6.6 | |
| $t_{PLH}$ | LEAB | $\overline{B}$ | 2.7 | 4.2 | 5.8 | 2.7 | 6.4 | ns |
| $t_{PHL}$ | | | 3.5 | 5 | 6.5 | 3.5 | 7.3 | |
| $t_{PLH}$ | CLKAB | $\overline{B}$ | 2.3 | 3.9 | 5.5 | 2.3 | 6 | ns |
| $t_{PHL}$ | | | 2.9 | 4.5 | 6.1 | 2.9 | 6.7 | |
| $t_{PLH}$ | 2CLKAB | $2\overline{CLKAB}$ | 4.6 | 6.9 | 8.8 | 4.6 | 9.9 | ns |
| $t_{PHL}$ | | | 4.9 | 6.5 | 8.1 | 4.9 | 8.8 | |
| $t_{PLH}$ | $\overline{B}$ | AO | 3.5 | 5.9 | 7.9 | 3.5 | 8 | ns |
| $t_{PHL}$ | | | 2.2 | 3.7 | 5.3 | 2.2 | 5.7 | |
| $t_{PLH}$ | LEBA | AO | 1.8 | 3.2 | 4.6 | 1.8 | 5.1 | ns |
| $t_{PHL}$ | | | 1.7 | 3 | 4.4 | 1.7 | 4.7 | |
| $t_{PLH}$ | CLKBA | AO | 1.8 | 3.1 | 4.6 | 1.8 | 5.1 | ns |
| $t_{PHL}$ | | | 1.7 | 3.1 | 4.6 | 1.7 | 4.9 | |
| $t_{PLH}$ | $2\overline{CLKAB}$ | 2CLK | 6.4 | 9.7 | 11.8 | 6.4 | 13.4 | ns |
| $t_{PHL}$ | | | 4.1 | 6.9 | 8.9 | 4.1 | 10.3 | |
| $t_{PLH}$ | OEB | $\overline{B}$ | 2.7 | 4.6 | 6.4 | 2.7 | 6.7 | ns |
| $t_{PHL}$ | | | 2.9 | 4.1 | 5.9 | 2.9 | 6.6 | |
| $t_{PLH}$ | $\overline{OEB}$ | $\overline{B}$ | 2.6 | 4.3 | 6.2 | 2.6 | 6.6 | ns |
| $t_{PHL}$ | | | 3.4 | 4.6 | 6.4 | 3.4 | 7 | |
| $t_{PZH}$ | OEA | AO | 1.4 | 2.9 | 4.4 | 1.4 | 4.9 | ns |
| $t_{PZL}$ | | | 1.4 | 2.6 | 4 | 1.4 | 4.6 | |
| $t_{PHZ}$ | OEA | AO | 1.7 | 3.4 | 5.1 | 1.7 | 5.8 | ns |
| $t_{PLZ}$ | | | 2.2 | 3.6 | 5 | 2.2 | 5.5 | |
| $t_{PZH}$ | $\overline{OEA}$ | AO | 1.7 | 3.3 | 4.7 | 1.7 | 5.5 | ns |
| $t_{PZL}$ | | | 1.7 | 3.1 | 4.4 | 1.7 | 5.1 | |
| $t_{PHZ}$ | $\overline{OEA}$ | AO | 1.5 | 2.9 | 4.5 | 1.5 | 5.1 | ns |
| $t_{PLZ}$ | | | 2 | 3.1 | 4.6 | 2 | 4.8 | |
| $t_{sk(p)}$† | Pulse skew, AI to $\overline{B}$ or $\overline{B}$ to AO | | | 1 | | | | ns |
| $t_{sk(o)}$† | Output skew, AI to $\overline{B}$ or $\overline{B}$ to AO | | | 0.5 | | | | ns |
| $t_t$ Transition time | $\overline{B}$ outputs (1.3 V to 1.8 V) | | 0.9 | 1.7 | | 0.5 | 4.6 | ns |
| | AO outputs (10% to 90%) | | 0.5 | 2 | | 0.4 | 4.2 | |
| $\overline{B}$-port input pulse rejection | | | 1 | | | 1 | | ns |

† Skew values are applicable for through mode only.

## PARAMETER MEASUREMENT INFORMATION

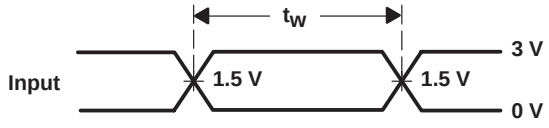



LOAD CIRCUIT FOR A OUTPUTS

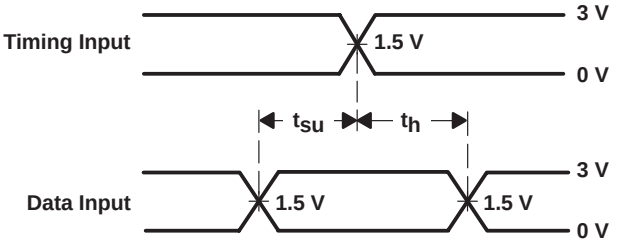



| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |

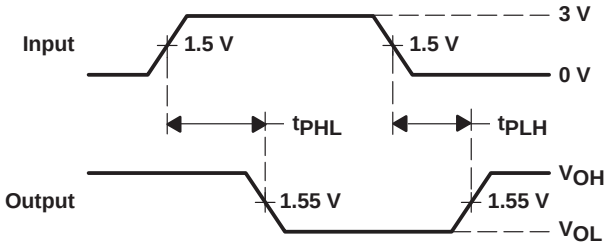
LOAD CIRCUIT FOR B OUTPUTS



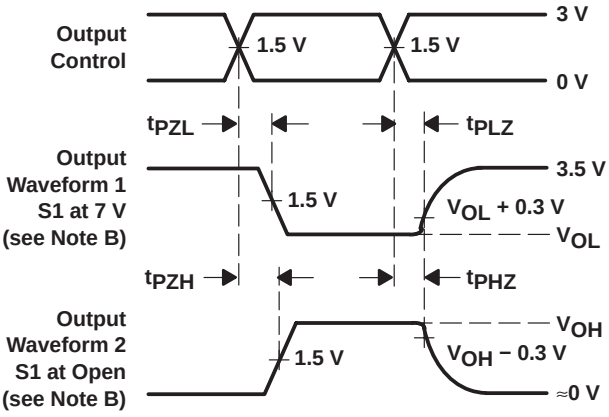

VOLTAGE WAVEFORMS
PULSE DURATION



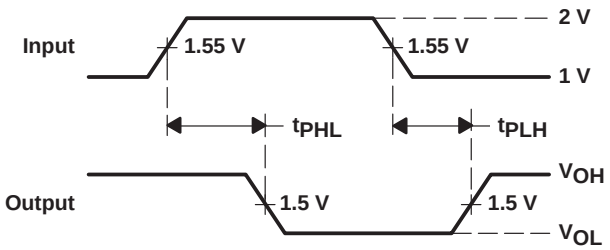

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A TO B)




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A PORT)




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B TO A)

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: TTL inputs: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns; BTL inputs: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| SN74FB1651PCA | ACTIVE | HLQFP | PCA | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |

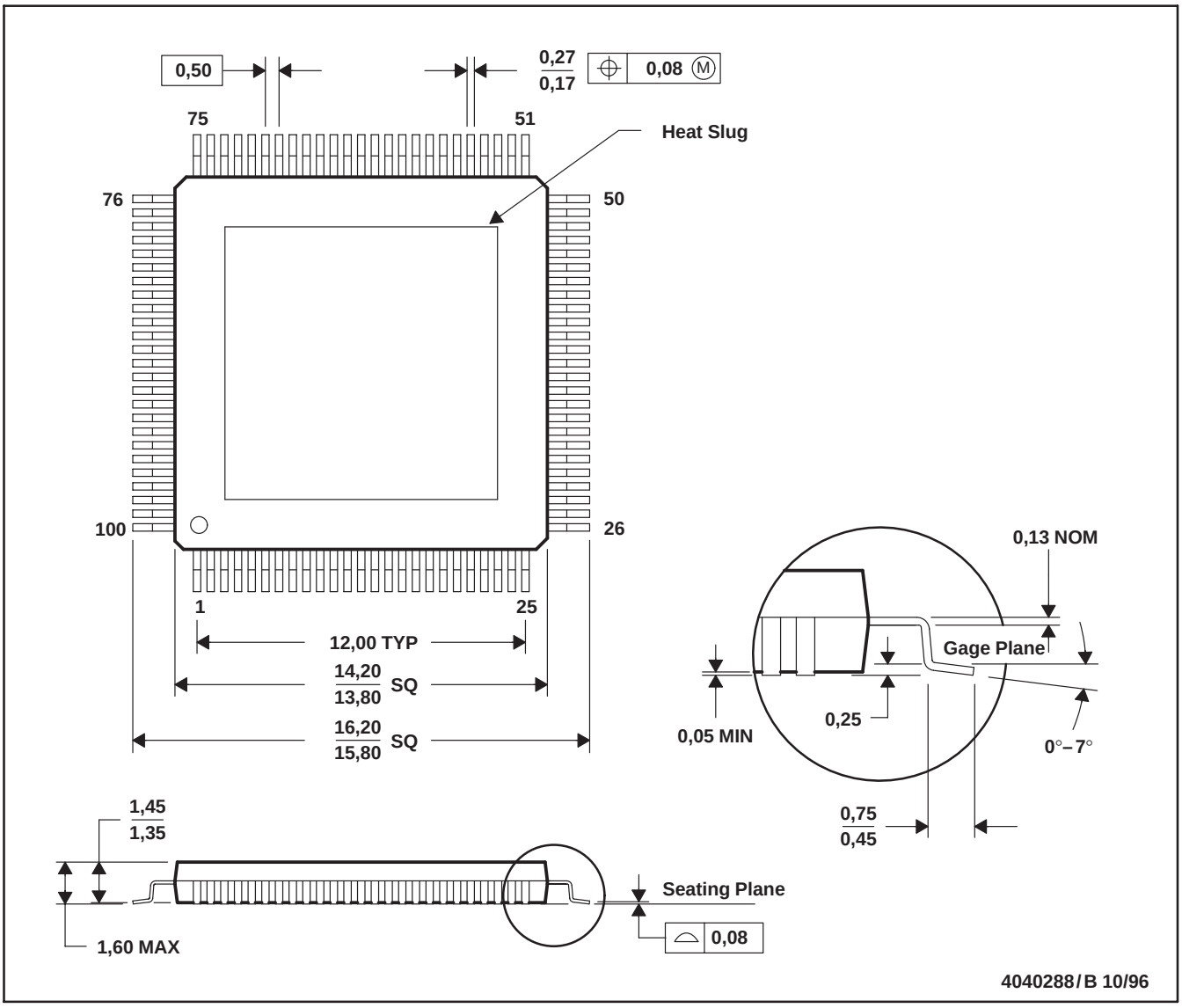
(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

MHTQ003A – JANUARY 1995 – REVISED DECEMBER 1996

**PCA (S-PQFP-G100)** **PLASTIC QUAD FLATPACK (DIE DOWN)**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Thermally enhanced molded plastic package with a heat slug (HSL)
D. Falls within JEDEC MS-026

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