National Semiconductor

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MM54C150/MM74C150 16-Line to 1-Line Multiplexer MM72C19/MM82C19 TRI-STATE® 16-Line to 1-Line Multiplexer

MM54C150/MM74C150 16-Line to 1-Line Multiplexer
MM72C19/MM82C19 TRI-STATE 16-Line to 1-Line Multiplexer

General Description

The MM54C150/MM74C150 and MM72C19/MM82C19 multiplex 16 digital lines to 1 output. A 4-bit address code determines the particular 1-of-16 inputs which is routed to the output. The data is inverted from input to output.

A strobe override places the output of MM54C150/MM74C150 in the logical "1" state and the output of MM72C19/MM82C19 in the high-impedance state.

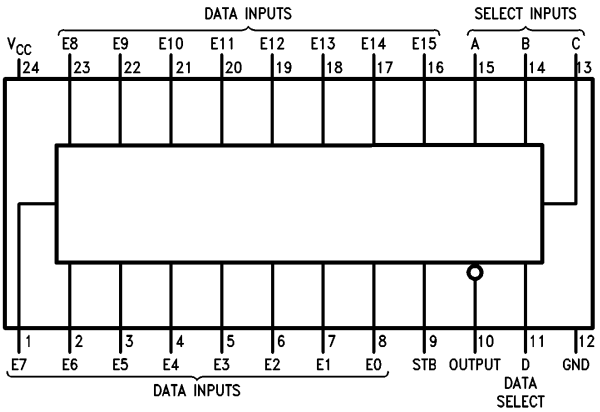
All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ TTL compatibility	Drive 1 TTL Load

Connection Diagram

Dual-In-Line Package



TL/F/5891–1

Order Number MM54C150, MM74C150, MM72C19 or MM82C19

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C150, MM72C19	−55°C to +125°C
MM74C150, MM82C19	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3.0V to 15V
V_{CC}	18V
Lead Temperature (soldering, 10 seconds)	260°C

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V V_{CC} = 10V	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V V_{CC} = 10V			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0V, I_O = −10 μA V_{CC} = 10V, I_O = −10 μA	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0V, I_O = +10 μA V_{CC} = 10V, I_O = +10 μA			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	V
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
I_{OZ}	Output Current in High Impedance State MM72C19/MM82C19	 V_{CC} = 15V, V_O = 15V V_{CC} = 15V, V_O = 0V	 −1.0	 0.005 −0.005	 1.0 	 μA μA
I_{CC}	Supply Current	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, 72C, V_{CC} = 4.5V 74C, 82C, V_{CC} = 4.75V	V_{CC}−1.5 V_{CC}−1.5			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, 72C, V_{CC} = 4.5V 74C, 82C, V_{CC} = 4.75V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, 72C, V_{CC} = 4.5V, I_O = −1.6 mA 74C, 82C, V_{CC} = 4.75V, I_O = −1.6 mA	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, 72C, V_{CC} = 4.5V, I_O = 1.6 mA 74C, 82C, V_{CC} = 4.75V, I_O = 1.6 mA			0.4 0.4	V V
Output Drive (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−4.35	−8		mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−20	−40		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	4.35	8		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	20	40		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data Inputs to Output	$V_{CC} = 5.0V$ $V_{CC} = 10V$ $V_{CC} = 5.0V$, $C_L = 150$ pF $V_{CC} = 10V$, $C_L = 150$ pF		250 110 290 120	600 300 650 330	ns ns ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data Select Inputs to Output	$V_{CC} = 5.0V$ $V_{CC} = 10V$		290 120	650 330	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Strobe to Output MM54C150/MM74C150	$V_{CC} = 5.0V$ $V_{CC} = 10V$		120 55	300 150	ns ns
t_{1H}, t_{0H}	Delay from Strobe to High Impedance State MM72C19/MM82C19	$V_{CC} = 5.0V$, $R_L = 10k$, $C_L = 5$ pF $V_{CC} = 10V$, $R_L = 10k$, $C_L = 5$ pF		80 60	200 150	ns ns
t_{H1}, t_{H0}	Delay from Strobe to Logical "1" Level or to Logical "0" Level (from High Impedance State) MM72C19/MM82C19	$V_{CC} = 5.0V$, $R_L = 10k$, $C_L = 5$ pF $V_{CC} = 10V$, $R_L = 10k$, $C_L = 5$ pF		80 30	250 120	ns ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5.0		pF
C_{OUT}	Output Capacitance MM72C19/MM82C19	(Note 2)		11.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		100		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics, application note AN-90.

Truth Table

MM54C150/MM74C150

Inputs																				Output
D	C	B	A	STROBE	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13	E14	E15	W
X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1*
0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	0	1	0	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	1	0	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	0	0	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	0	0	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	1	0	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	0	0	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	0	0	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	1	0	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	1
0	1	0	1	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	0
0	1	1	0	0	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	1
0	1	1	0	0	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	0
0	1	1	1	0	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	1
0	1	1	1	0	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	0
1	0	0	0	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	1
1	0	0	0	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	0
1	0	0	1	0	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
1	0	0	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	0
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	1
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	0
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	1
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	0
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	1
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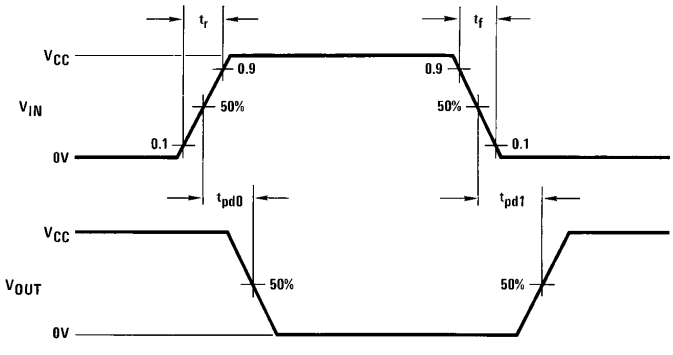
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	0
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	1
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	0
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0

*For MM72C19/MM82C19 this would be Hi-Z, everything else is the same.

Switching Time Waveforms

CMOS to CMOS



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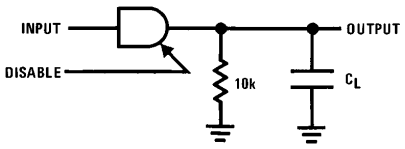
Switching Time Waveforms (Continued)

t_{1H} and t_{H1}



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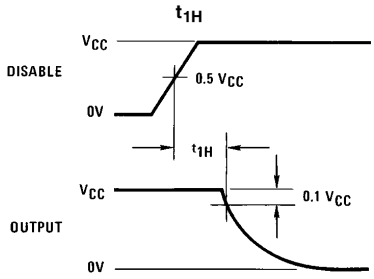
t_{1H}



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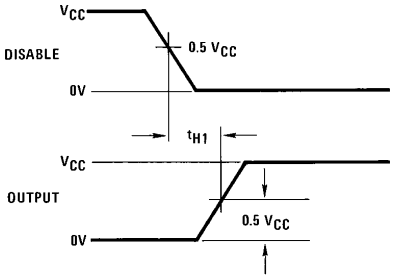
t_{H1}



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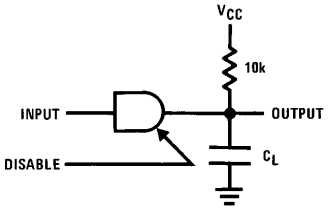
t_{0H} and t_{H0}



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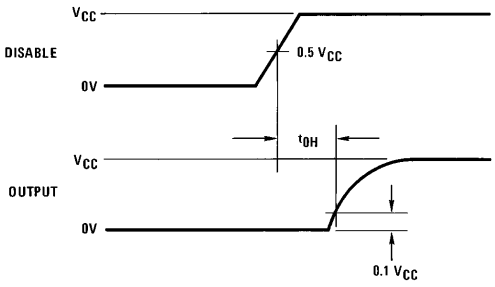
t_{0H}



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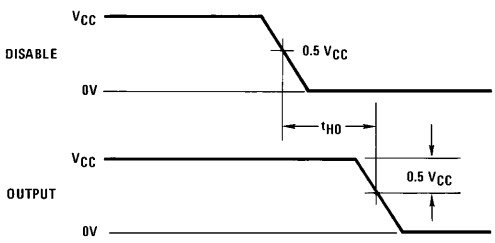
t_{H0}



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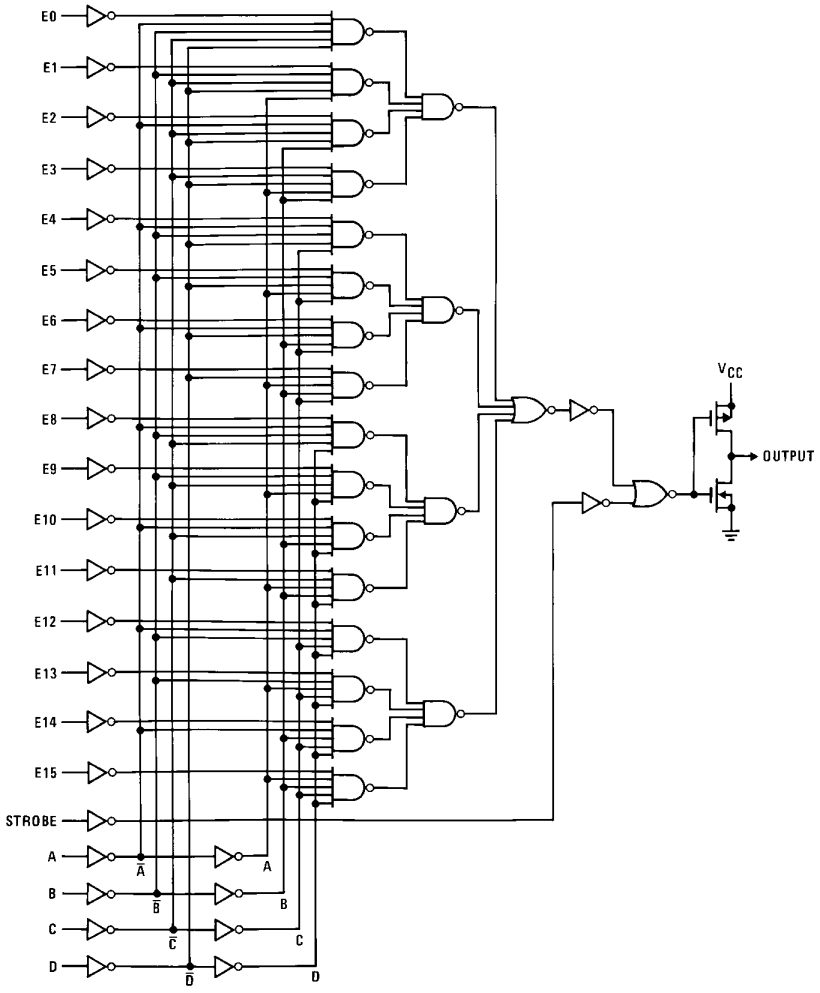
Note: Delays measured with input t_r, $t_f \leq 20$ ns.

Logic Diagrams

MM54C150/MM74C150



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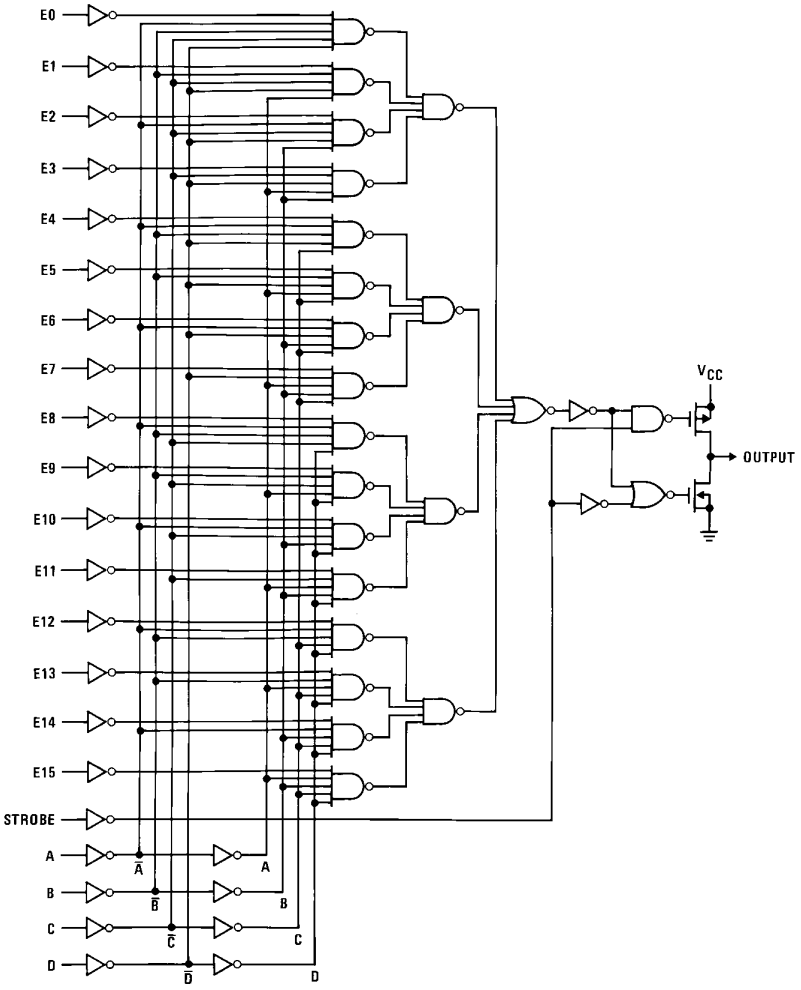
Logic Diagrams (Continued)

MM72C19/MM82C19



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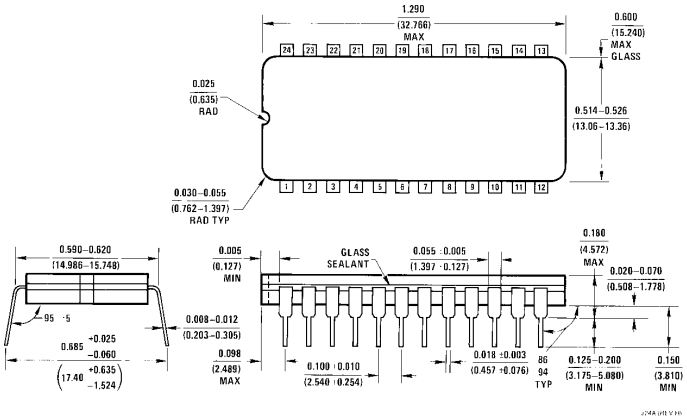
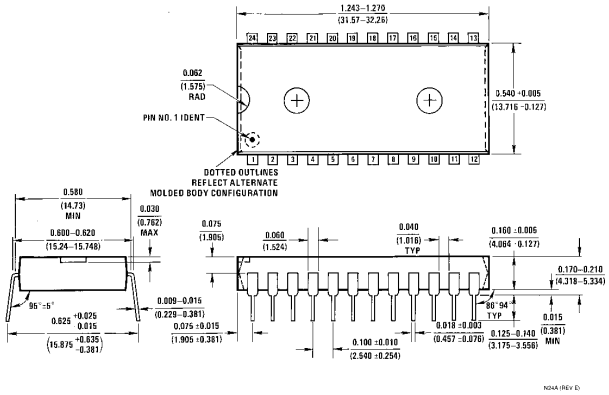
Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number MM54C150J or MM74C150J, MM72C19J or MM82C19J
NS Package Number J24A



Molded Dual-In-Line Package (N)
Order Number MM54C150N, MM74C150N, MM72C19N or MM82C19N
NS Package Number N24A

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