

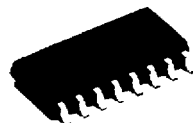
DESCRIPTION

FEATURES

- 

Outline 16P4(P)

2.54mm pitch 300mil DIP
(6.3mm x 19.0mm x 3.3mm)



Outline 16P2S-A(FP)

1.27mm pitch 225mil SOP
(4.4mm x 10.0mm x 1.5mm)

RECOMMENDED OPERATING CONDITIONS

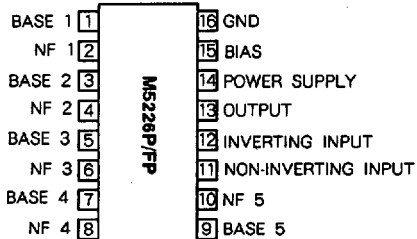
Supply voltage range.....	V _{CC} = 4 to 20V
Rated supply voltage.....	V _{CC} = 20V
Rated power dissipation	700mW (P) 550mW(FP)

The diagram illustrates the signal flow in a stereo system. It begins with an antenna connected to an RF Tuner Block. Below this, a CD Player Block and a Tape Deck Block are shown. All three blocks feed into a central Input Selector block, which contains a switch currently positioned towards the CD Player. The output of the Input Selector is split into two parallel channels, each passing through a capacitor. Each channel then goes through a Graphic Equalizer block labeled 'M5226P/FP'. The outputs of these equalizers are connected to a Master Volume Control block, which features a vertical potentiometer symbol. After the volume control, the signal is again split into two channels, each passing through a capacitor. These channels then enter a Power Amp block, represented by a trapezoidal shape. Finally, the outputs of the power amplifiers are connected to two separate speaker icons.

M5226P/FP

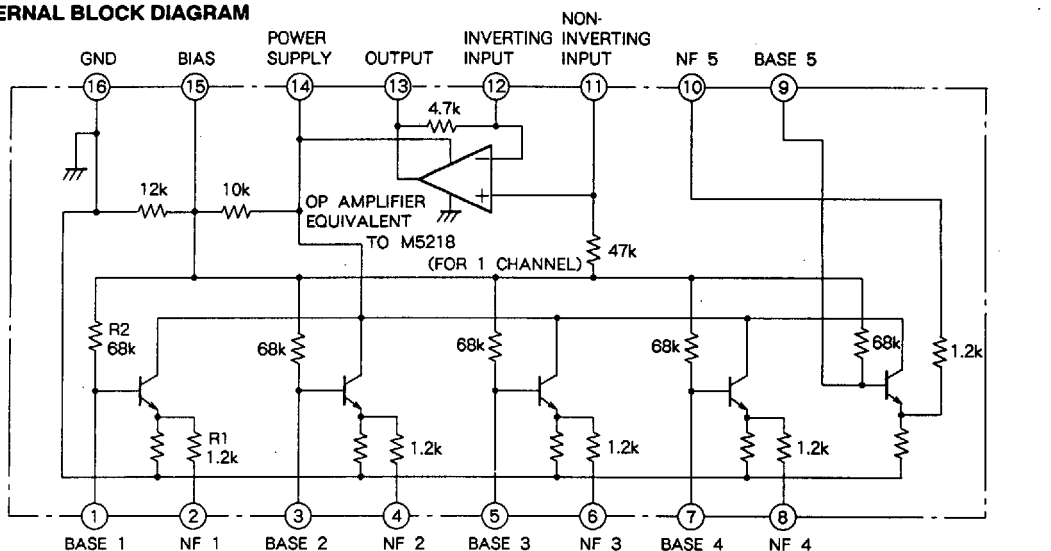
5-ELEMENT GRAPHIC EQUALIZER IC

PIN CONFIGURATION (TOP VIEW)



Outline 16P4(P)
16P2S-A(FP)

IC INTERNAL BLOCK DIAGRAM



Unit Resistance : Ω

M5226P/FP

5-ELEMENT GRAPHIC EQUALIZER IC

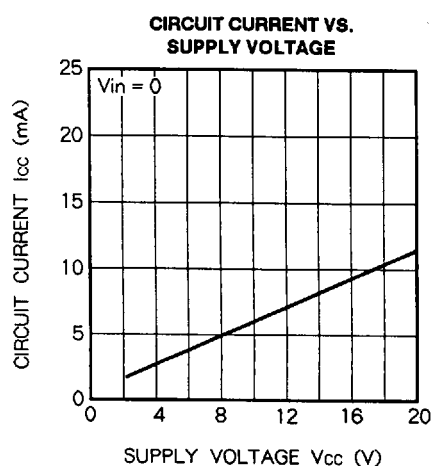
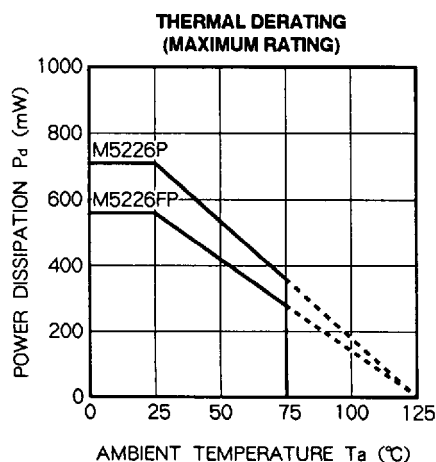
ABSOLUTE MAXIMUM RATINGS (Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V _{cc}	Supply voltage	20	V
I _{LP}	Load current	30	mA
P _d	Power dissipation	550(FP)/1000(DIP)	mW
T _{opr}	Operating temperature	-20 to +75	°C
T _{stg}	Storage temperature	-55 to +125	°C

ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{cc} = 9V)

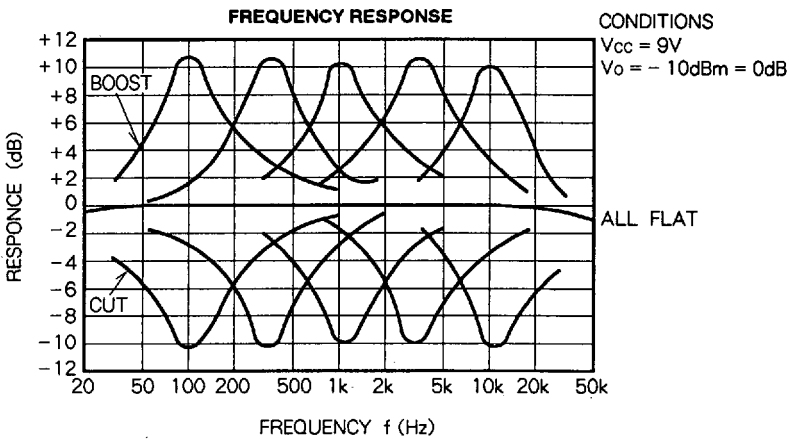
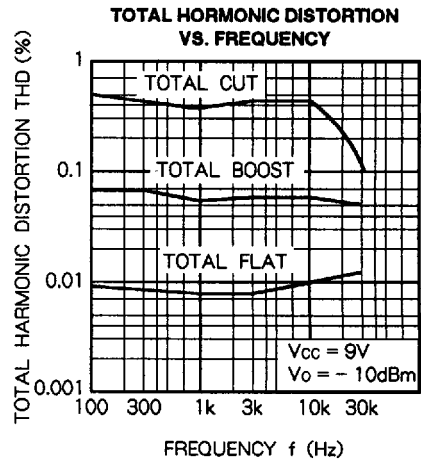
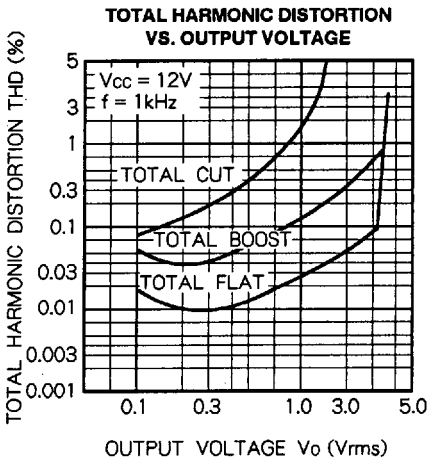
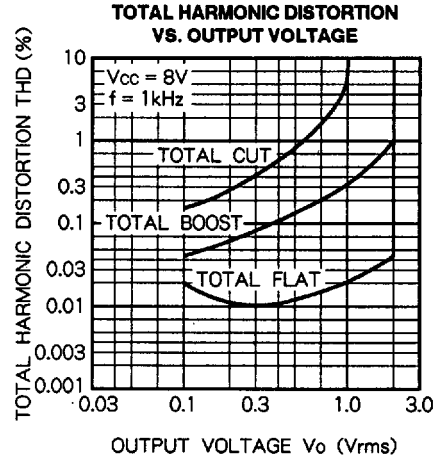
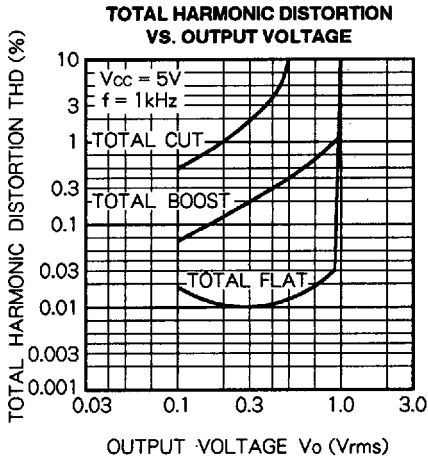
Symbol	Parameter		f [Hz]	Test conditions	Limits			Unit	
					Min	Typ	Max		
I _{CC}	Circuit current		—	V _{in} = 0	3.0	5.2	8.0	mA	
G _{V(FLAT)}	Voltage gain	Flat	1k	V _{in} = − 10dBm	− 3.8	− 0.8	+ 2.2	dB	
G _{V(BOOST)}		Boost	108	V _{in} = − 10dBm	7.2	9.7	11.2		
			343		7.2	9.7	11.2		
			1.08k		7.2	9.7	11.2		
			3.43k		7.2	9.7	11.2		
			10.8k		7.2	9.7	11.2		
G _{V(CUT)}		Cut	108	V _{in} = − 10dBm	− 12.8	− 11.3	− 8.8	dB	
			343		− 12.8	− 11.3	− 8.8		
			1.08k		− 12.8	− 11.3	− 8.8		
			3.43k		− 12.8	− 11.3	− 8.8		
			10.8k		− 12.8	− 11.3	− 8.8		
THD	Total harmonic distortion		1k	V _{in} = 1V _{rms}	—	0.02	0.1	%	
V _{NO}	Output noise voltage		Input short BW : 10Hz to 30kHz (3dB) flat			—	5.0	20	μV _{rms}

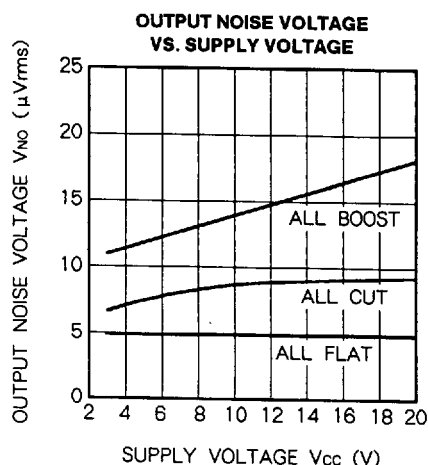
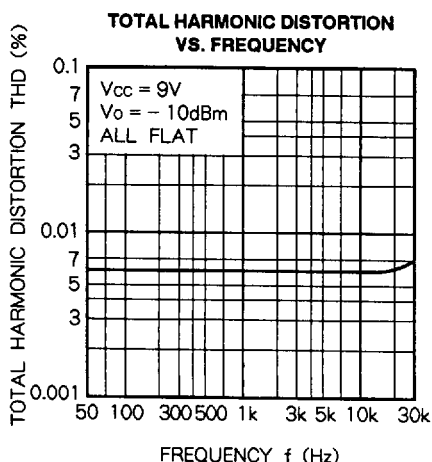
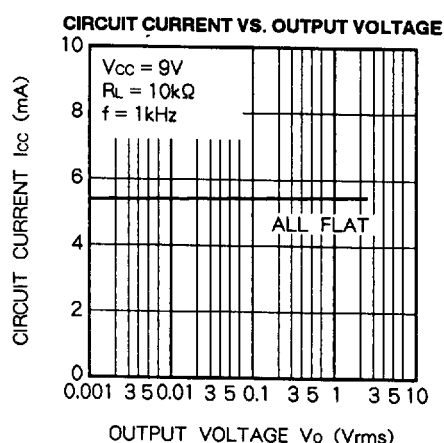
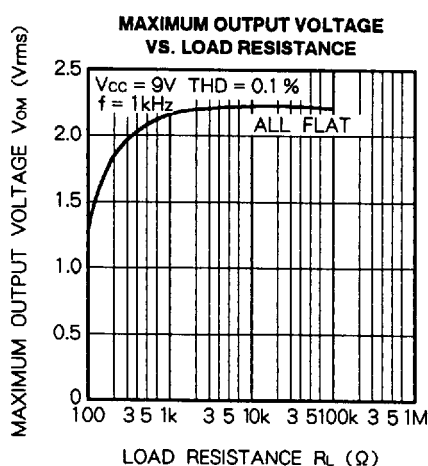
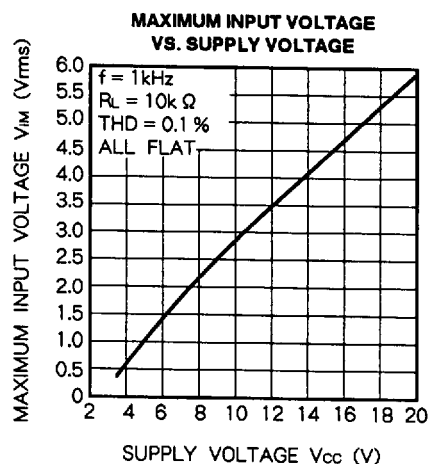
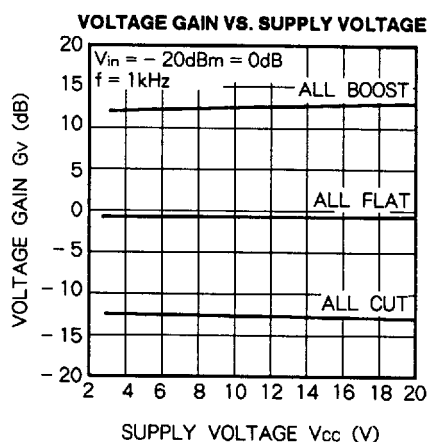
TYPICAL CHARACTERISTICS



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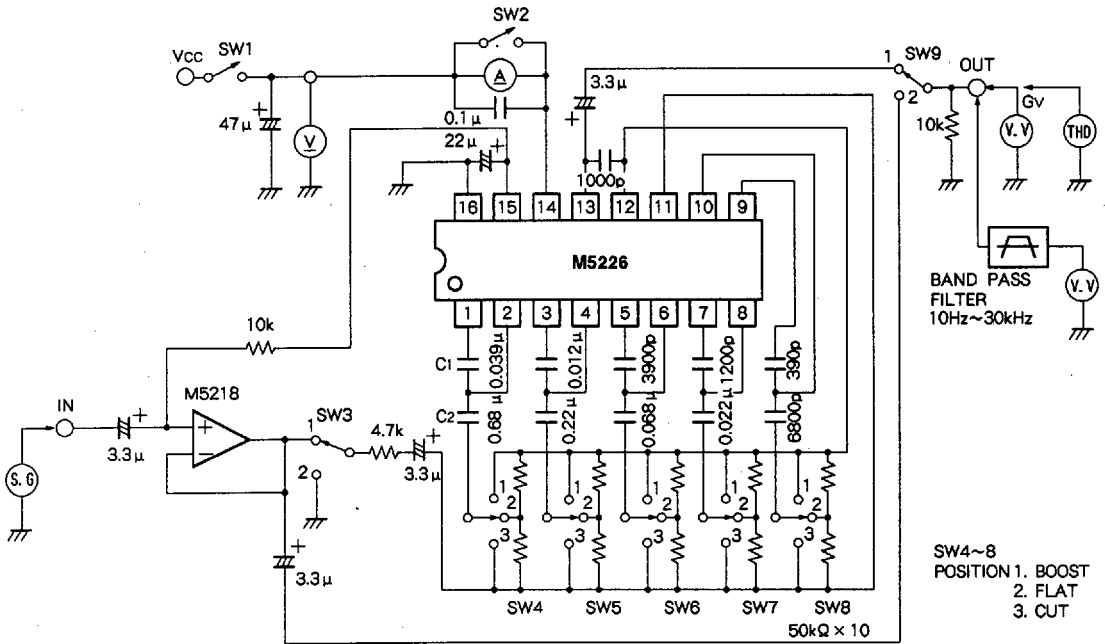
5-ELEMENT GRAPHIC EQUALIZER IC





5-ELEMENT GRAPHIC EQUALIZER IC

TEST CIRCUIT (Circuit current I_{cc} , Voltage gain G_v , Total harmonic distortion THD, Output noise voltage V_{no})



Units Resistance : Ω
Capacitance : F

TEST CIRCUIT SWITCH MATRIX

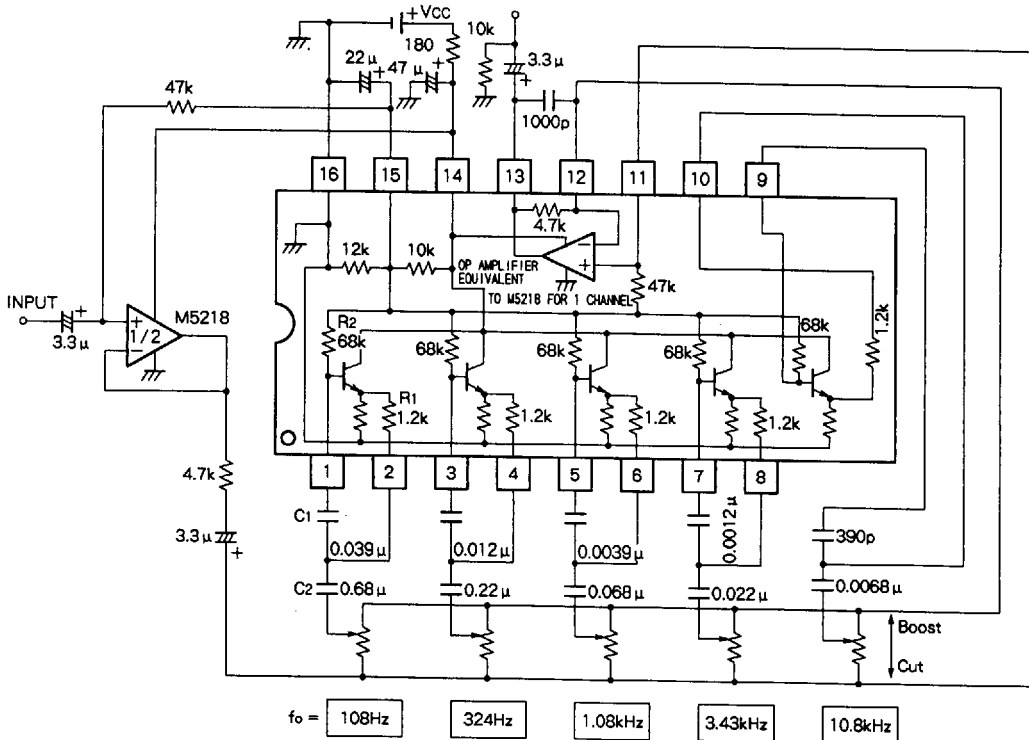
Test item	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9
loc	OFF	1	○	○	○	○	○	1
Gv(FLAT)	ON	1	2	2	2	2	2	1
Gv(BOOST)	f = 108Hz	ON	1	2	2	2	2	1
	f = 343Hz	ON	1	2	2	2	2	1
	f = 1.08kHz	ON	1	2	2	1	2	1
	f = 3.43kHz	ON	1	2	2	1	2	1
	f = 10.8kHz	ON	1	2	2	2	1	1
Gv(CUT)	f = 108Hz	ON	1	3	2	2	2	1
	f = 343Hz	ON	1	2	3	2	2	1
	f = 1.08kHz	ON	1	2	2	3	2	1
	f = 3.43kHz	ON	1	2	2	3	2	1
	f = 10.8kHz	ON	1	2	2	2	3	1
THD	ON	1	2	2	2	2	2	1
VNo(ALLFLAT)	ON	2	2	2	2	2	2	1

Note: The mark "O" applies to both 1 and 2

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5-ELEMENT GRAPHIC EQUALIZER IC

APPLICATION EXAMPLE

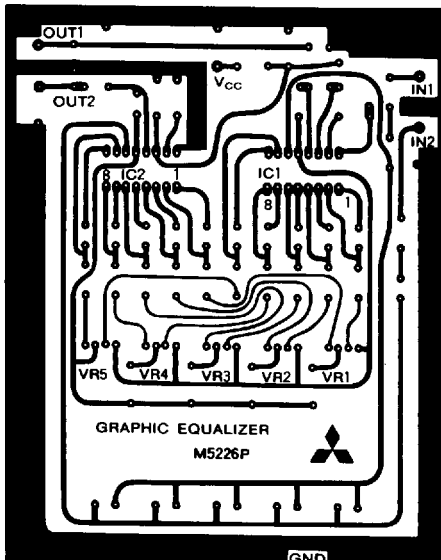


$$\text{RESONANCE FREQUENCY } f_o = \frac{1}{2\pi \sqrt{C_1 \cdot C_2 \cdot R_1 \cdot R_2}} \text{ (Hz)}$$

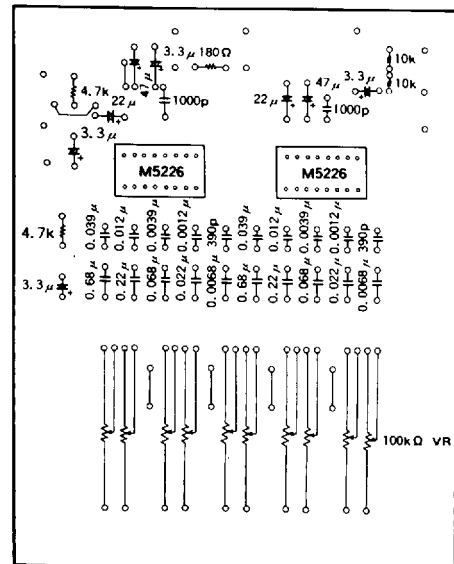
Units Resistance : Ω
Capacitance : F

PRINTED CIRCUIT BOARD FOR CIRCUIT TESTING (TYPICAL APPLICATION EXAMPLE)

PC BOARD PARTS-PLACEMENT DIAGRAM
(COPPER FOIL SIDE)



PC BOARD PARTS-PRACEMENT-DIAGRAM
(PARTS SIDE)



M5226P/FP

5-ELEMENT GRAPHIC EQUALIZER IC

APPLICATION EXAMPLE (7-ELEMENT)

