

FDS8858CZ

Dual N & P-Channel PowerTrench® MOSFET

N-Channel: 30V, 8.6A, 17.0mΩ P-Channel: -30V, -7.3A, 20.5mΩ

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 17mΩ at V_{GS} = 10V, I_D = 8.6A
- Max $r_{DS(on)}$ = 20mΩ at V_{GS} = 4.5V, I_D = 7.3A

Q2: P-Channel

- Max $r_{DS(on)}$ = 20.5mΩ at V_{GS} = -10V, I_D = -7.3A
- Max $r_{DS(on)}$ = 34.5mΩ at V_{GS} = -4.5V, I_D = -5.6A
- High power and handling capability in a widely used surface mount package
- Fast switching speed



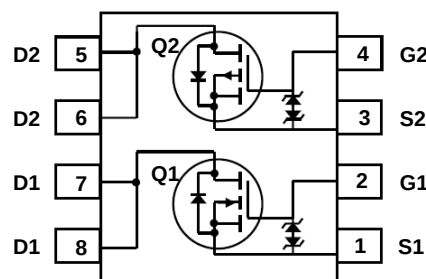
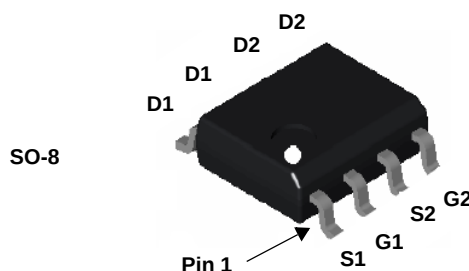
General Description

These dual N and P-Channel enhancement mode power MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Application

- Inverter
- Synchronous Buck



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V _{DS}	Drain to Source Voltage	30	-30	V
V _{GS}	Gate to Source Voltage	±20	±25	V
I _D	Drain Current - Continuous			

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	40	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	78	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS8858CZ	FDS8858CZ	SO-8	13"	12mm	2500 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$ $I_D = -250\mu\text{A}$, $V_{GS} = 0\text{V}$	Q1 Q2	30 -30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C $I_D = -250\mu\text{A}$, referenced to 25°C	Q1 Q2		22 22		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}$, $V_{GS} = 0\text{V}$ $V_{DS} = -24\text{V}$, $V_{GS} = 0\text{V}$	Q1 Q2			1 -1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$ $V_{GS} = \pm 25\text{V}$, $V_{DS} = 0\text{V}$	Q1 Q2			± 10 ± 10	μA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$ $V_{GS} = V_{DS}$, $I_D = -250\mu\text{A}$	Q1 Q2	1 -1	1.6 -2.1	3 -3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C $I_D = -250\mu\text{A}$, referenced to 25°C	Q1 Q2		-5.4 -6.0		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}$, $I_D = 8.6\text{A}$ $V_{GS} = 4.5\text{V}$, $I_D = 7.3\text{A}$ $V_{GS} = 10\text{V}$, $I_D = 8.6\text{A}$, $T_J = 125^\circ\text{C}$	Q1		12.4 15.2 17.7	17.0 20.0 24.3	m Ω
		$V_{GS} = -10\text{V}$, $I_D = -7.3\text{A}$ $V_{GS} = -4.5\text{V}$, $I_D = -5.6\text{A}$ $V_{GS} = -10\text{V}$, $I_D = -7.3\text{A}$, $T_J = 125^\circ\text{C}$	Q2		17.1 26.5 24.0	20.5 34.5 28.8	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{V}$, $I_D = 8.6\text{A}$ $V_{DS} = -5\text{V}$, $I_D = -7.3\text{A}$	Q1 Q2		27 21		S

Dynamic Characteristics

C_{iss}	Input Capacitance	Q1 $V_{DS} = 15\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$	Q1 Q2		905 1675	1205 2230	pF
C_{oss}	Output Capacitance	Q2	Q1 Q2		180 290	240 390	pF
C_{rss}	Reverse Transfer Capacitance	$V_{DS} = -15\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$	Q1 Q2		110 260	165 390	pF
R_g	Gate Resistance	$f = 1\text{MHz}$	Q1 Q2		1.3 4.4		Ω

Switching Characteristics

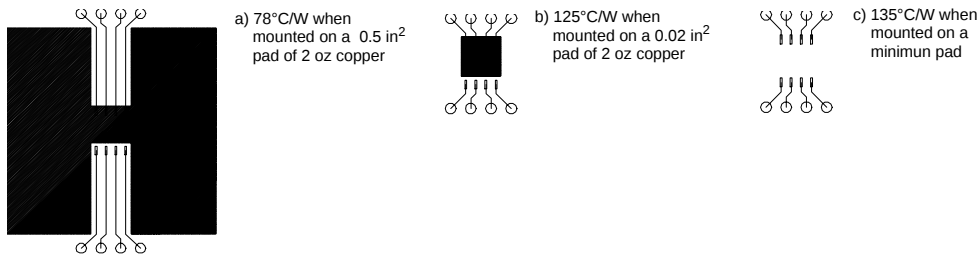
$t_{d(on)}$	Turn-On Delay Time	Q1	Q1 Q2		7 9	14 18	ns
t_r	Rise Time	$V_{DD} = 15\text{V}$, $I_D = 8.6\text{A}$, $V_{GS} = 10\text{V}$, $R_{GEN} = 6\Omega$	Q1 Q2		3 10	10 20	ns
$t_{d(off)}$	Turn-Off Delay Time	Q2	Q1 Q2		19 33	35 53	ns
t_f	Fall Time	$V_{DD} = -15\text{V}$, $I_D = -7.3\text{A}$, $V_{GS} = -10\text{V}$, $R_{GEN} = 6\Omega$	Q1 Q2		3 16	10 29	ns
$Q_{g(TOT)}$	Total Gate Charge	Q1 $V_{GS} = 10\text{V}$, $V_{DD} = 15\text{V}$, $I_D = 8.6\text{A}$	Q1 Q2		17 33	24 46	nC
Q_{gs}	Gate to Source Charge	Q2	Q1 Q2		2.7 6.1		nC
Q_{gd}	Gate to Drain "Miller" Charge	$V_{GS} = -10\text{V}$, $V_{DD} = -15\text{V}$, $I_D = -7.3\text{A}$	Q1 Q2		3.4 8.5		nC

Electrical Characteristics $T_J = 25^{\circ}\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics							
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 8.6\text{A}$ (Note 2) $V_{GS} = 0\text{V}, I_S = -7.3\text{A}$ (Note 2)	Q1 Q2		0.8 0.9	1.2 -1.2	V
t_{rr}	Reverse Recovery Time	Q1 $I_F = 8.6\text{A}, di/dt = 100\text{A/s}$	Q1 Q2		25 28	38 42	ns
Q_{rr}	Reverse Recovery Charge	Q2 $I_F = -7.3\text{A}, di/dt = 100\text{A/s}$	Q1 Q2		19 22	29 33	nC

Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

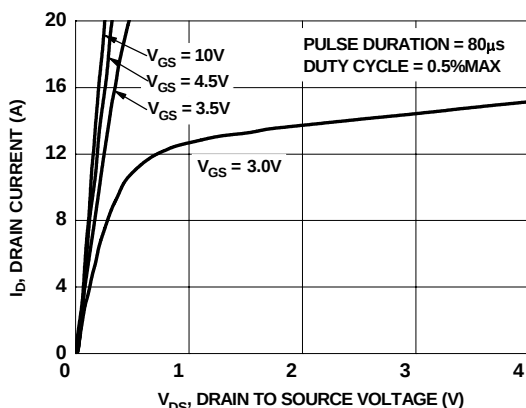


Figure 1. On-Region Characteristics

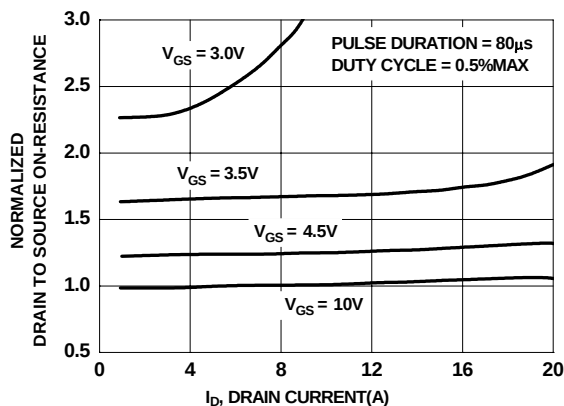


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

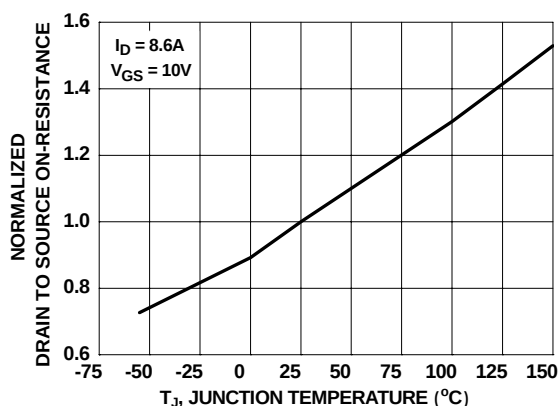


Figure 3. Normalized On-Resistance vs Junction Temperature

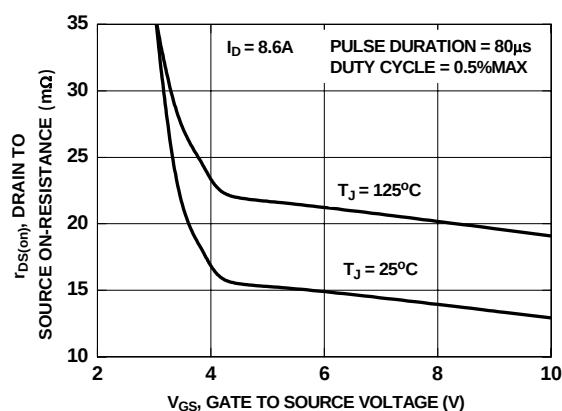


Figure 4. On-Resistance vs Gate to Source Voltage

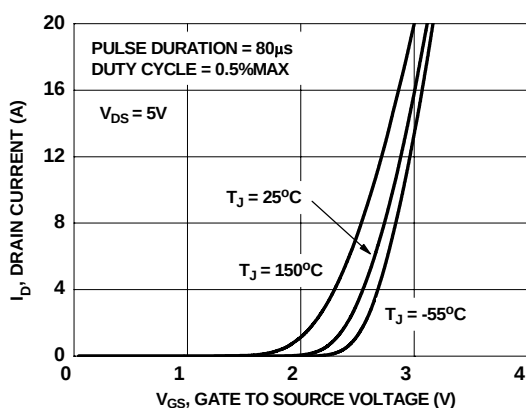


Figure 5. Transfer Characteristics

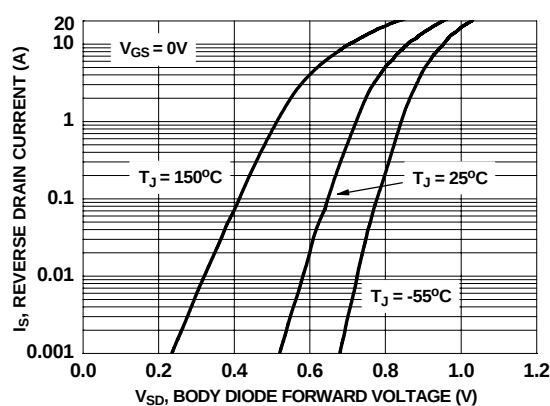


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

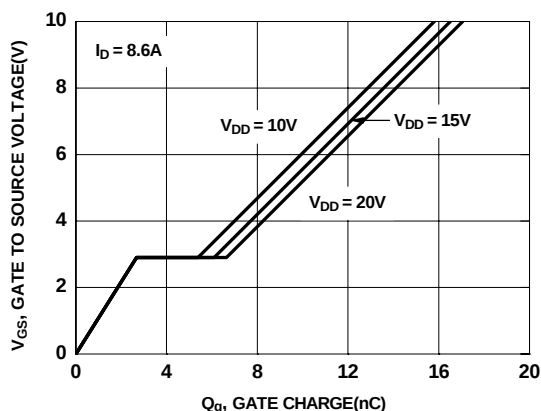


Figure 7. Gate Charge Characteristics

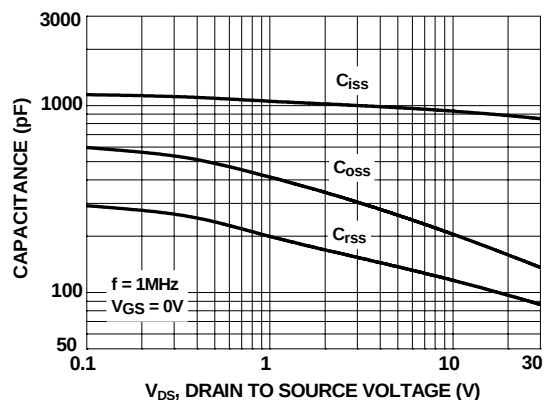


Figure 8. Capacitance vs Drain to Source Voltage

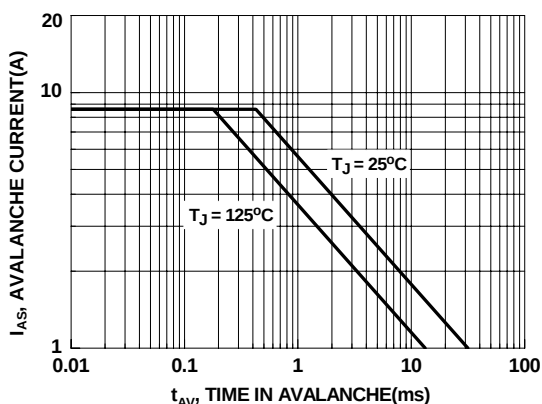


Figure 9. Unclamped Inductive Switching Capability

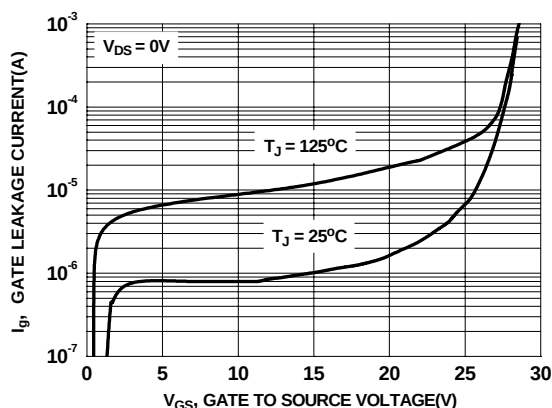


Figure 10. Gate Leakage Current vs Gate to Source Voltage

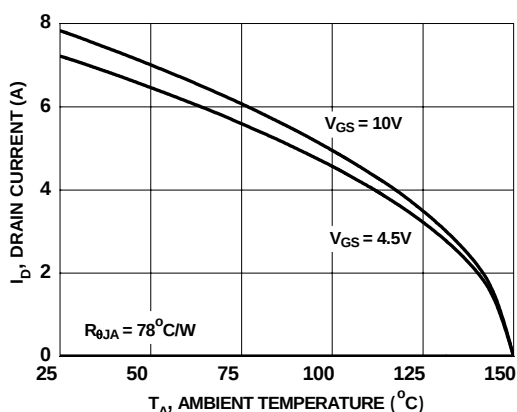


Figure 11. Maximum Continuous Drain Current vs Ambient Temperature

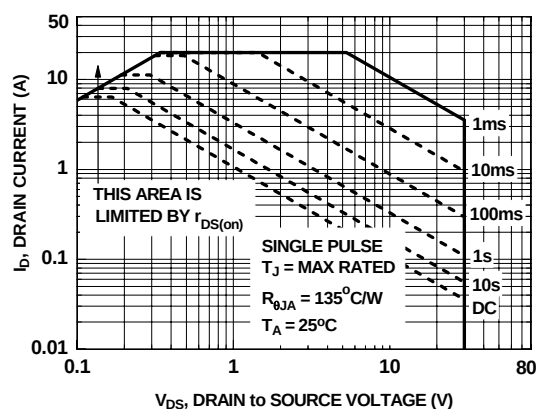


Figure 12. Forward Bias Safe Operating Area

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

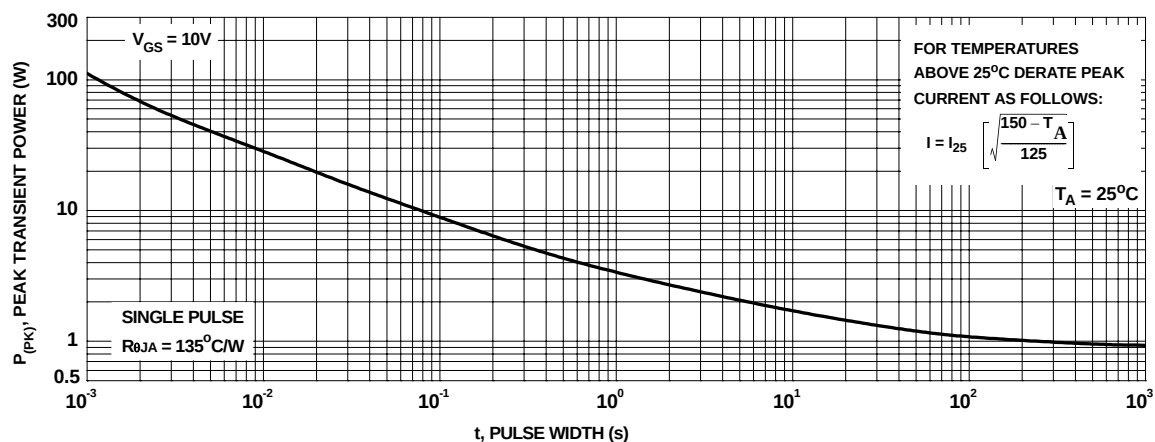


Figure 13. Single Pulse Maximum Power Dissipation

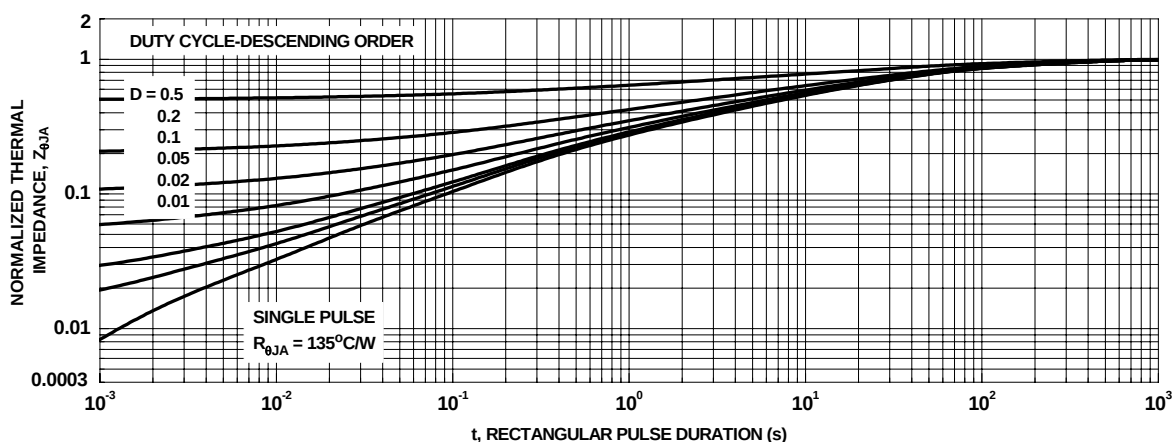


Figure 14. Transient Thermal Response Curve

Typical Characteristics (Q2 P-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

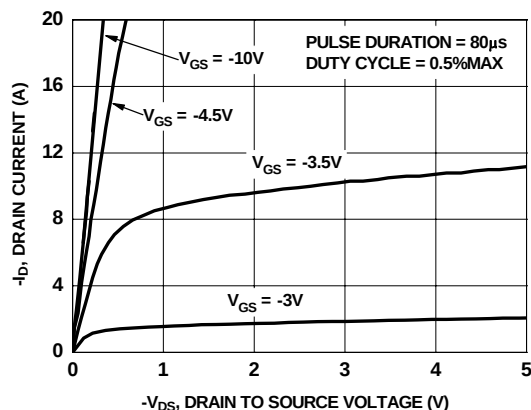


Figure 15. On-Region Characteristics

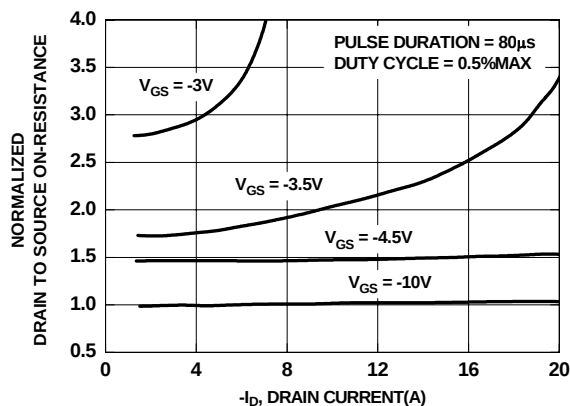


Figure 16. Normalized on-Resistance vs Drain Current and Gate Voltage

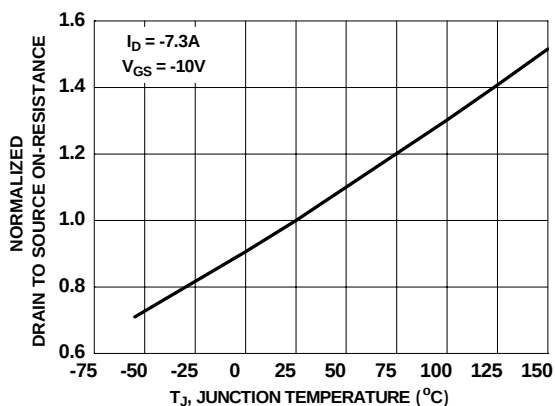


Figure 17. Normalized On-Resistance vs Junction Temperature

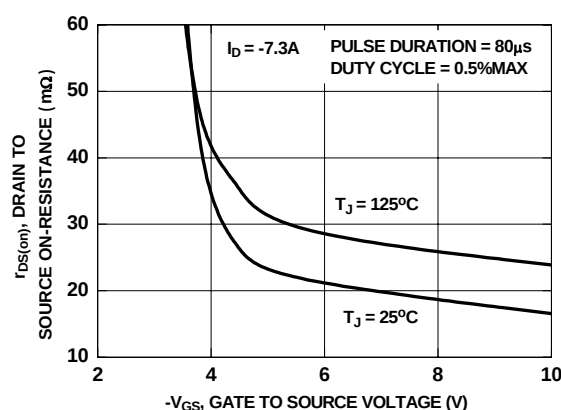


Figure 18. On-Resistance vs Gate to Source Voltage

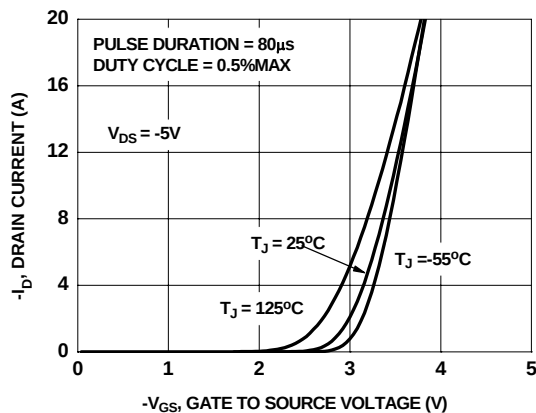


Figure 19. Transfer Characteristics

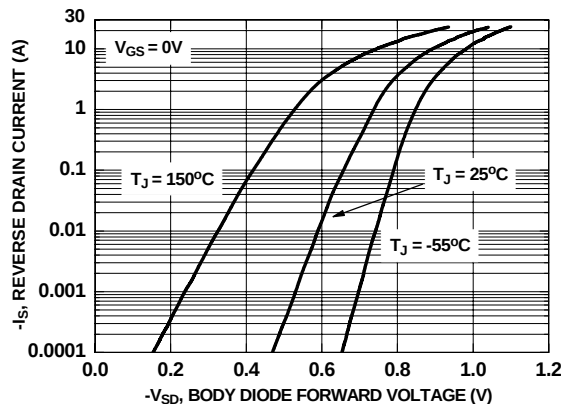


Figure 20. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics(Q2 P-Channel) $T_J = 25^{\circ}\text{C}$ unless otherwise noted

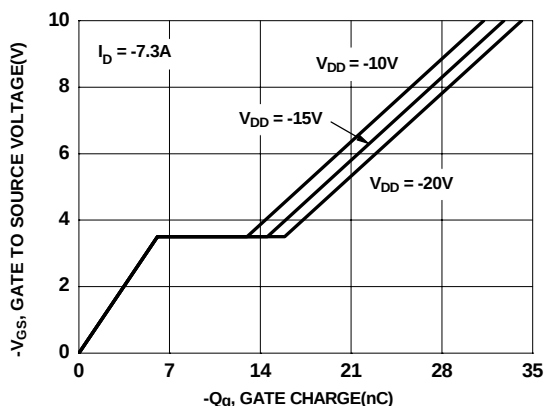


Figure 21. Gate Charge Characteristics

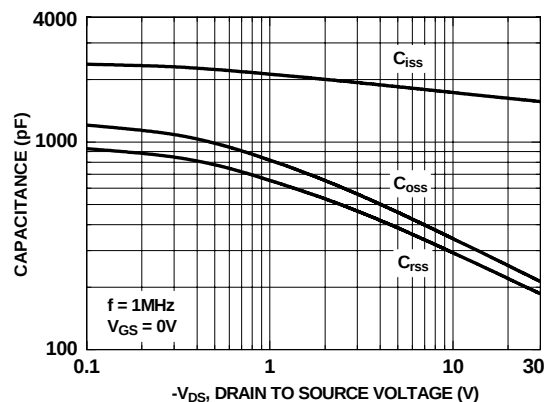


Figure 22. Capacitance vs Drain to Source Voltage

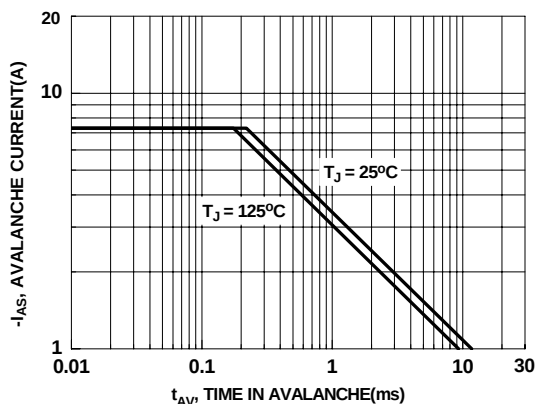


Figure 23. Unclamped Inductive Switching Capability

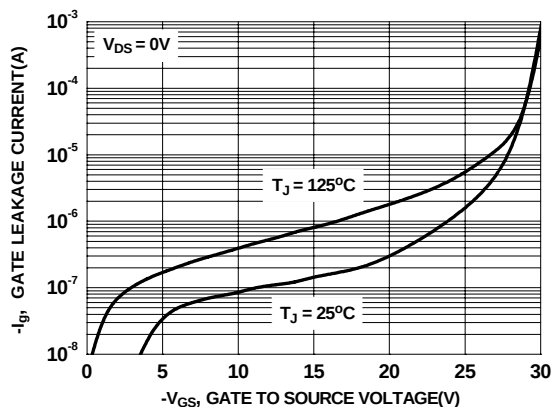


Figure 24. Gate Leakage Current vs Gate to Source Voltage

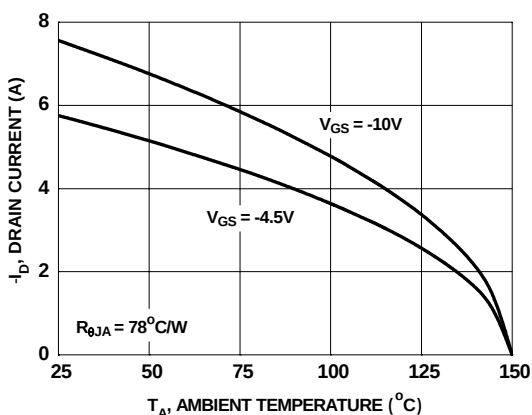


Figure 25. Maximum Continuous Drain Current vs Ambient Temperature

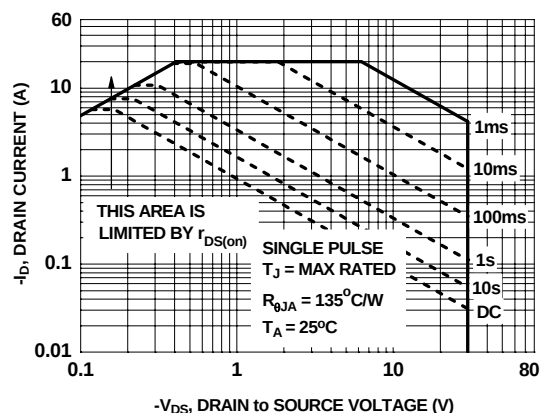


Figure 26. Forward Bias Safe Operating Area

Typical Characteristics(Q2 P-Channel) $T_J = 25^{\circ}\text{C}$ unless otherwise noted

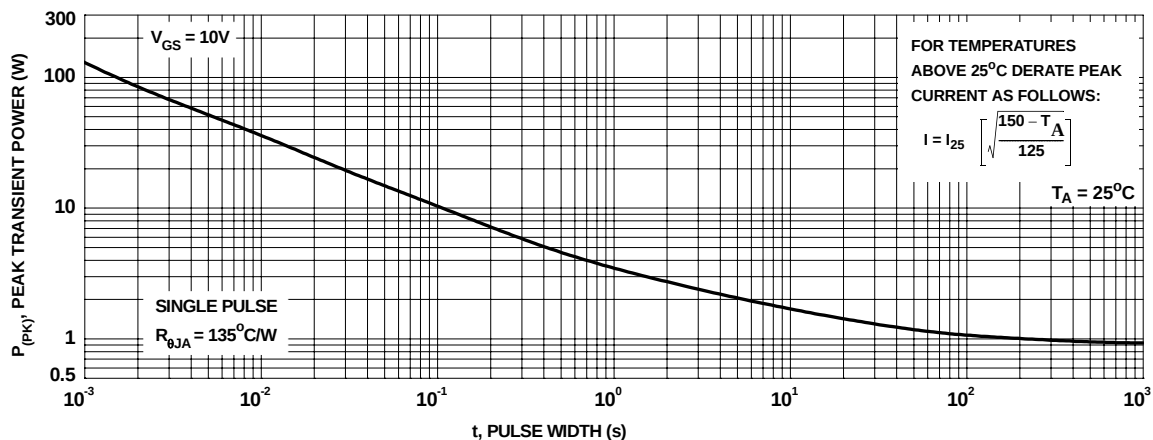


Figure 27. Single Pulse Maximum Power Dissipation

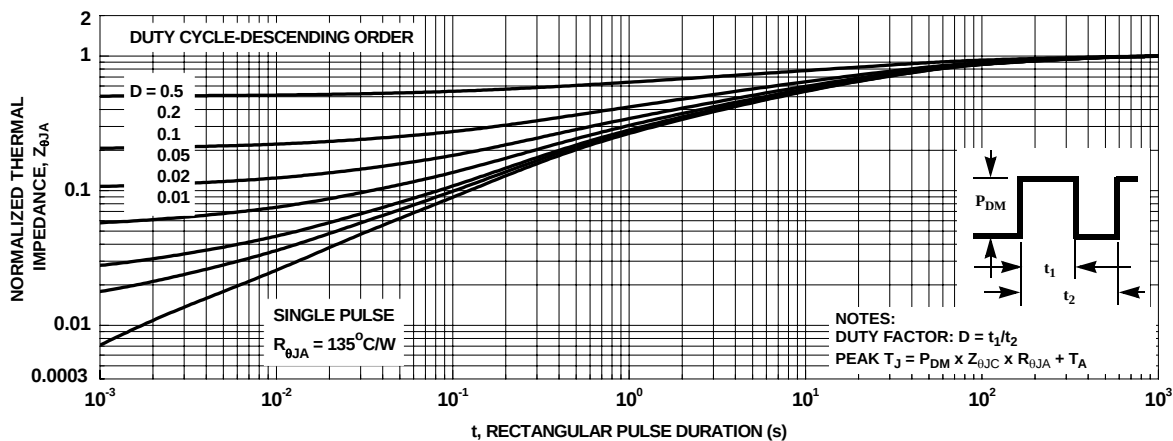


Figure 28. Transient Thermal Response Curve



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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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