

CET

CEP13N5/CEB13N5 CEF13N5

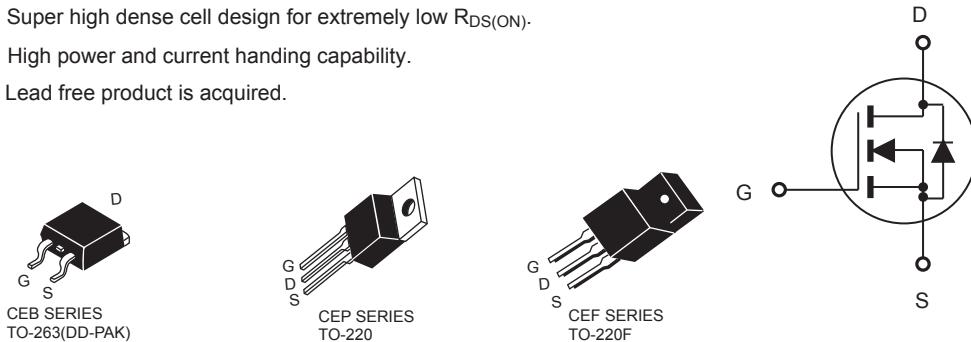
N-Channel Enhancement Mode Field Effect Transistor

PRELIMINARY

FEATURES

Type	V _{DSS}	R _{DS(ON)}	I _D	@V _{GS}
CEP13N5	500V	0.48Ω	13A	10V
CEB13N5	500V	0.48Ω	13A	10V
CEF13N5	500V	0.48Ω	13A ^d	10V

- Super high dense cell design for extremely low R_{DS(ON)}.
- High power and current handing capability.
- Lead free product is acquired.



ABSOLUTE MAXIMUM RATINGS T_C = 25°C unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263	TO-220F	
Drain-Source Voltage	V _{DS}	500		V
Gate-Source Voltage	V _{GS}	±30		V
Drain Current-Continuous @ T _C = 25°C	I _D	13	13 ^d	A
Drain Current-Continuous @ T _C = 100°C	I _D	8	8 ^d	A
Drain Current-Pulsed ^a	I _{DM} ^e	52	52 ^d	A
Maximum Power Dissipation @ T _C = 25°C - Derate above 25°C	P _D	214	60	W
		1.43	0.4	W/°C
Operating and Store Temperature Range	T _J , T _{stg}	-55 to 175		°C

Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	R _{θJC}	0.7	2.5	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.5	65	°C/W

This is preliminary information on a new product in development now .
Details are subject to change without notice .

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<http://www.cetsemi.com>



CEP13N5/CEB13N5 □

CEF13N5

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}} = 0\text{V}, I_{\text{D}} = 250\mu\text{A}$	500			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = 500\text{V}, V_{\text{GS}} = 0\text{V}$		1		μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{\text{GS}} = 30\text{V}, V_{\text{DS}} = 0\text{V}$		100		nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{\text{GS}} = -30\text{V}, V_{\text{DS}} = 0\text{V}$		-100		nA
On Characteristics^b						
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{GS}} = V_{\text{DS}}, I_{\text{D}} = 250\mu\text{A}$	2		4	V
Static Drain-Source On-Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10\text{V}, I_{\text{D}} = 6.5\text{A}$		0.38	0.48	Ω
Forward Transconductance	g_{FS}	$V_{\text{DS}} = 25\text{V}, I_{\text{D}} = 6.5\text{A}$		10		S
Dynamic Characteristics^c						
Input Capacitance	C_{iss}	$V_{\text{DS}} = 25\text{V}, V_{\text{GS}} = 0\text{V}, f = 1.0 \text{ MHz}$		2100		pF
Output Capacitance	C_{oss}			220		pF
Reverse Transfer Capacitance	C_{rss}			7		pF
Switching Characteristics^c						
Turn-On Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = 250\text{V}, I_{\text{D}} = 13\text{A}, V_{\text{GS}} = 10\text{V}, R_{\text{GEN}} = 25\Omega$		42	84	ns
Turn-On Rise Time	t_r			62	124	ns
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$			130	260	ns
Turn-Off Fall Time	t_f			25	50	ns
Total Gate Charge	Q_g	$V_{\text{DS}} = 400\text{V}, I_{\text{D}} = 13\text{A}, V_{\text{GS}} = 10\text{V}$		50	66	nC
Gate-Source Charge	Q_{gs}			11		nC
Gate-Drain Charge	Q_{gd}			19		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current	I_s^f				13	A
Drain-Source Diode Forward Voltage ^b	V_{SD}^g	$V_{\text{GS}} = 0\text{V}, I_s = 13\text{A}$			1.4	V
Notes :						
a.Repetitive Rating : Pulse width limited by maximum junction temperature .						
b.Pulse Test : Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.□						
c.Guaranteed by design, not subject to production testing.□						
d.Limited only by maximum temperature allowed .						
e.Pulse width limited by safe operating area .						
f.Full package $I_s(\text{max}) = 6.6\text{A}$.						
g.Full package V_{SD} test condition $I_s = 6.6\text{A}$.						

CEP

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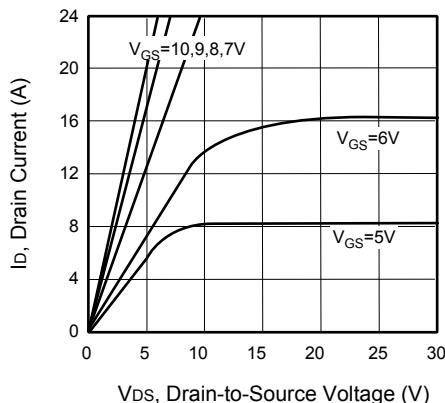


Figure 1. Output Characteristics

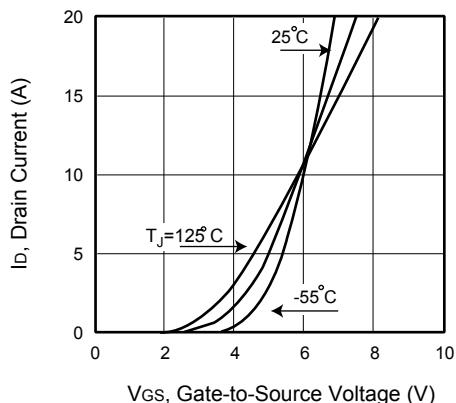


Figure 2. Transfer Characteristics

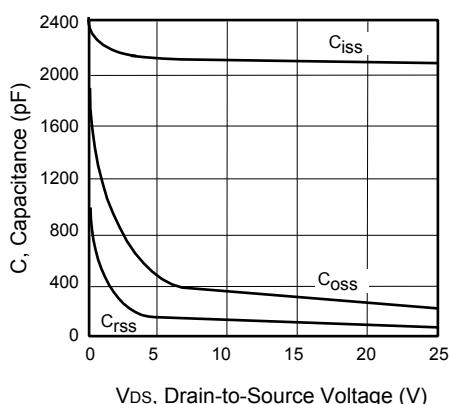


Figure 3. Capacitance

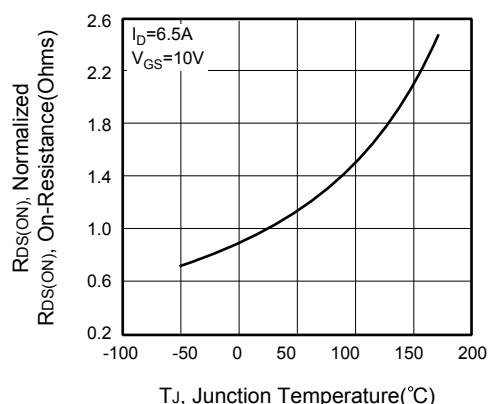


Figure 4. On-Resistance Variation with Temperature

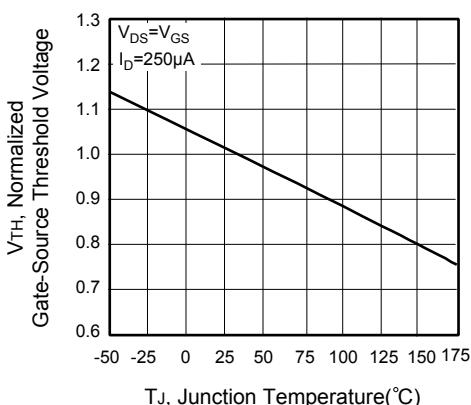


Figure 5. Gate Threshold Variation with Temperature

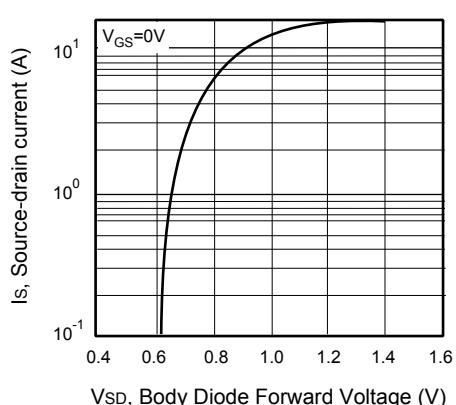


Figure 6. Body Diode Forward Voltage Variation with Source Current

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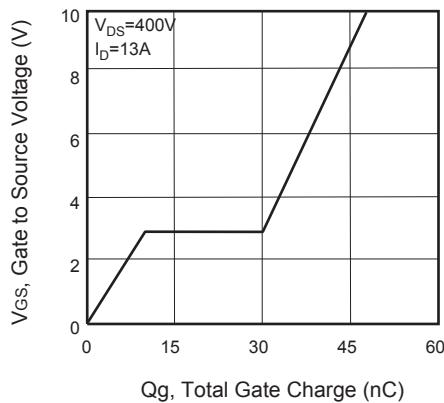


Figure 7. Gate Charge

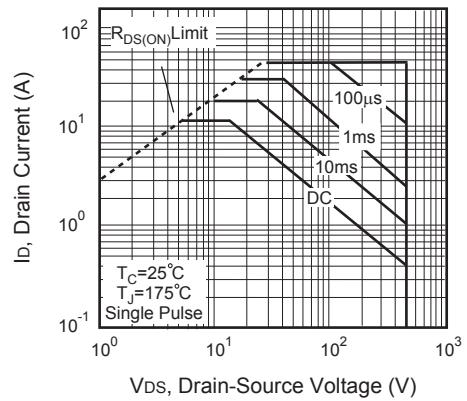


Figure 8. Maximum Safe Operating Area



Figure 9. Switching Test Circuit

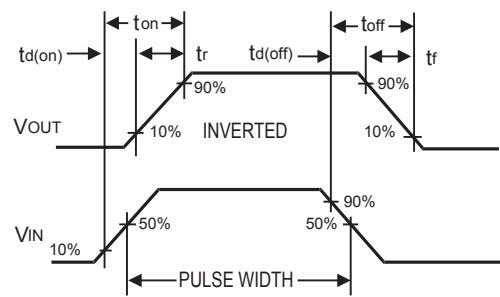


Figure 10. Switching Waveforms

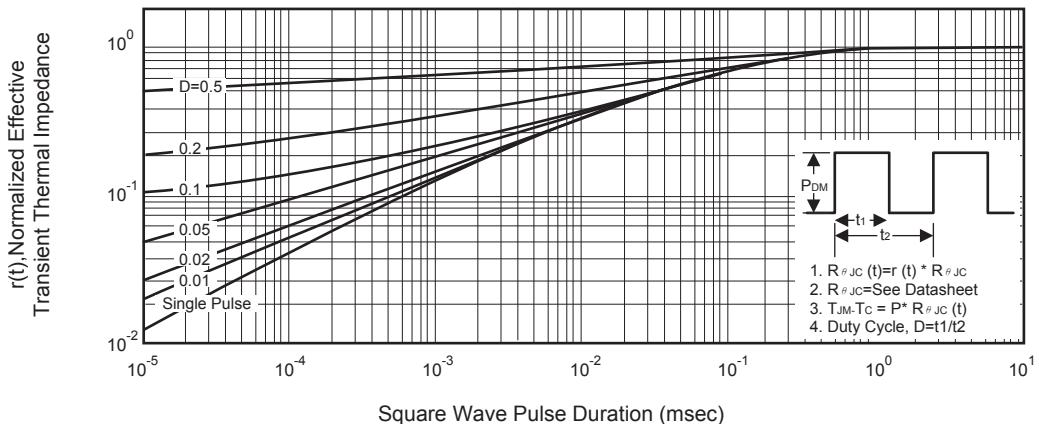


Figure 11. Normalized Thermal Transient Impedance Curve