National Semiconductor

PRELIMINARY
October 2000

LMX9402
Frequency Synthesizer Module

General Description

The Frequency Synthesizer Module is a Low Temperature Co-fired Ceramic (LTCC) RF module consisting of a high performance frequency synthesizer, loop filter, and voltage controlled oscillator (VCO). The frequency synthesizer is fabricated using National's ABiC BiCMOS process (f_T = 14 GHz). The loop filter and VCO are fabricated on National's Low Temperature Co-fired Ceramics.

The Frequency Synthesizer Module can be used for local oscillator applications. Using a digital phase locked loop technique, the on board frequency synthesizer can generate a very stable, low noise local oscillator. Serial data is transferred into the module using a three wire interface. The loop filter is designed for fast lock times and maximum attenuation of reference spurs.

The module is available in a Ball Grid Array 560 mil X 560 mil X 220 mil package.

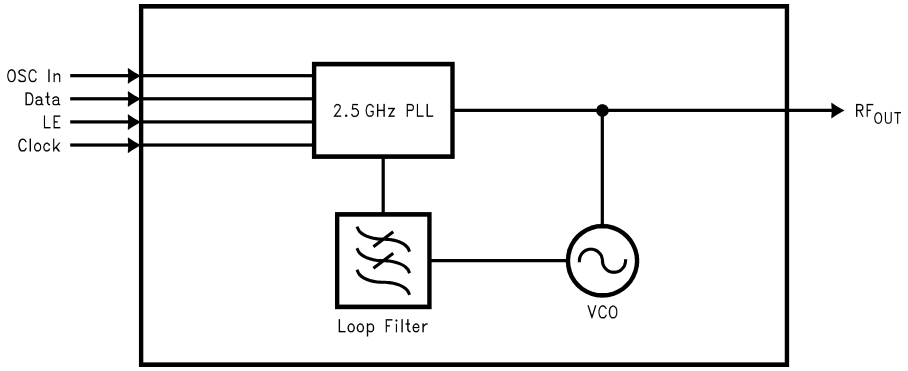
Features

- Low phase noise tunable local oscillator
- Low current consumption
- LMX2330A 2.5 GHz PLLatinum™ in module

Applications

- DCS wireless cellular systems
- Fixed wireless communications

Functional Block Diagram



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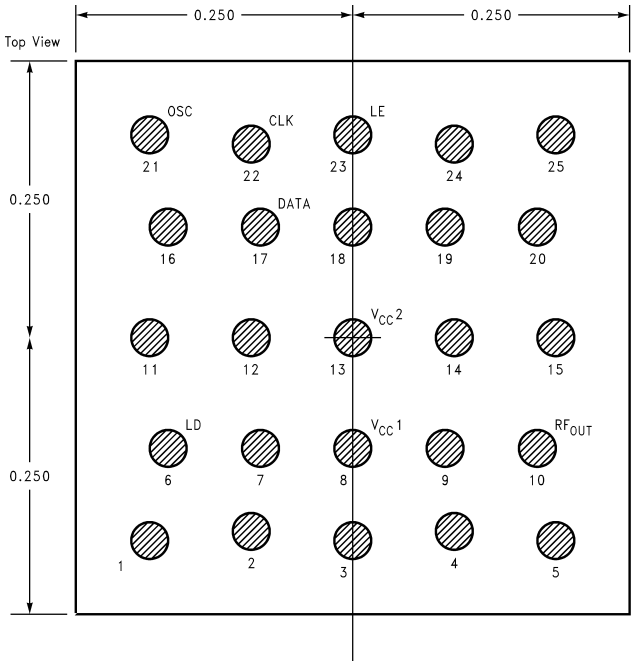
Ordering Information

Package	Temp. Range -10˚C to +85˚C	Transport Media	NSC Package Drawing
CBGA	LMX9402BL1577X	Tape and Reels	SB25A
CBGA	LMX9402BL1501X	Tape and Reels	SB25A
CBGA	LMX9402BL1619X	Tape and Reels	SB25A
CBGA	LMX9402BL1701X	Tape and Reels	SB25A

Connection Diagram



Top View 25-Pin CBGA Package
See NS Package Number SB25A

Pin Descriptions

Pin No.	Pin Name	I/O	Description
1,2,3,4,5	GND	—	Ground.
6	LD	O	Multiplexed output of the RF programmable dividers, reference dividers, or RF Lock Detect. Normally used as RF Lock Detect.
7	GND	—	Ground.
8	V_{CC1}	—	Power supply voltage input to PLL.
9	GND	—	Ground.
10	RFOUT	O	VCO Frequency Output.
11, 12	GND	—	Ground.
13	V_{CC2}	—	Power supply voltage input to VCO
14, 15, 16	GND	—	Ground.
17	Data	I	Binary serial data input. Data entered MSB first. LSB is control bit. High impedance CMOS input.
18, 19, 20	GND	—	Ground.
21	OSC_{IN}	I	Reference Oscillator input.
22	CLK	I	High impedance CMOS Clock input. Data is clocked in on the rising edge, into the various counters and registers.
23	LE	I	Load Enable input (with internal pull-up resistor). When LE Load Enable transitions HIGH, data stored in the shift registers is loaded into the appropriate latch (control bit dependent). Clock must be low when LE toggles high or low.
24, 25	GND	—	Ground.

Absolute Maximum Ratings (Note 1)

Power Supply Voltage (V_{CC})	4.75 to 5.5 V
Storage Temperature Range (T_S)	10˚C to 150˚C
ESD - Whole Body Model (Note 2)	TBD

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Conditions indicate conditions for which the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: This device is a high performance RF integrated circuit and is ESD sensitive. Handling and assembly of this device should be done on ESD protected workstations.

Recommended Operating Conditions (Note 1)

Supply Voltage (V_{CC})	
Min	4.75 V
Typ	5.0 V
Max	5.5 V
Operating Temperature (T_A)	−10˚C to +85˚C

Frequency Synthesizer Electrical Characteristics

Note: all specifications on this table are for the BL1501 version unless noted in bold.

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
I_{CC}	Power Supply Current	V_{CC1} and V_{CC2}		18	32	mA
f_{OSC}	Crystal Reference Frequency			13	40	MHz
f_{REF}	Reference Frequency			200		kHz
LBW	Loop Bandwidth			20		kHz
f_{VCO}	Tuning Frequency		1464.2		1538.8	MHz
f_{VCO}	**BL1577 Tuning Frequency**		**1540.2**		**1614.8**	**MHz**
f_{VCO}	**BL1619 Tuning Frequency**		**1589**		**1650**	**MHz**
f_{VCO}	**BL1701 Tuning Frequency**		**1680**		**1740**	**MHz**
P_{OUT}	Output Level		0	3	+6	dBm
∫ (f_m)	Single Side Band Phase Noise	f_m = 5 kHz		−82		dBc/Hz
		$f_m \geq$ 800 kHz		−142		dBc/Hz
∫ (f_m)	**BL1577 Single Side Band Phase Noise**	**f_m = 2 kHz**		**−82**	**−80**	**dBc/Hz**
		$f_m \geq$ 800 kHz		**−142**	**−140**	**dBc/Hz**
∫ (f_m)	**BL1619 Single Side Band Phase Noise**	**f_m = 2 kHz**			**−81**	**dBc/Hz**
		$f_m \geq$ 800 kHz			**−141**	**dBc/Hz**
∫ (f_m)	**BL1701 Single Side Band Phase Noise**	**f_m = 2 kHz**			**−81**	**dBc/Hz**
		$f_m \geq$ 800 kHz			**−141**	**dBc/Hz**
	Spurious Reference Sidebands	200 kHz Offset		−80	−60	dBc
		400 kHz Offset		−90	−80	dBc
		600 kHz Offset		−95	−90	dBc
		800 kHz Offset		−96	−95	dBc
	Nth Spurious Harmonic	2nd Harmonic		−15	−10	dBc
	Spurious Non Harmonic				−100	dBc
T_{LOCK}	Frequency Lock Time (MAX)	Within 10˚ of Final Frequency		400	500	µs
T_{LOCK}	**BL1577 Frequency Lock Time (MAX)**	**Within 10˚ of Final Frequency**			**500**	**µs**
T_{LOCK}	**BL1619 Frequency Lock Time (MAX)**	**Within 10˚ of Final Frequency**			**500**	**µs**
T_{LOCK}	**BL1701 Frequency Lock Time (MAX)**	**Within 10˚ of Final Frequency**			**500**	**µs**

Voltage Controlled Oscillator Electrical Characteristics

Note: all specifications on this table are for the BL1501 version unless noted in bold.

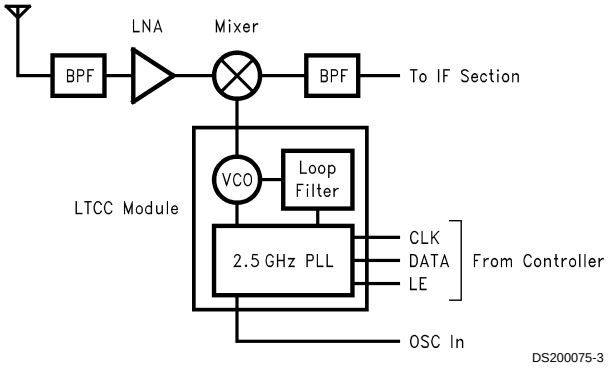
Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
I_{CC}	Power Supply Current	V_{CC2} only		12	18	mA
f_{VCO}	Tune Range	Tune Voltage 0V to 5V	1420		1570	MHz
f_{VCO}	**BL1577 Tune Range**	**Tune Voltage 0V to 5V**	**1480**		**1640**	**MHz**
f_{VCO}	**BL1619 Tune Range**	**Tune Voltage 0V to 5V**	**1565**		**1670**	**MHz**
f_{VCO}	**BL1701 Tune Range**	**Tune Voltage 0V to 5V**	**1660**		**1760**	**MHz**
K_V	Gain	f_{VCO} = 1540.2 to 1614.8 MHz		32		MHz/V
P_{OUT}	Output Level		0	3	+6	dBm
∫ (f_m)	Single Side Band Phase Noise	f_m = 10 kHz		−102		dBc/Hz
		f_m = 100 kHz		−122		dBc/Hz
		f_m = 1000 kHz		−142		dBc/Hz
	Nth Spurious Harmonic	2nd Harmonic		−15	−10	dBc

DC Electrical Characteristics

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
V_{IH}	High Level Input Voltage		V_{CC} − 0.8			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{IN}	Input Current	GND < V_{IN} < V_{CC}	−1.0		1.0	µA
t_{CS}	Data to Clock Set Up Time		50			ns
t_{CH}	Data to Clock Hold Time		10			ns
t_{CWH}	Clock Pulse Width High		50			ns
t_{CWL}	Clock Pulse Width Low		50			ns
t_{ES}	Clock to Load Enable Set Up Time		50			ns
t_{EW}	Load Enable Pulse Width		50			ns

Note 3: DC Electrical Characteristics for the digital section apply to the power down pin and the MICROWIRE™ Interface.

Typical Application Example



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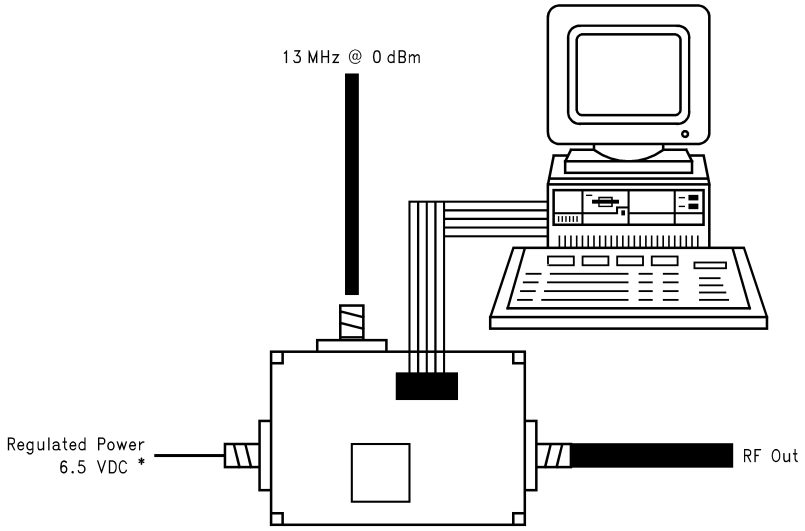
Evaluation Board Setup



* The VCO is powered through a 5.0V regulator on evaluation board.

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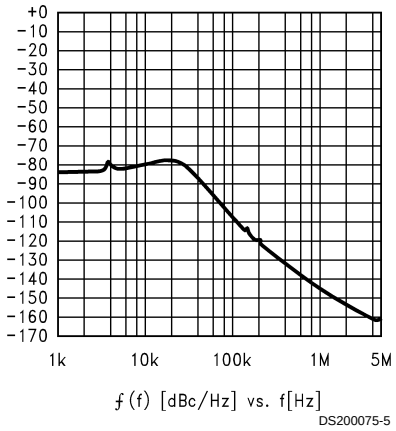
Typical Phase Noise

Typical Phase Noise (BL1501)



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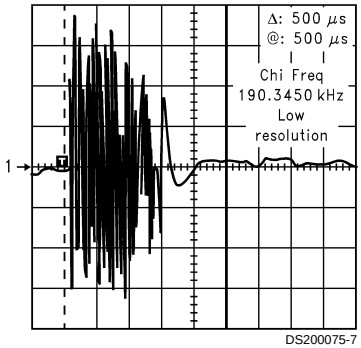
Note: Phase noise was measured using HP3048, FM Discriminator method. Delay line approximately 95 nS.

Typical Lock Time BL1577A



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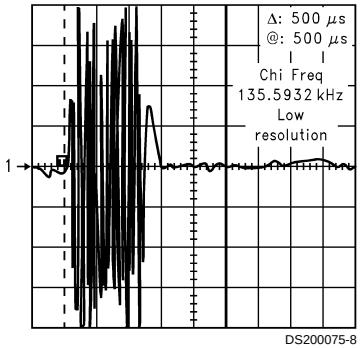

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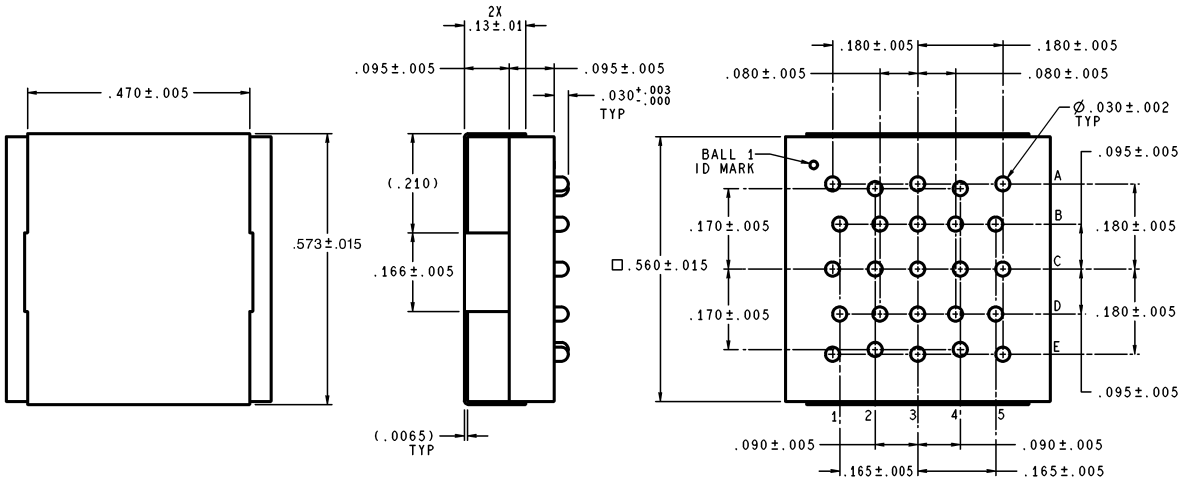
Physical Dimensions inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN INCHES

SB25A (Rev B)

25-Pin CBGA Package
Order Number LMX9402SB,
NS Package Number SB25A

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