

LMH0056

HD/SD SDI Reclocker with 4:1 Input Multiplexer

General Description

The LMH0056 HD/SD SDI Reclocker with 4:1 Input Multiplexer is a monolithic integrated circuit that retimes bit-serial digital video data conforming to the SMPTE 259M (A & C) and SMPTE 292M standards. The LMH0056 operates at serial data rates of 143 Mbps, 270 Mbps, 1.483 Gbps and 1.485 Gbps. The LMH0056 supports DVB-ASI operation at 270 Mbps. The LMH0056 includes an integrated 4:1 input multiplexer for selecting one of four input data streams for retiming.

The LMH0056 automatically detects the incoming data rate and adjusts itself to retime the incoming data to suppress accumulated jitter. The LMH0056 recovers the serial data-rate clock and optionally provides it as an output. The LMH0056 has two differential serial data outputs; the second output may be selected as a low-jitter, data-rate clock output. Controls and indicators are: serial clock or second serial data output select, manual rate select input, SD/HD rate indicator output, lock detect output, auto/manual data bypass and output mute. The serial data inputs, outputs, and serial data-rate clock outputs are differential LVPECL compatible. The CML serial data and serial data-rate clock outputs are suitable for driving 100Ω differentially terminated networks. The control logic inputs and outputs are LVC MOS compatible.

The LMH0056 is powered from a single 3.3V supply. Power dissipation is typically 350 mW. The device is housed in a 48-pin LLP package.

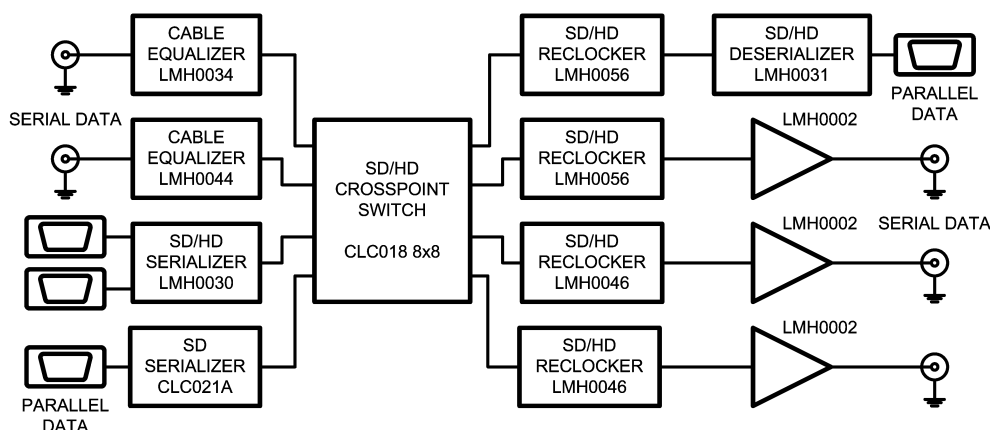
Features

- Supports SMPTE 259M (A & C) and SMPTE 292M serial digital video standards
- Supports 143 Mbps, 270 Mbps, 1.483 Gbps, and 1.485 Gbps serial data rate operation
- Supports DVB-ASI at 270 Mbps
- Single 3.3V supply operation
- 350 mW typical power consumption
- Integrated 4:1 multiplexed input
- Two differential, reclocked outputs
- Choice of second reclocked output or low-jitter, differential, data-rate clock output
- Single 27 MHz external crystal or reference clock input
- Manual rate select input
- SD/HD operating rate indicator output
- Lock Detect indicator output
- Output mute function for data and clock
- Auto/Manual reclocker bypass
- Differential LVPECL compatible serial data inputs and outputs
- LVC MOS control inputs and indicator outputs
- 48-Pin LLP package
- Industrial temperature range: -40°C to +85°C

Applications

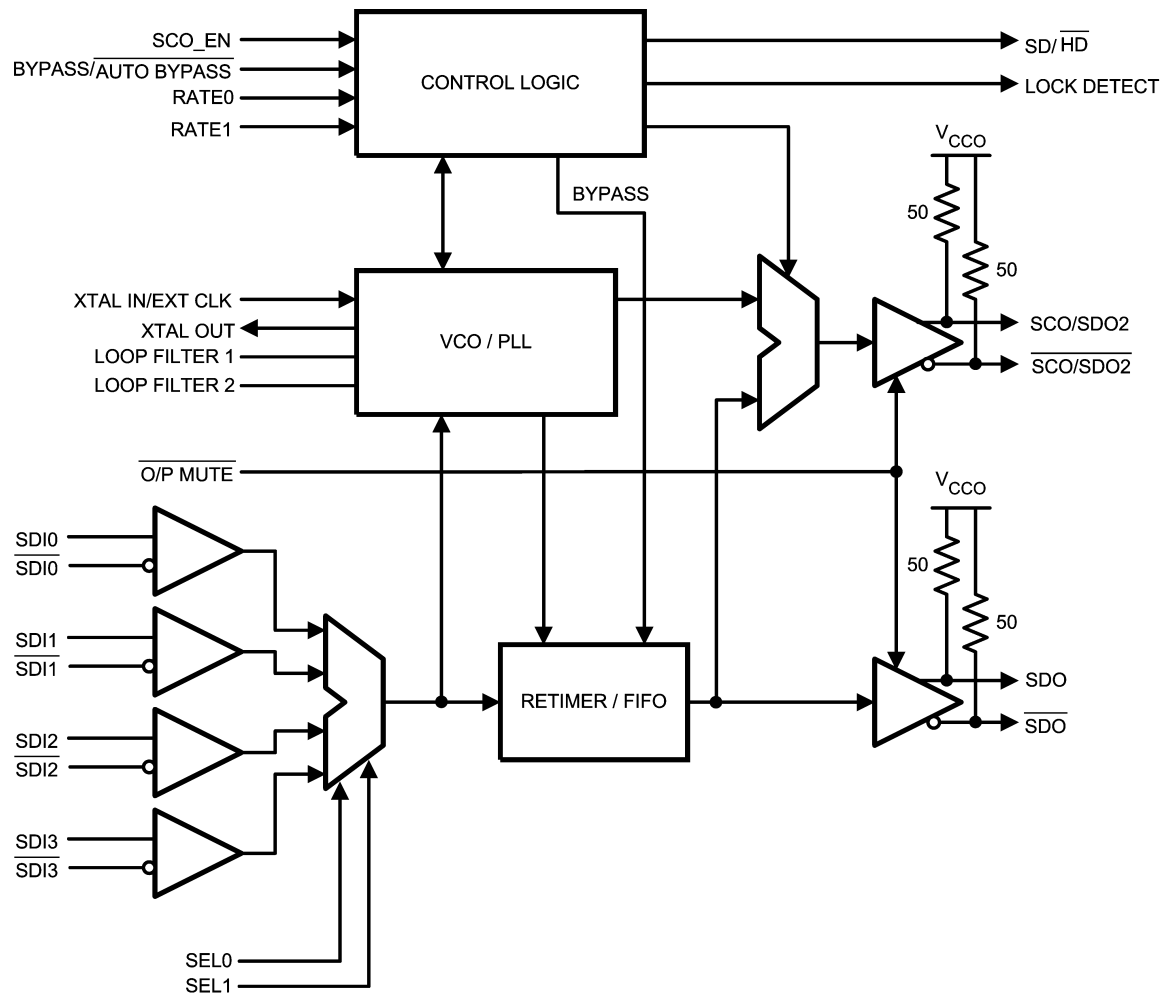
- SDTV/HDTV serial digital video interfaces for:
 - Digital video routers and switchers
 - Digital video processing and editing equipment
 - DVB-ASI equipment
 - Video standards and format converters

Typical Application



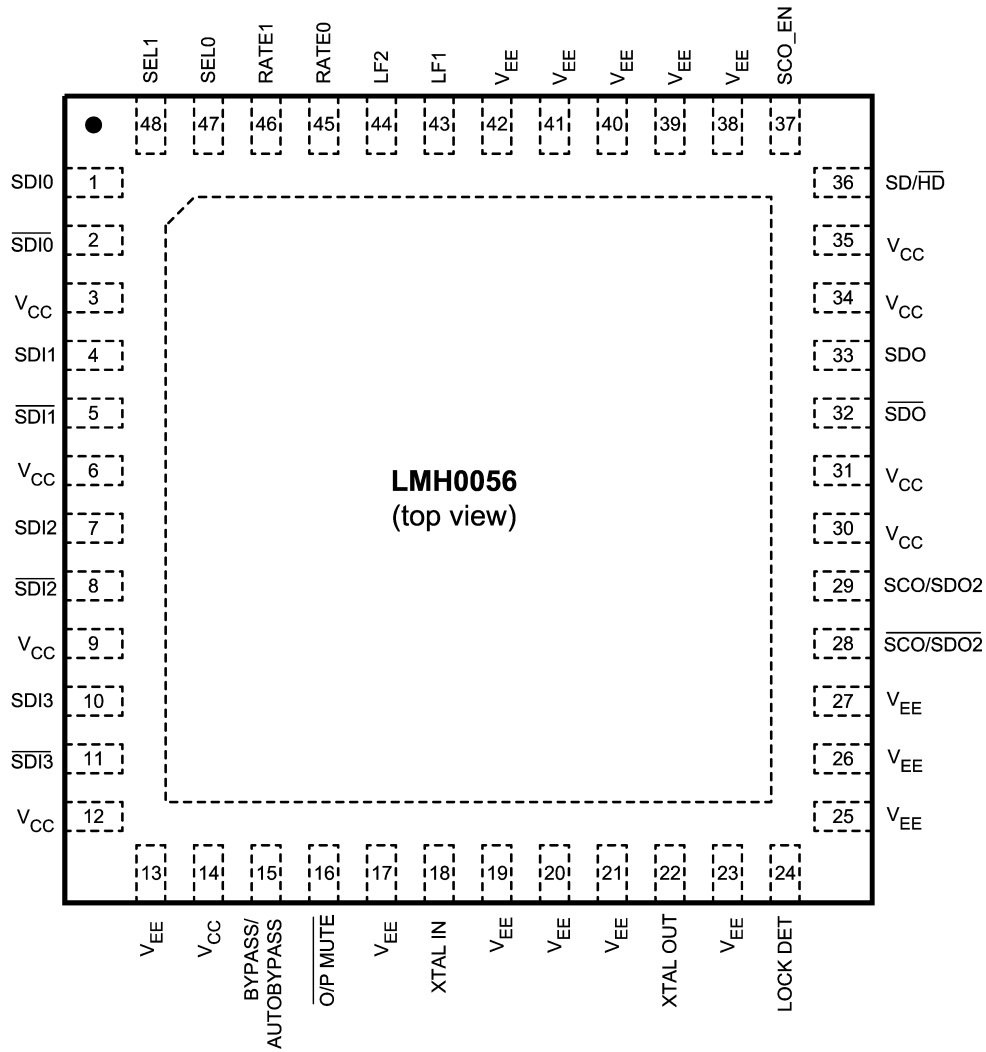
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Block Diagram



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Connection Diagram



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The exposed die attach pad is the negative electrical terminal for this device. It must be connected to the negative power supply voltage.

48-Pin LLP
Order Number LMH0056SQ
See NS Package Number SQA-48C

Pin Descriptions

Pin	Name	Description
1	SDI0	Data Input 0 true
2	$\overline{\text{SDI0}}$	Data Input 0 complement
3	V _{CC}	Positive power supply input
4	SDI1	Data Input 1 true
5	$\overline{\text{SDI1}}$	Data Input 1 complement
6	V _{CC}	Positive power supply input
7	SDI2	Data Input 2 true
8	$\overline{\text{SDI2}}$	Data Input 2 complement
9	V _{CC}	Positive power supply input
10	SDI3	Data Input 3 true
11	$\overline{\text{SDI3}}$	Data Input 3 complement
12	V _{CC}	Positive power supply input
13	V _{EE}	Negative power supply input
14	V _{CC}	Positive power supply input
15	BYPASS/AUTO BYPASS	Bypass / Auto Bypass mode select
16	OUTPUT MUTE	Data and Clock Output Mute input (active low)
17	V _{EE}	Negative power supply input
18	XTAL IN/EXT CLK	Crystal or External Oscillator input
19	V _{EE}	Negative power supply input
20	V _{EE}	Negative power supply input
21	V _{EE}	Negative power supply input
22	XTAL OUT	Crystal Oscillator output
23	V _{EE}	Negative power supply input
24	LOCK DETECT	PLL Lock Detect output (active high)
25	V _{EE}	Negative power supply input
26	V _{EE}	Negative power supply input
27	V _{EE}	Negative power supply input
28	$\overline{\text{SCO/SDO2}}$	Serial Clock or Serial Data Output 2 complement
29	SCO/SDO2	Serial Clock or Serial Data Output 2 true
30	V _{CC}	Positive power supply input
31	V _{CC}	Positive power supply input
32	$\overline{\text{SDO}}$	Data Output complement
33	SDO	Data Output true
34	V _{CC}	Positive power supply input
35	V _{CC}	Positive power supply input
36	SD/HD	Data Rate Range output
37	SCO_EN	Serial Clock or Serial Data 2 Output select
38	V _{EE}	Negative power supply input
39	V _{EE}	Negative power supply input
40	V _{EE}	Negative power supply input
41	V _{EE}	Negative power supply input
42	V _{EE}	Negative power supply input
43	LF1	Loop Filter
44	LF2	Loop Filter
45	RATE 0	Data Rate select
46	RATE 1	Data Rate select
47	SEL0	Data Input select
48	SEL1	Data Input select

Absolute Maximum Ratings (Note 1) **It is anticipated that this device will not be offered in a military qualified version.** If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V_{CC}-V_{EE}$)	4.0V
Logic Supply Voltage (V_i)	$V_{EE}-0.15V$ to $V_{CC}+0.15V$
Logic Input Current (single input):	
$V_i = V_{EE}-0.15V$	-5 mA
$V_i = V_{CC}+0.15V$	+5 mA
Logic Output Voltage (V_o)	$V_{EE}-0.15V$ to $V_{CC}+0.15V$
Logic Output Source/Sink Current	± 8 mA
Serial Data Input Voltage (V_{SDI})	V_{CC} to $V_{CC}-2.0V$
Serial Data Output Sink Current (I_{SDO})	24 mA

Package Thermal Resistance

θ_{JA} 48-pin LLP 26.1°C/W

θ_{JC} 48-pin LLP 1.9°C/W

Storage Temp. Range -65°C to +150°C

Junction Temperature +150°C

Lead Temperature (Soldering 4 Sec) +260°C (Pb-free)

ESD Rating (HBM) 2 kV

ESD Rating (MM) 250V

Recommended Operating Conditions

Supply Voltage ($V_{CC}-V_{EE}$)	3.3V $\pm 5\%$
Logic Input Voltage	V_{EE} to V_{CC}
Differential Serial Input Voltage	800 mV $\pm 10\%$
Serial Data or Clock Output Sink Current (I_{SO})	16 mA max.
Operating Free Air Temperature (T_A)	-40°C to +85°C

DC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
V_{IH}	Input Voltage High Level		Logic level inputs	2		V_{CC}	V
V_{IL}	Input Voltage Low Level			V_{EE}		0.8	V
I_{IH}	Input Current High Level	$V_{IH} = V_{CC}$			1	20	μA
I_{IL}	Input Current Low Level	$V_{IL} = V_{EE}$			-1	-20	μA
V_{OH}	Output Voltage High Level	$I_{OH} = -2$ mA	All logic level outputs	2			V
V_{OL}	Output Voltage Low Level	$I_{OL} = +2$ mA				$V_{EE} + 0.6$	V
V_{SDID}	Serial Input Voltage, Differential		SDI	200		1600	mV _{P-P}
V_{CMI}	Input Common Mode Voltage		SDI	$V_{CC}-1.6$		$V_{CC}-0.2$	V
V_{SDOD}	Serial Output Voltage, Differential	100 Ω differential load	SCO, SDO	720	800	880	mV _{P-P}
V_{CMO}	Output Common Mode Voltage	100 Ω differential load	SCO, SDO		$V_{CC}-V_{SDOD}/2$		V
I_{LEAK}	Leakage Current		LF1, LF2		TBD		μA
I_{CC}	Power Supply Current, 3.3V supply, Total	270 Mbps, NTSC color bar pattern			105		mA
I_{CC}	Power Supply Current, 3.3V supply, Total	1485 Mbps, NTSC color bar pattern			105		mA

AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Note 3)

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
BR _{SD}	Serial Data Rate	SMPTE 259M, A	SDI, SDO		143		Mbps
BR _{SD}	Serial Data Rate	SMPTE 259M, C	SDI, SDO		270		Mbps
BR _{SD}	Serial Data Rate	SMPTE 292M	SDI, SDO		1483, 1485		Mbps
TOL _{JIT}	Serial Input Jitter Tolerance	143 or 270 Mbps, (Notes 7, 8, 9)	SDI	>6			UI _{P-P}
TOL _{JIT}	Serial Input Jitter Tolerance	143 or 270 Mbps, (Notes 7, 8, 10, 13)	SDI	>0.6			UI _{P-P}
TOL _{JIT}	Serial Input Jitter Tolerance	1483 Mbps or 1485 Mbps, (Notes 7, 8, 9)	SDI	>6			UI _{P-P}
TOL _{JIT}	Serial Input Jitter Tolerance	1483 Mbps or 1485 Mbps, (Notes 7, 8, 10, 13)	SDI	>0.6			UI _{P-P}
t _{JIT}	Additive Output Jitter	143 Mbps, (Note 8)	SDO		0.02	0.08	UI _{P-P}
t _{JIT}	Additive Output Jitter	270 Mbps, (Note 8)	SDO		0.02	0.08	UI _{P-P}
t _{JIT}	Additive Output Jitter	1483 Mbps, 1485 Mbps, (Note 8)	SDO		0.05	0.1	UI _{P-P}
λ _{BW}	Jitter Transfer Function –3 dB Bandwidth (Fractional Loop Bandwidth)	All supported data rates, (Note 11)		0.1	0.25	0.35	%BR _{SD}
δ	Jitter Transfer Function Peaking	All supported data rates, (Note 12)			0.05	0.1	dB
F _{CO}	Serial Clock Output Frequency	143 Mbps data rate	SCO		143		MHz
F _{CO}	Serial Clock Output Frequency	270 Mbps data rate	SCO		270		MHz
F _{CO}	Serial Clock Output Frequency	1483 Mbps data rate	SCO		1483		MHz
F _{CO}	Serial Clock Output Frequency	1485 Mbps data rate	SCO		1485		MHz
t _{JIT}	Serial Clock Output Jitter		SCO		2	3	ps _{RMS}
	Serial Clock Output Alignment with respect to Data Interval		SCO, SDO	35		65	%
	Serial Clock Output Duty Cycle		SCO	40		60	%
T _{ACQ}	Acquisition Time	Color bar pattern or PRBS 23 sequence. (Note 6)			10		ms
t _r , t _f	Input rise/fall time	10%–90%	Logic inputs		1.5	3	ns
t _r , t _f	Input rise/fall time	20%–80%, 143 or 270 Mbps	SDI	400		1500	ps
t _r , t _f	Input rise/fall time	20%–80%, 1483 or 1485 Mbps	SDI	80	120	170	ps
t _r , t _f	Output rise/fall time	10%–90%, C _L = 5 pF	Logic outputs		1.5	3	ns
t _r , t _f	Output rise/fall time	20%–80%, 1483 or 1485 Mbps, (Note 5)	SCO, SDO		90	130	ps

AC Electrical Characteristics (Continued)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Note 3)

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
F_{REF}	Reference Clock Frequency				27		MHz
F_{TOL}	Ref. Clock Freq. Tolerance	-10°C to $+60^{\circ}\text{C}$			± 50		ppm
V_{RAMP}	Power Supply Ramp Rate		V_{CC} , V_{EE}	TBD			V/ μS

Note 1: "Absolute Maximum Ratings" are those parameter values beyond which the life and operation of the device cannot be guaranteed. The stating herein of these maximums shall not be construed to imply that the device can or should be operated at or beyond these values. The table of "Electrical Characteristics" specifies acceptable device operating conditions.

Note 2: Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are referenced to V_{EE} (equal to zero volts).

Note 3: Typical values are stated for: $V_{CC} = +3.3\text{V}$, $T_A = +25^{\circ}\text{C}$.

Note 4: Spec is guaranteed by design.

Note 5: $R_L = 100\Omega$ differential.

Note 6: Measured from first SDI transition until Lock Detect (LD) output goes high (true).

Note 7: Peak-to-peak amplitude with sinusoidal modulation per SMPTE RP 184-1996 paragraph 4.1. The test data signal shall be color bars.

Note 8: This parameter is guaranteed by characterization over voltage and temperature limits.

Note 9: Refer to "A1" in Figure 1 of SMPTE RP 184-1996.

Note 10: Refer to "A2" in Figure 1 of SMPTE RP 184-1996.

Note 11: Refer to "fc" in Figure 3 of SMPTE RP 184-1996.

Note 12: Refer to "P" in Figure 3 of SMPTE RP 184-1996.

Note 13: The input jitter tolerance at frequencies higher than the B3 frequency indicated in SMPTE 259M or SMPTE 292M shall be ≥ 0.8 UI when measured using the Gennum stepped-jitter method described in Gupta, A., Tailor, B., and Francis, J., "The Deficiencies in Measuring Input Jitter Tolerance (I_{JT}) using Sine wave modulated Jitter."

Device Description

The LMH0056 HD/SD SDI Reclocker with 4:1 Input Multiplexer is used in many types of digital video signal processing equipment. Supported serial digital video standards are SMPTE 259M A & C and SMPTE 292M. Corresponding serial data rates are 143 Mbps, 270 Mbps, 1.483 Gbps and 1.485 Gbps. DVB-ASI data at 270 Mbps may also be retimed. The LMH0056 retimes the serial data stream to suppress accumulated jitter. It provides two low-jitter, differential, serial data outputs. The second output may be selected to output either serial data or a low-jitter serial data-rate clock. Controls and indicators are: serial data-rate clock or second serial data output select, manual rate select input, SD/HD rate output, lock detect output, auto/manual data bypass and output mute.

Serial data inputs are CML and LVPECL compatible. Serial data and data-rate clock outputs are differential CML and produce LVPECL compatible levels. The output buffer design can drive AC or DC-coupled, terminated 100Ω differential loads. The differential output level is 800 mV_{P-P} ±10% into 100Ω AC or DC-coupled differential loads. Logic inputs and outputs are LVCMOS compatible.

The device package is a 48-pin LLP with an exposed die attach pad. The exposed die attach pad is electrically connected to device ground (V_{EE}) and is the negative electrical terminal for the device. This terminal must be connected to the negative power supply or circuit ground.

Serial Data Inputs, Serial Data and Clock Outputs

SERIAL DATA INPUT AND OUTPUTS

The differential serial data inputs, SDI0-SDI3, accept serial digital video data at the rates specified in *Table 1*. The serial data input is differential LVPECL compatible. These inputs are intended to be DC interfaced to devices such as the LMH0034 adaptive cable equalizer. These inputs are not internally terminated or biased. The inputs may be AC-coupled if a suitable input bias voltage is provided.

The LMH0056 provides four independent, multiplexed data inputs. The active input channel is selected via the SEL0 and SEL1 pins, as shown in *Table 2*.

The LMH0056 has two, retimed, differential, serial data outputs, SDO and SCO/SDO2. These outputs provide low jitter, differential, retimed data to devices such as the LMH0002 cable driver or the LMH0031 deserializer. Output SCO/SDO2 is multiplexed and can provide either a second serial data output or a serial data-rate clock output.

The SCO_EN input controls the operating mode for the SCO/SDO2 output. When the SCO_EN input is high the SCO/SDO2 output provides a serial data-rate clock. When SCO_EN is low, the SCO/SDO2 output provides retimed serial data.

Both differential serial data outputs, SDO and SCO/SDO2, are muted when the MUTE input is a logic low level. SCO/SDO2 also mutes when the Bypass mode is activated when this output is operating as the serial clock output. When muted, SDO and SDO (or SDO2 and SDO2) will assume opposite differential output levels. The CML serial data out-

puts are differential LVPECL compatible. These outputs have internal 50Ω pull-ups and are suitable for driving AC or DC-coupled, 100Ω center-tapped, AC grounded or 100Ω un-center-tapped, differentially terminated networks.

OPERATING SERIAL DATA RATES

This device operates at serial data rates of 143 Mbps, 270 Mbps, 1483 Mbps and 1485 Mbps. The device does not lock to harmonics of these rates. The device does not lock and automatically enters the reclocker bypass mode for the following data rates: 177 Mbps, 360 Mbps, and 540 Mbps.

SERIAL DATA CLOCK/SERIAL DATA 2 OUTPUT

The Serial Data Clock/Serial Data 2 Output is controlled by the SCO_EN input and provides either a second retimed serial data output or a low jitter differential clock output appropriate to the serial data rate being processed. When operating as a serial clock output, the rising edge of the clock will be positioned within the corresponding serial data bit interval within 15% of the center of the data interval.

Differential output SCO/SDO2 functions as the second serial data output when the SCO_EN input is a logic-low level. This output functions as the serial data-rate clock output when the SCO_EN input is a logic-high level. The SCO_EN input has an internal pull-down device and the default state of SCO_EN is low (serial data output 2 enabled). SCO/SDO2 is muted when the MUTE input is a logic low level. When the Bypass mode is activated and this output is functioning as a serial clock output, the output will also be muted.

Control Inputs and Indicator Outputs

SERIAL DATA RATE SELECTOR

The Serial Data Rate Selector (RATE [1:0]) permits the user to fix the operating serial data rate. The pins have internal pull-downs which maintain a logic-low input condition unless externally driven to a logic-high condition. This input also serves to place the device in a test mode. The codes shown in *Table 1* select the desired operating serial data rate. The LMH0056 then enters either the Auto-Rate Detect mode, a single operating rate, or the test mode. Selecting the 270 Mbps rate mode may also be used when reclocking DVB-ASI data. DVB-ASI data is MPEG2 coded data that is transmitted in 8B10B coding. The device should reclock this data without harmonic locking.

TABLE 1. Data Rate Select Input Codes

RATE [1:0] Code	Data Rate or Mode	Comments
00	Auto-Rate Detect mode	143 Mbps rate operation supported only in ARD mode
01	270 Mbps	May be used to support DVB-ASI operation
10	1483/1485 Mbps	

Control Inputs and Indicator Outputs (Continued)

SERIAL DATA INPUT SELECTOR

The Serial Data Input Selector (SEL [1:0]) allows the user to select the active input channel. *Table 2* shows the input selected for a given state of SEL [1:0].

TABLE 2. Data Input Select Codes

SEL [1:0] Code	Selected Input
00	SDI0
01	SDI1
10	SDI2
11	SDI3

LOCK DETECT

The Lock Detect (LD) output, when high, indicates that data is being received and the PLL is locked. LD may be connected to the $\overline{\text{MUTE}}$ input to mute the data and clock outputs when no data signal is being received. See *Table 3*.

$\overline{\text{MUTE}}$

The $\overline{\text{MUTE}}$ input, when low, mutes the serial data and clock outputs. It may be connected to Lock Detect or externally driven to mute or un-mute the outputs. If $\overline{\text{MUTE}}$ is connected to LD, then the data and clock outputs are muted when the PLL is not locked. This function overrides the Bypass function: see *Table 3*. $\overline{\text{MUTE}}$ has an internal pull-up device to enable the output by default.

BYPASS/AUTO BYPASS

The Bypass/Auto Bypass input, when high, forces the device to output the data without reclocking it. When this input is low, the device automatically bypasses the reclocking function when the device is in an unlocked condition or the detected data rate is a rate which the device does not support. See *Table 3*. BYPASS/AUTO BYPASS has an internal pull-down device.

TABLE 3. Control Functionality

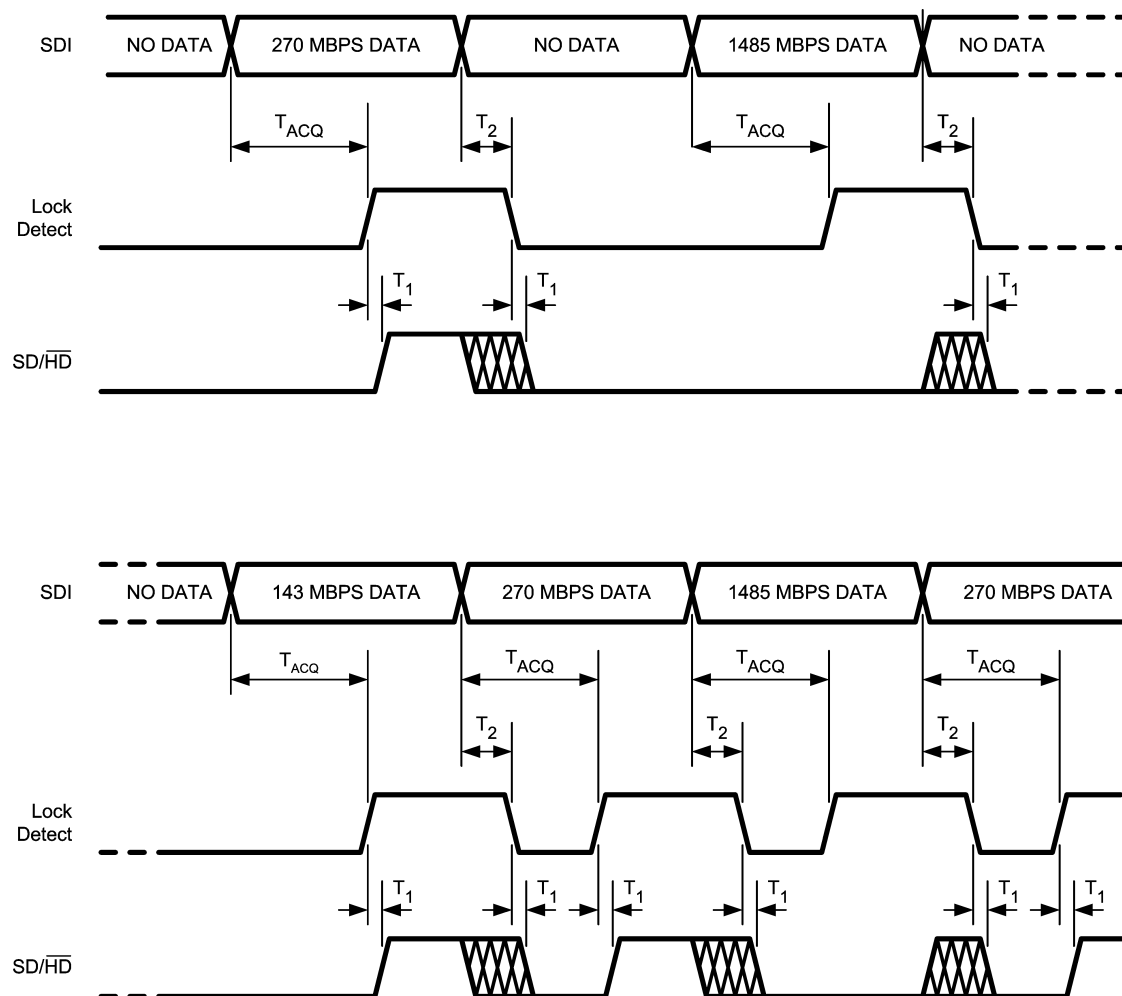
LOCK DETECT	OUTPUT $\overline{\text{MUTE}}$	BYPASS/AUTO BYPASS	DEVICE STATUS
0	1	0	PLL unlocked, reclocker bypassed
1	1	0	PLL locked to supported data rate, reclocker not bypassed
X	0	X	Outputs muted
0	LOCK DETECT	X	Outputs muted
1	LOCK DETECT	0	PLL locked to supported data rate, reclocker not bypassed
1	LOCK DETECT	1	PLL locked to supported data rate, reclocker bypassed
X	1	1	Outputs not muted, reclocker bypassed

Control Inputs and Indicator Outputs (Continued)

SD/ $\overline{\text{HD}}$

The SD/ $\overline{\text{HD}}$ output indicates whether the LMH0056 is processing SD or HD data rates. It may be used to control another device such as the LMH0002 cable driver. When this output is high it indicates that the data rate is 270 Mbps (or 143 Mbps). When low, the indicated data rate is 1485 or

1485 Mbps. The SD/ $\overline{\text{HD}}$ output is a registered function and is only valid when the PLL is locked and the Lock Detect output is high. The SD/ $\overline{\text{HD}}$ is undefined for a short time after lock detect assertion or de-assertion caused by a data rate change on the SDI input. See Figure 1 for a timing diagram showing the relationship between SDI, Lock Detect, and SD/ $\overline{\text{HD}}$. When the PLL is not locked (the Lock Detect output is low), the SD/ $\overline{\text{HD}}$ output defaults to HD (low).



T_{ACQ} = Acquisition Time, defined in the AC Electrical Characteristics Table

T_1 = Time from Lock Detect assertion or deassertion until SD/ $\overline{\text{HD}}$ output is valid, typically 37 ns (one 27 MHz clock period)

T_2 = Time from SDI input change until Lock Detect de-assertion, 1 ms maximum. SD/ $\overline{\text{HD}}$ output is not valid during this time.

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FIGURE 1. SDI, Lock Detect, and SD/ $\overline{\text{HD}}$

Control Inputs and Indicator Outputs (Continued)

SCO_EN

Input SCO_EN enables the SCO/SDO2 differential output to function either as a serial data-rate clock or second serial data output. SCO/SDO2 functions as a serial data-rate clock when SCO_EN is high. This pin has an internal pull-down device. The default state (low) enables the SCO/SDO2 output as a second serial data output.

CRYSTAL OR EXTERNAL CLOCK REFERENCE

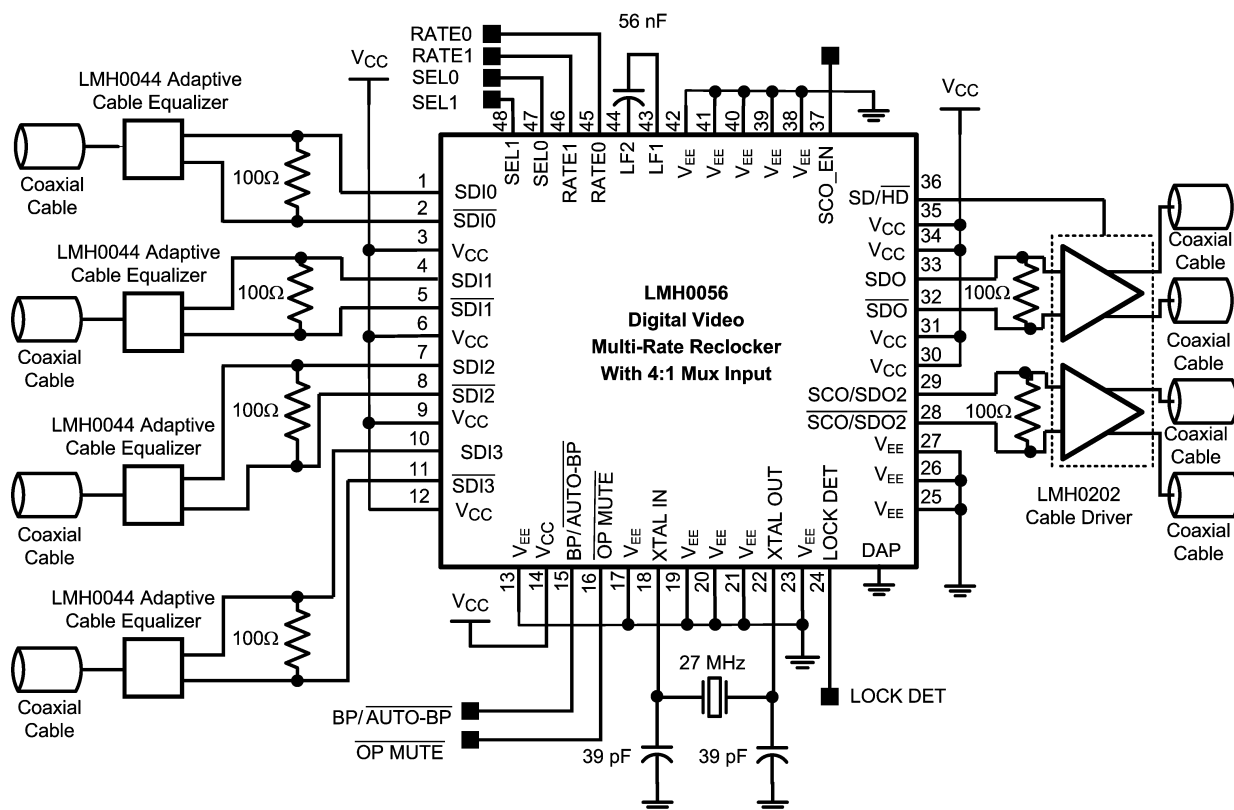
The LMH0056 uses a 27 MHz crystal or external clock signal as a timing reference input. A 27 MHz parallel resonant crystal and load network may be connected to the XTAL IN/EXT CLK and XTAL OUT pins. Alternatively, a 27 MHz LVCMOS compatible clock signal may be input to XTAL IN/EXT CLK. Parameters for a suitable crystal are given in *Table 4*.

TABLE 4. Crystal Parameters

Parameter	Value
Frequency	27 MHz
Frequency Stability	±100 ppm @ recommended drive level
Operating Mode	Fundamental mode, Parallel Resonant
Load Capacitance	20 pF
Shunt Capacitance	7 pF
Series Resistance	40Ω max.
Recommended Drive Level	100 μW
Maximum Drive Level	500 μW
Operating Temperature Range	–10°C to +60°C

Application Information

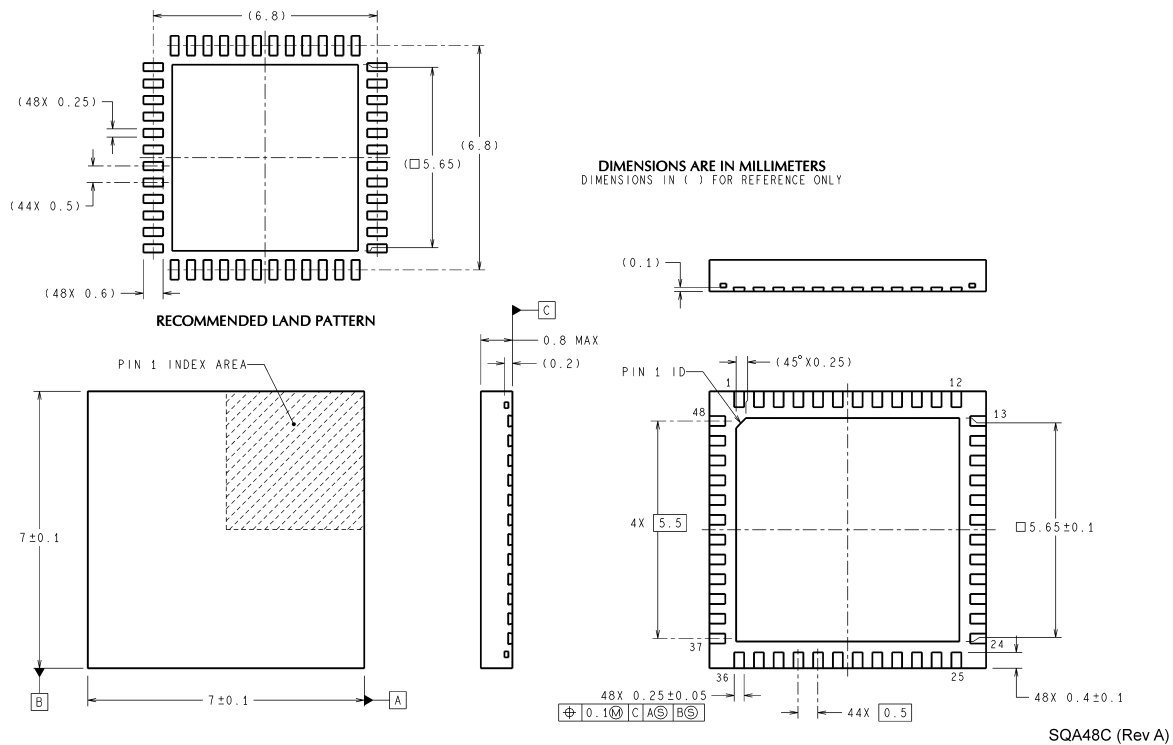
Figure 2 shows an application circuit for the LMH0056 along with the LMH0044 SMPTE 292M / 259M Adaptive Cable Equalizers and LMH0202 SMPTE 292M / 259M Dual Cable Driver.



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FIGURE 2. Application Circuit

Physical Dimensions inches (millimeters) unless otherwise noted



48-Pin LLP
Order Number LMH0056SQ
NS Package Number SQA-48C

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