National Semiconductor

August 1996

LM1212
230 MHz Video Amplifier System with OSD Blanking

General Description

The LM1212 is a very high frequency video amplifier system intended for use in high resolution monochrome or RGB color monitor applications with OSD. In addition to the wideband video amplifier the LM1212 contains a gated differential input black level clamp comparator for brightness control, a DC controlled attenuator for contrast control and a DC controlled sub contrast attenuator for drive control. The DC control for the contrast attenuator is pinned out separately to provide a more accurate control system for RGB color monitor applications. All DC controls offer a high input impedance and operate over a 0V–4V range for easy interface to bus controlled alignment systems. During the OSD window, the output is blanked to < 0.4V. The LM1212 operates from a nominal 12V supply but can be operated with supply voltages down to 8V for applications that require reduced IC package power dissipation characteristics.

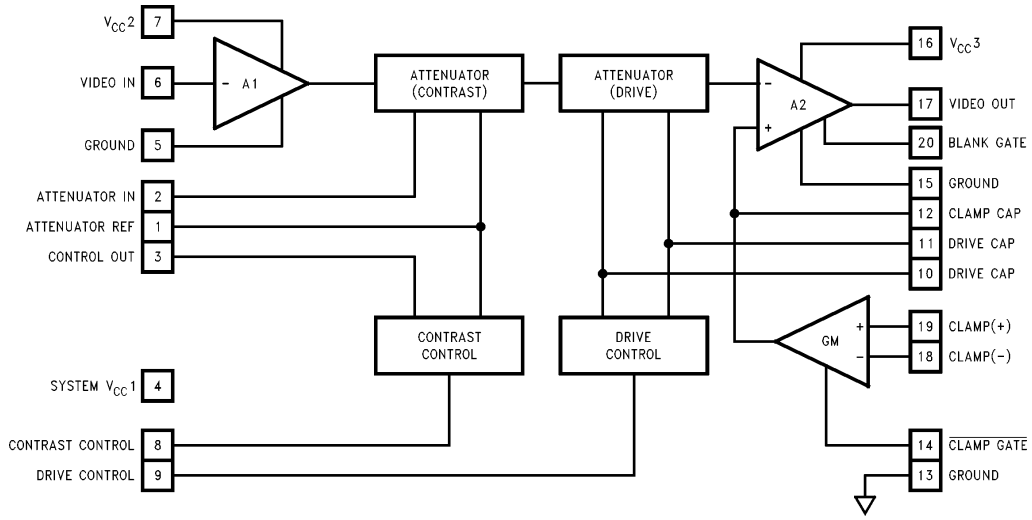
Features

- Wideband video amplifier
  ($f_{-3\,dB}$ = 230 MHz at V_O = 4 V_{PP})
- t_r, t_f = 1.5 ns at V_O = 4 V_{PP}
- Externally gated comparator for brightness control
- 0V to 4V high input impedance DC contrast control (> 40 dB range)
- 0V to 4V high input impedance DC drive control (±3 dB range)
- Ouput blanked to < 0.4V for OSD window
- Easy to parallel three LM1212s for optimum color tracking in RGB systems
- Output stage clamps to 0.65V and provides up to 9V output voltage swing
- Output stage directly drives most hybrid or discrete CRT amplifier stages

Applications

- High resolution CRT monitors with OSD
- Video switches
- Video AGC amplifier
- Wideband amplifier with gain and DC offset control

Block and Connection Diagram



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Order Number LM1212N
See NS Package Number N20A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC} Pins 4, 7, 16 to Ground Pins 5, 13, 15	15V
Voltage at Any Input Pin (V_{IN})	$V_{CC} \geq V_{IN} \geq$ GND
Video Output Current (I_{17})	28 mA
Package Power Dissipation at $T_A = 25°C$ (Above 25°C Derate Based θ_{JA} and T_J)	1.56W
Package Thermal Resistance (θ_{JA}) N20A	68°C/W
Junction Temperature (T_J)	150°C
Storage Temperature Range (T_{stg})	−65°C to +150°C
Lead Temperature N Package (Soldering, 10 sec.)	265°C
ESD Susceptibility Human Body Model: 100 pF Discharged through a 1.5k Resistor	2 kV

Operating Ratings (Note 2)

Temperature Range	−20°C to +80°C
Supply Voltage (V_{CC})	$8V \leq V_{CC} \leq 13.2V$

DC Electrical Characteristics

See Test Circuit *(Figure 1)*, $T_A = 25°C$, V4 = V7 = V16 = 12V, S1 Open, V19 = 4V, V8 = 4V, V9 = 4V, V14 = 0V unless otherwise noted.

Symbol	Parameter	Conditions	Typical (Note 3)	Limit (Note 4)	Units
I_S 4, 7, 16	Total Supply Current	$R_{Load} = \infty$ (Note 5)	51	80	mA (max)
V_6	Video Input Bias Voltage		2.9	2	V (min)
V_{14L}	Clamp Gate Low Input Voltage	Clamp Comparator On		0.8	V (max)
V_{14H}	Clamp Gate High Input Voltage	Clamp Comparator Off		2	V (min)
I_{14L}	Clamp Gate Low Input Current	$V_{14} = 0V$	−0.5		μA
I_{14H}	Clamp Gate High Input Current	$V_{14} = 12V$	0.005		μA
I_{12+}	Clamp Cap Charge Current		800	500	μA (min)
I_{12-}	Clamp Cap Discharge Current		−800	−500	μA (min)
V_{17L}	Video Output Low Voltage		0.2	0.65	V (max)
V_{17H}	Video Output High Voltage		10	9	V (min)
V_{OS}	Comparator Input Offset Voltage	$V_{18} - V_{19}$	30	±75	mV (max)
V_{20L}	Blank Gate Low Input Voltage	Blank Gate Off	1.2	0.8	V (max)
V_{20H}	Blank Gate High Input Voltage	Blank Gate On	2.6	3	V (min)
I_{20L}	Blank Gate Low Input Current	$V_{20} = 0.8V$	0.01	1	μA (max)
I_{20H}	Blank Gate High Input Current	$V_{20} = 3V$	33	200	μA (max)
V_{17}(blanked)	Blanked Output Voltage	$V_{20} = 3V$	0.3	0.8	V (max)

AC Electrical Characteristics

See Test Circuit *(Figure 1)*, $T_A = 25°C$, V4 = V7 = V16 = 12V, S1 Closed, V19 = 4V, V8 = 4V, V9 = 4V, V14 = 0V unless otherwise noted.

Symbol	Parameter	Conditions	Typical (Note 3)	Limit (Note 4)	Units
R_{IN}	Video Amplifier Input Resistance	$f_{IN} = 12$ kHz	20		kΩ
A_V max	Video Amplifier Gain	$V_8 = 4V$, $V_9 = 4V$	20	14	V/V (min)
ΔA_V 2V	Attenuation at 2V	Ref: A_V max, $V_8 = 2V$	−6		dB
ΔA_V 0.5V	Attenuation at 0.5V	Ref: A_V max, $V_8 = 0.5V$	−38	−20	dB (min)
Δ Drive	Δ Gain Range	$V_9 = 0V$ to 4V	6	4.5	dB (min)
THD	Video Amplifier Distortion	$V_O = 4\ V_{PP}$, $f_{IN} = 12$ kHz	0.5		%
$f_{-3\ dB}$	Video Amplifier Bandwidth (Note 6)	$V_O = 4\ V_{PP}$	230		MHz
t_r	Output Rise Time (Note 6)	$V_O = 4\ V_{PP}$	1.5		ns
t_f	Output Fall Time (Note 6)	$V_O = 4\ V_{PP}$	1.5		ns

Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional but do not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: Typical specifications are specified at $+25°C$ and represent the most likely parametric norm.

Note 4: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 5: The supply current specified is the quiescent current for V_{CC1}, V_{CC2} and V_{CC3} with $R_{Load} = \infty$, see *Figure 1's* test circuit. The total supply current also depends on the output load, R_{Load}. The increase in device power dissipation due to R_{Load} must be taken into account when operating the device at the maximum ambient temperature.

Note 6: When measuring video amplifier bandwidth or pulse rise and fall times, a double sided full ground plane printed circuit board is recommended. The measured rise and fall times are effective rise and fall times, taking into account the rise and fall times of the generator and the oscilloscope.

Test Circuit

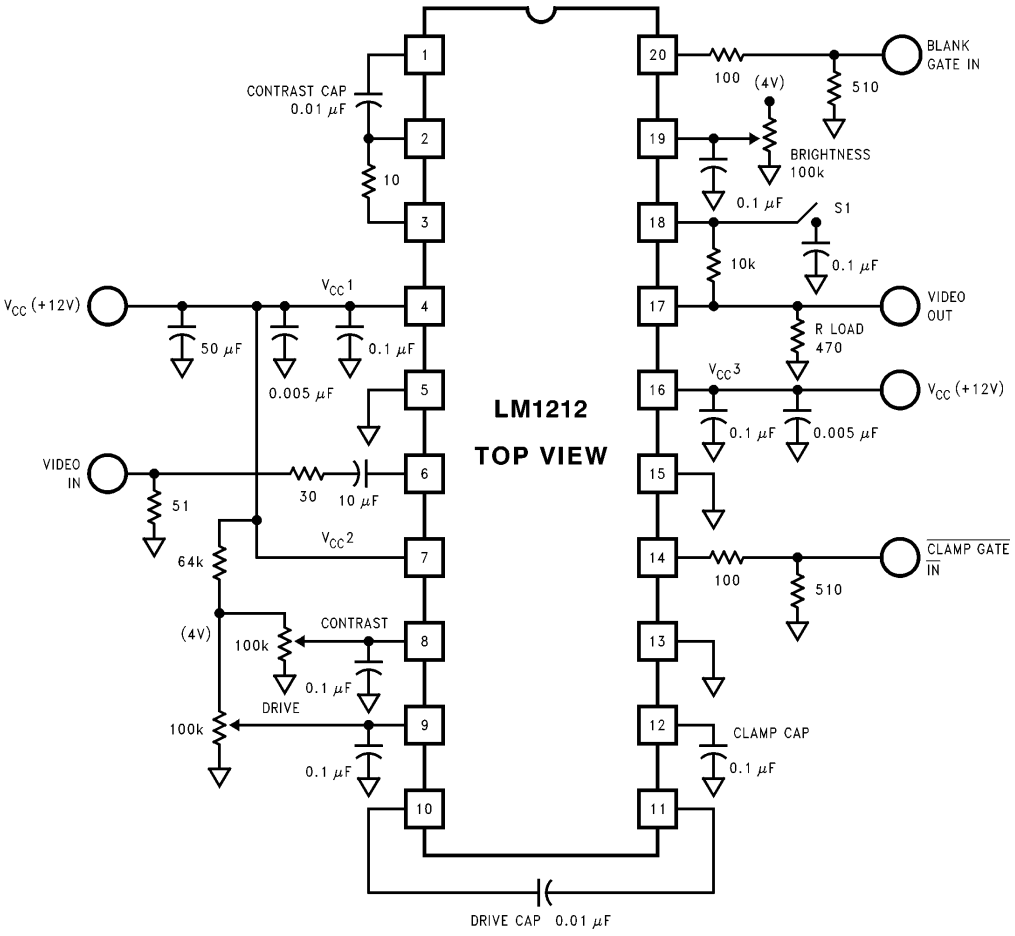

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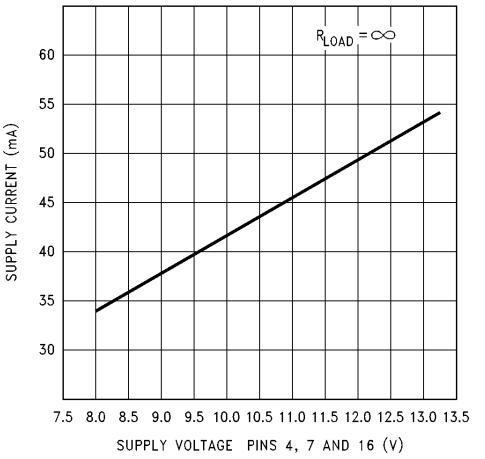
FIGURE 1. LM1212 Test Circuit

Typical Performance Characteristics (V_{CC} = 12V, T_A = 25°C unless otherwise specified)

Quiescent Supply Current vs Supply Voltage



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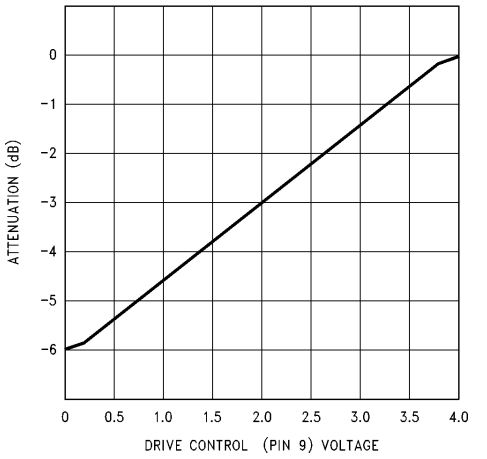
Attenuation vs Drive Control Voltage



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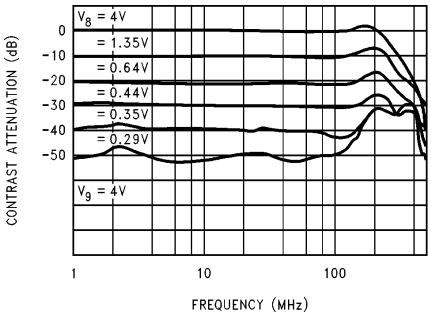
Contrast vs Frequency



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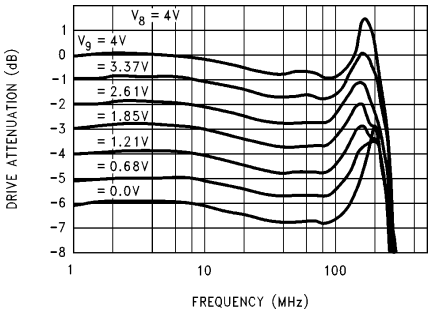
Drive vs Frequency



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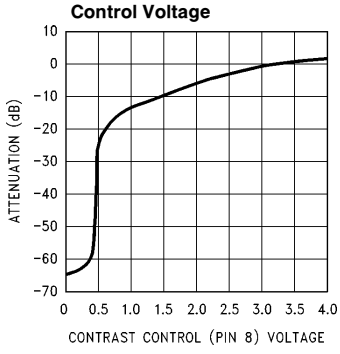
Attenuation vs Contrast Control Voltage



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Circuit Description

Figure 2 shows a block diagram of the LM1212 video amplifier along with contrast and brightness (black level) control. Contrast control is a DC-operated attenuator which varies the AC gain of the amplifier. Signal attenuation (contrast) is achieved by varying the base drive to a differential pair and thereby unbalancing the current through the differential pair. As shown in *Figure 2*, a 5.3V bias voltage is internally connected to the positive input of the attenuator and to Pin 1. Pin 3 provides a control voltage for the negative input (pin 2) of the attenuator. The voltage at pin 3 varies as the voltage at the contrast control input (pin 8) varies thus providing signal attenuation. The gain is maximum (0 dB attenuation) if the voltage at pin 8 is 4V and is minimum (maximum attenuation) if the voltage at pin 8 is 0V. The 0V to 4V DC-operated drive control at pin 9 provides a 6 dB gain adjustment range. This feature is necessary for RGB applications where independent gain adjustment of each channel is required.

The brightness or black level clamping requires a ''sample and hold'' circuit which holds the DC bias of the video amplifier constant during the black level reference portion of the video waveform. Black level clamping, often referred to as DC restoration, is accomplished by applying a back porch clamp signal to the clamp gate input pin (pin 14). The clamp comparator is enabled when the clamp signal goes low during the black level reference period (see *Figure 2*). When the clamp comparator is enabled, the clamp capacitor connected to pin 12 is either charged or discharged until the voltage at the minus input of the comparator matches the voltage set at the plus input of the comparator. During the video portion of the signal, the clamp comparator is disabled and the clamp capacitor holds the proper DC bias. In a DC coupled cathode drive application, picture brightness function can be achieved by varying the voltage at the comparator's plus input. Note that the back porch clamp pulse width (t_W in *Figure 2*) must be greater than 100 ns for proper operation.

OSD blanking is activated through an active high TTL signal at pin 20. When pin 20 has a high logic level the video output at pin 17 drops to $<$ 100 mV. During this time an external signal can be applied to the output, driving the video level to the desired level for the OSD window. This OSD signal will back bias the emitter of the internal output transistor, Q23 (see *Figure 4*). The maximum voltage to this transistor under this condition is 5V. This signal must also supply enough current to the pull-down transistor, Q24, which is about 100 mA. The OSD blanking can only be done during the active video period. If activated during the clamp pulse period, the OSD blanking will interfere with the DC restoration.

VIDEO AMPLIFIER SECTION (Input Stage)

A simplified schematic of LM1212's video amplifier input stage is shown in *Figure 3* . The 5.4V zener diode, Q1, Q6 and R2 bias the base of Q7 at 2.6V. The AC coupled video signal applied to pin 6 is referenced to the 2.6V bias voltage.

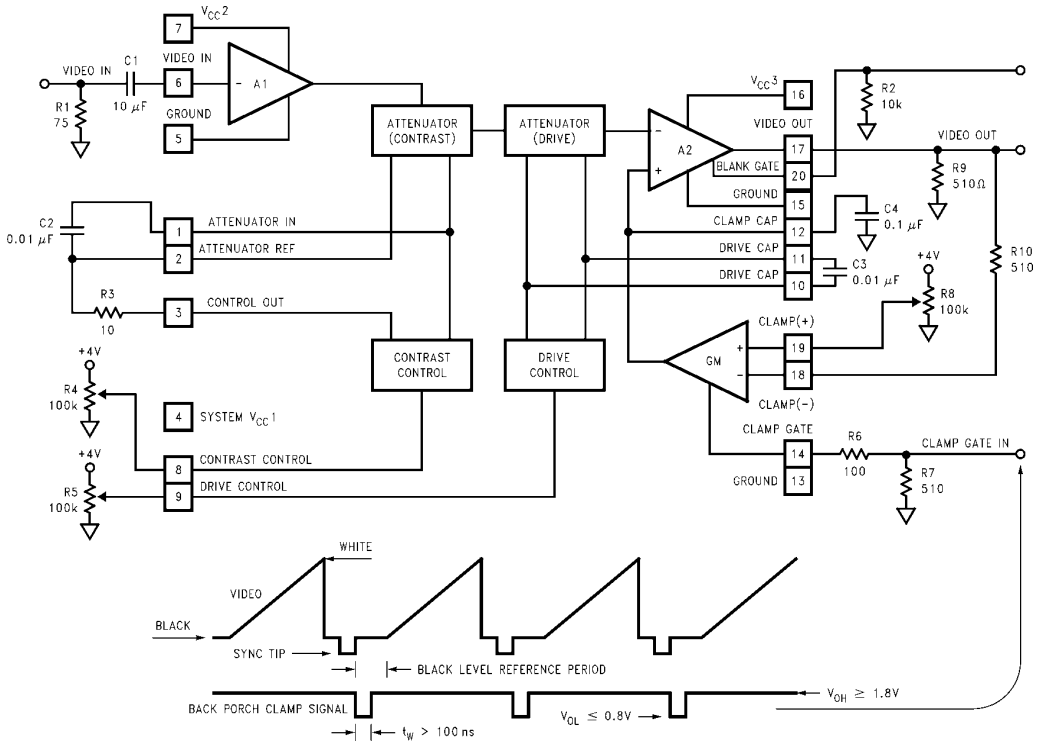

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FIGURE 2. Block Diagram of the LM1212 Video Amplifier with Contrast and Brightness (Black Level) Control

Circuit Description (Continued)

Transistor Q7 buffers the video signal, V_{IN}, and Q8 converts the voltage to current. The AC collector current through Q8 is $I_{C8} = V_{IN}/R9$. Under maximum gain condition, transistors Q9 and Q11 are off and all of I_{C8} flows through the load resistors R10 and R11. The maximum signal gain at the base of Q13 is, $A_{V1} = -(R10 + R11)/R9 = -2$. Signal attenuation is achieved by varying the base drive to the differential pairs Q9, Q10 and Q11, Q12 thereby unbalancing the collector currents through the transistor pairs. Base of Q10 is biased at 5.3V by its connection to the emitter of Q41 (see *Figure 5*). Pin 2 is connected to pin 3 through a 10Ω resistor. Adjusting the contrast voltage at pin 8 produces a control voltage at pin 3 which drives the base of Q9. By varying the voltage at the base of Q9, Q8's collector current (I_{C8}) is diverted away from the load resistors R10 and R11, thereby providing signal attenuation. Maximum attenuation is achieved when all of I_{C8} flows through Q9 and no current flows through the load resistors.

The differential pair Q11 and Q12 provide drive control. Q12's base is internally biased at 7.3V. Adjusting the voltage at the drive control input (pin 9) produces a control voltage at the base of Q11. With Q9 off and Q12 off, all of I_{C8} flows through R10, thus providing a gain of $A_{V1} = -(R10/R9) \times V_{IN} = -1$. Drive control thus provides a 6 dB attenuation range.

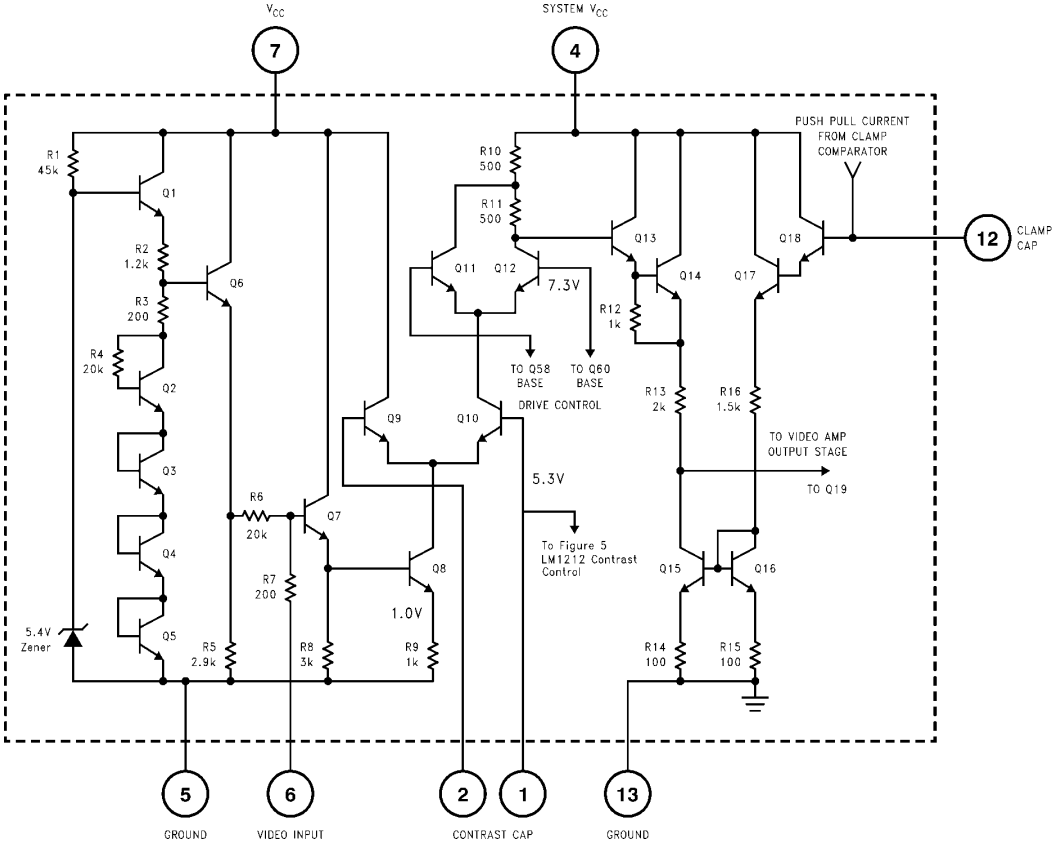

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FIGURE 3. Simplified Schematic of the LM1212 Video Amplifier Input Stage

Circuit Description (Continued)

VIDEO AMPLIFIER SECTION (Output Stage)

A simplified schematic of LM1212's video amplifier output stage is shown in *Figure 4*. The output stage is the second gain stage. Ideally the gain of the second gain stage would be $A_{V2} = -R21/R18 = -16$. Because of the output stage's low open loop gain, the gain is approximately $A_{V2} = -10$. Thus the maximum gain of the video amplifier is $A_V = A_{V1} \times A_{V2} = 20$. Transistors Q23 and Q24 provide a push-pull drive to the load. The output voltage can swing from 0.2V to 10V.

Q82 is the OSD blanking transistor. Its base is connected to pin 20 via R34. A high TTL signal at pin 20 turns on Q82. This forces a current flow-through R20 and R31. These two resistors form a voltage divider from the emitter of Q82. If the input at pin 20 ia a minimum TTL high of 2.0V, then the juction of R20 and R31 will have a voltage of 0.6V. This voltage is applied to the bases of Q22 and Q24. 0.6V is just enough voltage to drive transistors Q22 and Q24 into saturation, forcing the output voltage at pin 17 to drop below 100 mV. The OSD video signal is applied during this period. The emitter-base junction of Q82 can withstand a maximum reverse bias voltage of 5V, thus pin 17 must not be driven above 5V during OSD blanking.

CONTRAST CONTROL SECTION

A simplified schematic of LM1212's contrast control section is shown in *Figure 5*. A 0V to 4V DC voltage is applied at the contrast input (pin 8). Transistors Q29, Q30 and Q34 buffer and level shift the contrast voltage to the base of Q36. The voltage at the emitter of Q36 equals the contrast voltage (V_{cont}) and the current through Q36's collector is given by $I_{C36} = V_{cont}/R28$.

Transistor Q36's collector current is used to unbalance the current through the differential pair comprised of Q38 and Q40. Q40's base is internally biased at 5.3V. The 5.3V reference is also connected to pin 1 and to the base of Q10 (see *Figure 3*). The base of Q38 (pin 3) is externally connected to pin 2 through a 10Ω resistor (see *Figures 2* and *3*). With $V_{cont} = 2V$, the differential pair (Q38, Q40) is balanced and the voltage at pins 1 and 2 is 5.3V. Under this condition, Q8's collector current is equally split between Q9 and Q10 (see *Figure 3*) and the amplifier's gain is half the maximum gain. If contrast voltage at pin 8 is greater than 2V then Q36's collector current increases, thus pulling Q38's collector node lower and consequently moving Q38's base below 5.3V. With pin 2 at a lower voltage than pin 1, current through Q10 (see *Figure 3*) increases and the amplifier's gain increases. With $V_{cont} = 4V$, the amplifier's gain is maximum.

If the contrast voltage at pin 8 is less than 2V then Q36's collector current decreases and Q38's base is pulled above 5.3V. With pin 2 voltage greater than pin 1 voltage, less current flows through Q10 (see *Figure 3*), consequently the amplifier's gain decreases. With $V_{cont} = 0V$, the amplifier's gain is minimum (i.e., maximum attenuation).

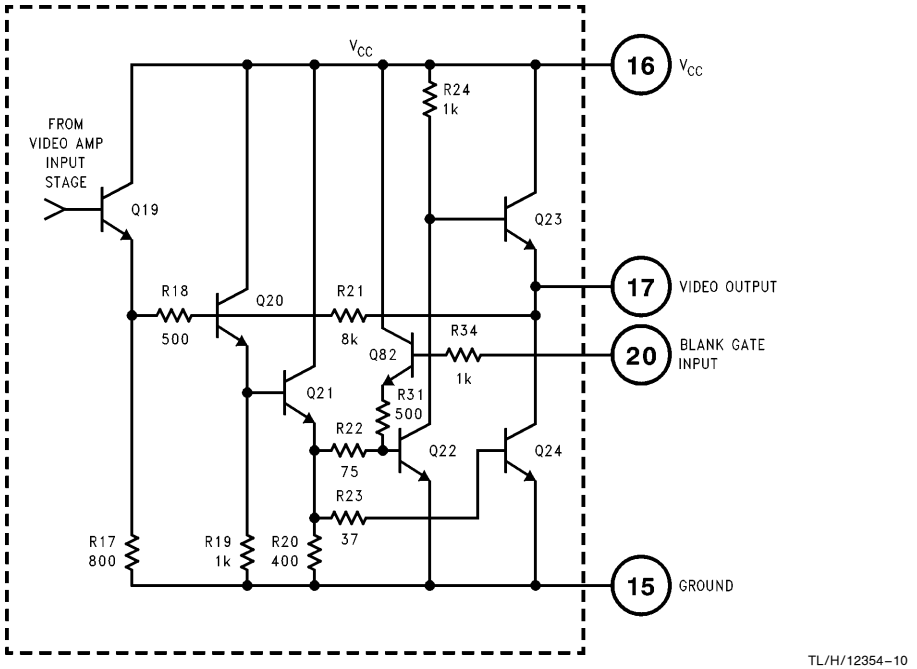

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FIGURE 4. Simplified Schematic of LM1212 Video Amplifier Output Stage

Circuit Description (Continued)

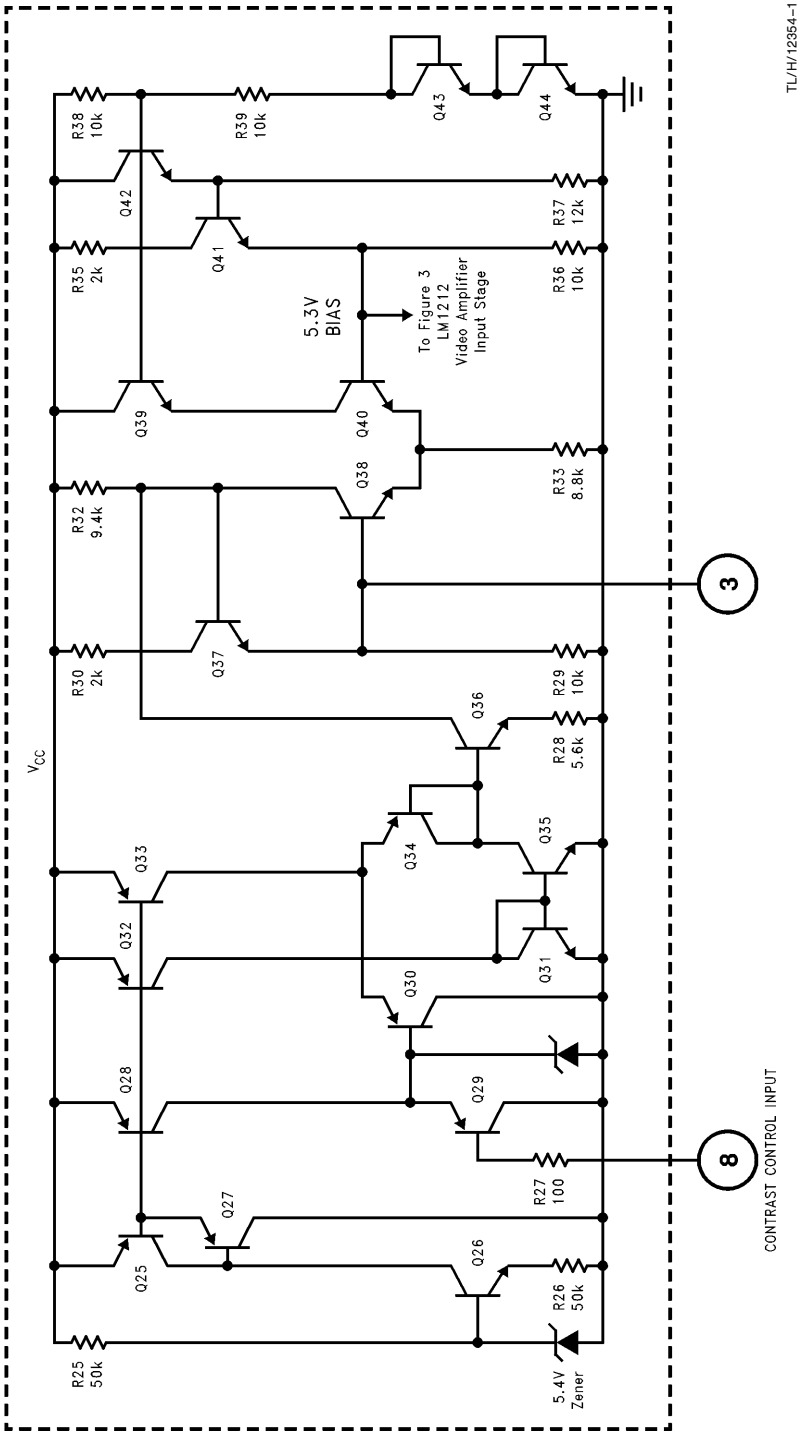

FIGURE 5. Simplified Schematic of LM1212 Contrast Control

Circuit Description (Continued)

DRIVE CONTROL SECTION

A simplified schematic of the LM1212's drive control section is shown in *Figure 6* . A 0V to 4V DC voltage is applied at the drive control input (pin 9). Transistors Q49, Q50 and Q54 buffer and level shift the contrast voltage to the base of Q56. The voltage at the emitter of Q56 equals the drive voltage, V_{drive} and the current through Q56's collector is given by $I_{C56} = V_{drive}/R43$.

Transistor Q56's collector current is used to unbalance the current through the differential pair comprised of Q58 and Q60. Q60's base is internally biased at 7.1V and connected to the base of Q12 (see *Figure 3*). Q58's base is internally connected to the base of Q11 (see *Figure 3*). With $V_{cont} =$ 2V, the differential pair (Q58, Q60) is balanced and the voltage at the bases of Q11 and Q12 is 7.1V. Under this condition, Q10's collector current is equally split between Q11 and Q12 (see *Figure 3*). If the drive voltage at pin 9 is greater than 2V then Q56's collector current increases, thus pulling Q58's collector node lower and consequently moving Q58's base below 7.1V. With base of Q11 below 7.1V, current through Q12 (see *Figure 3*) increases and the amplifier's gain increases. With $V_{drive} =$ 4V, the amplifier's gain is maximum under maximum contrast condition (i.e., $V_{cont} =$ 4V).

If the drive voltage at pin 8 is less than 2V then Q56's collector current decreases and Q58's base is pulled above 7.1V. With base of Q11 greater than 7.1V, less current flows through Q12 (see *Figure 3*), consequently the amplifier's gain decreases. With $V_{drive} =$ 0V, the amplifier's gain is 6 dB less than the maximum gain.

CLAMP GATE AND CLAMP COMPARATOR SECTION

Figures 7 and *8* show simplified schematics of the clamp gate and clamp comparator circuits. The clamp gate circuit *(Figure 7)* consists of a PNP input buffer transistor (Q82), a PNP emitter coupled pair (Q85 and Q86) referenced on one side to 2.1V and an output switch transistor Q89. When the clamp gate input at pin 14 is high ($>$ 1.5V) the Q89 switch is on and shunts the 200 μA current from current source Q90 to ground. When pin 14 is low ($<$ 1.3V) the Q89 switch is off and the 200 μA current is mirrored by the current mirror comprised of Q91 and Q75 (see *Figure 8*). Consequently the clamp comparator comprised of the differential pair Q74 and Q77 is enabled. The input of the clamp comparator is similar to the clamp gate except that an NPN emitter coupled pair is used to control the current that will charge or discharge the clamp capacitor externally connected from pin 12 to ground. PNP transistors are used at the inputs because they offer a number of advantages over NPNs. PNPs will operate with base voltages at or near ground and will usually have a greater emitter base breakdown voltage (BVebo). Because the differential input voltage to the clamp comparator during the video scan period could be greater than the BVebo of NPN transistors, a resistor (R63) with a value one half that of R60 or R68 is connected between the bases of Q71 and Q79. The clamp comparator's common mode range is from ground to approximately 9V and the maximum differential input voltage is V_{CC}.

Circuit Description (Continued)

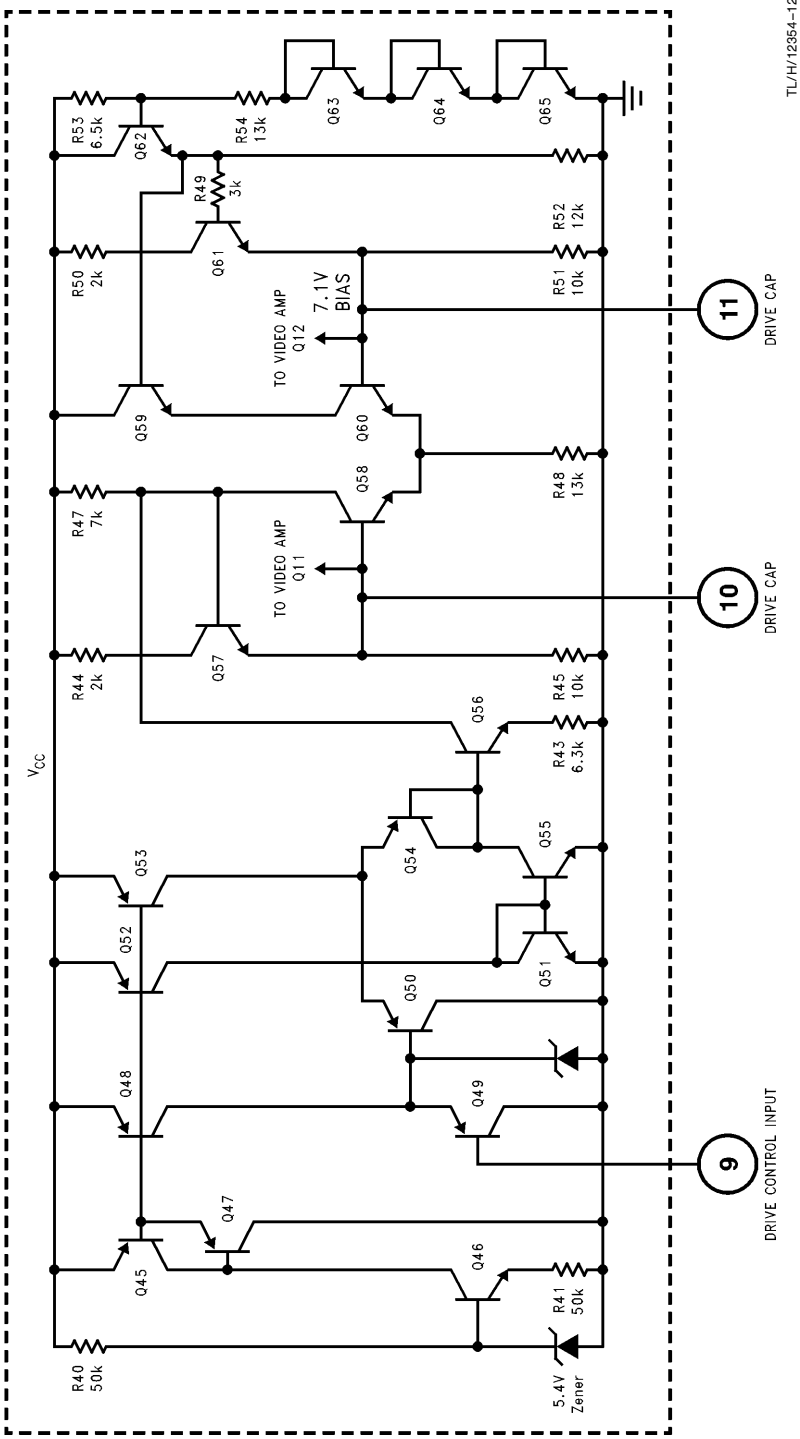

FIGURE 6. Simplified Schematic of the LM1212 Drive Control

Circuit Description (Continued)

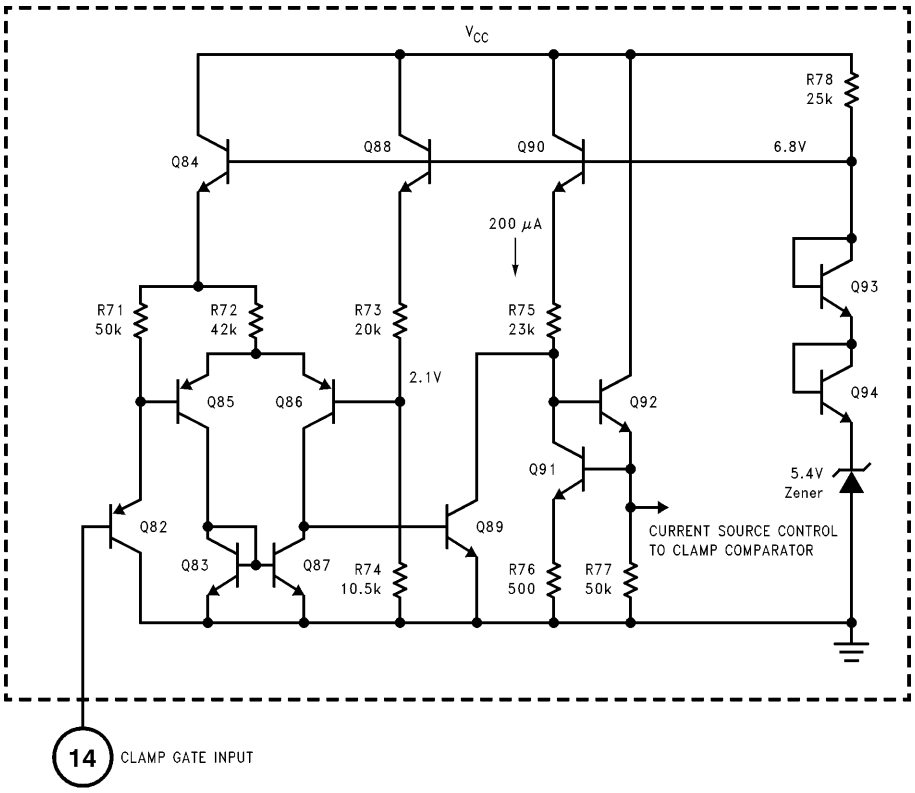

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FIGURE 7. Simplified Schematic of the LM1212 Clamp Gate Circuit

Circuit Description (Continued)

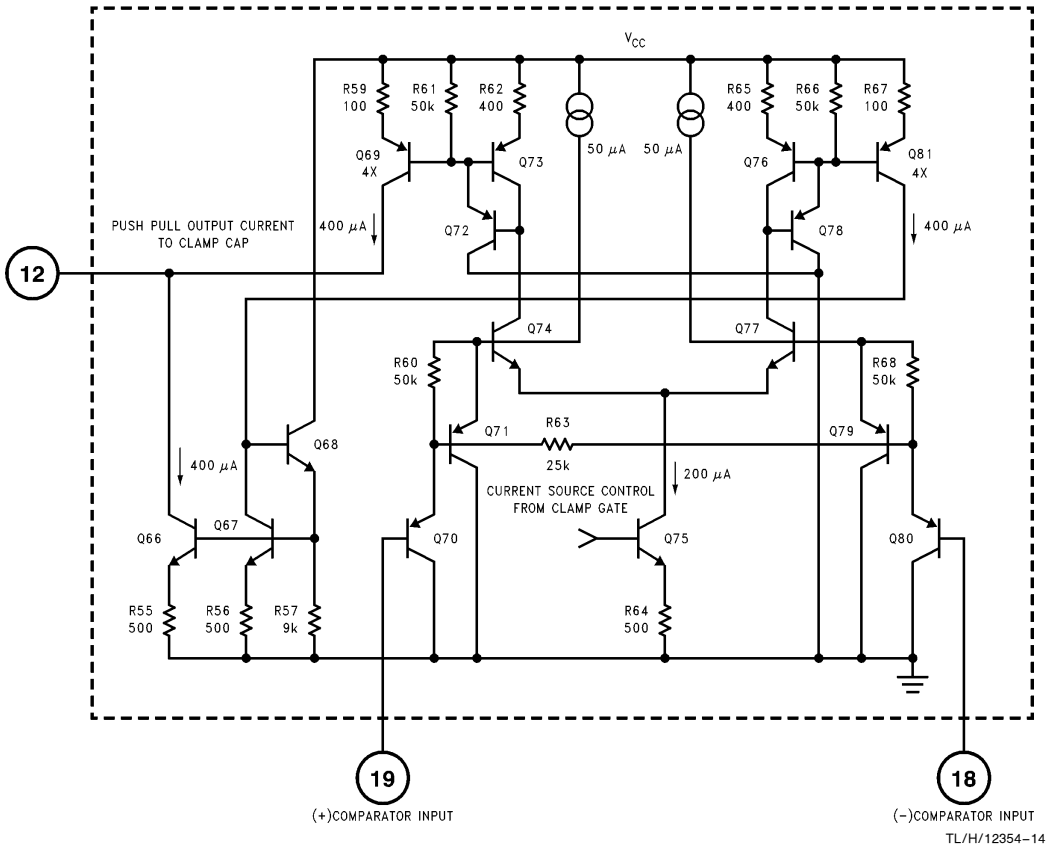

FIGURE 8. Simplified Schematic of the LM1212 Clamp Comparator Circuit

Applications of the LM1212

SINGLE VIDEO CHANNEL

A typical application for a single video channel is shown in *Figure 9*. The video signal is AC coupled to pin 6. The LM1212 internally biases the video signal to 2.6 V_{DC}. Contrast control is achieved by applying a 0V to 4V DC voltage at pin 8. The amplifier's gain is minimum (i.e., maximum signal attenuation) if pin 8 is at 0V and is maximum if pin 8 is at 4V. With pin 9 (drive control) at 0V, the amplifier has a maximum gain of 10.

For DC restoration, a clamp signal must be applied to the clamp gate input (pin 14). The clamp signal should be logic low (less than 0.8V) only during the back porch (black level reference period) interval (see *Figure 2*). The clamp gate input is TTL compatible. Brightness control is provided by applying a 0V to 4V DC voltage at pin 19. For example, if pin 19 is biased at 1V then the video signal's black level will be clamped at 1V. A 510Ω load resistor is connected from the video output pin (pin 17) to ground. This resistor biases the output stage of the amplifier. For power dissipation considerations, the load resistor should not be much less than 510Ω.

RGB VIDEO PREAMPLIFIER

Figure 10 shows an RGB video preamplifier circuit using three LM1212s. Note that pin 2 of IC1 is connected to pin 2 of IC2 and IC3 respectively. This allows IC1 to provide a master contrast control and optimum contrast tracking. Connecting pin 1 of all 3 ICs together provides the reference voltage for the contrast control. Adjusting the contrast voltage at pin 8 of IC1 will vary the gain of all three video channels. Drive control input (pin 9) of each LM1212 allows individual gain adjustment for achieving white balance.

The black level of each video channel can be individually adjusted to the desired voltage by adjusting the voltage at pin 19. In a DC-coupled cathode drive application, adjusting the voltage at pin 19 of each IC will provide cutoff adjustment. In an AC-coupled cathode drive application, the video signal is AC coupled and DC restored at the cathode. In such an application, the video signal's black level may be clamped to the desired level by simply biasing pin 19 to the black level voltage by using a voltage divider at pin 19.

Applications of the LM1212 (Continued)

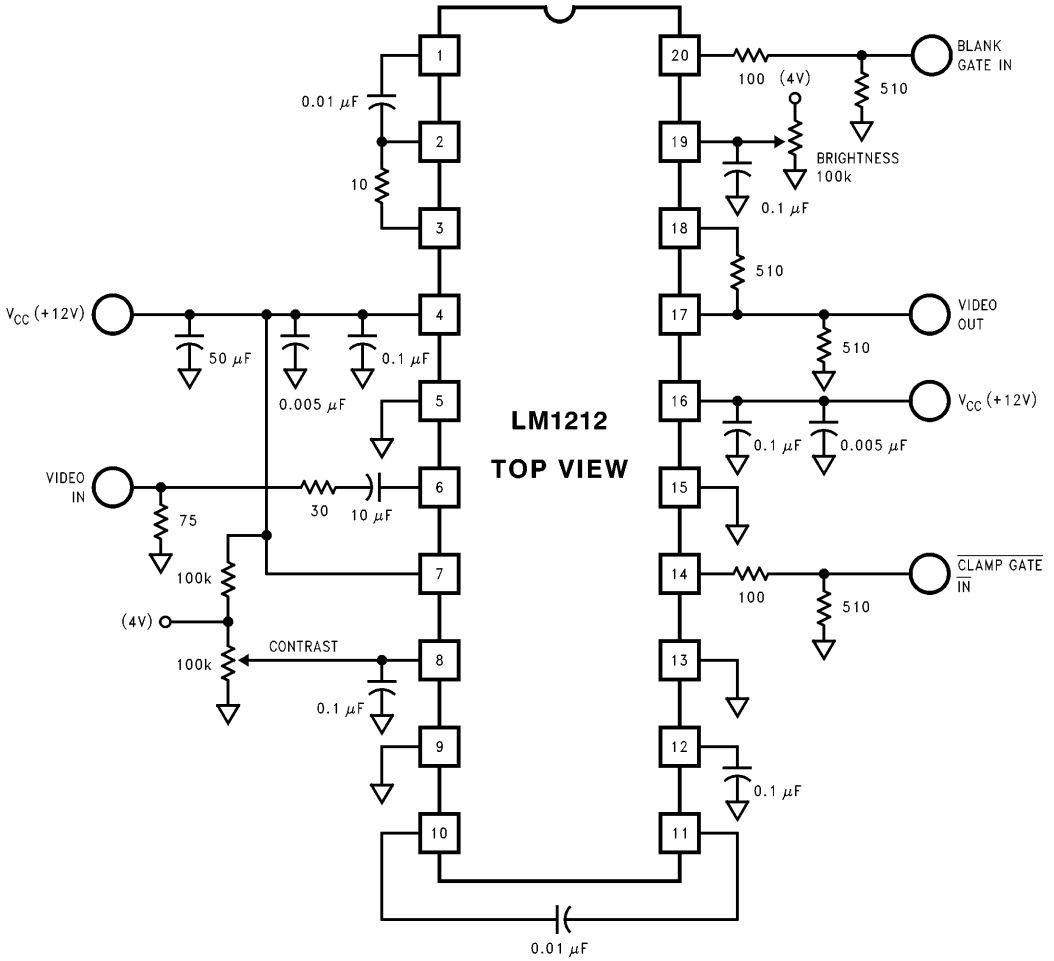

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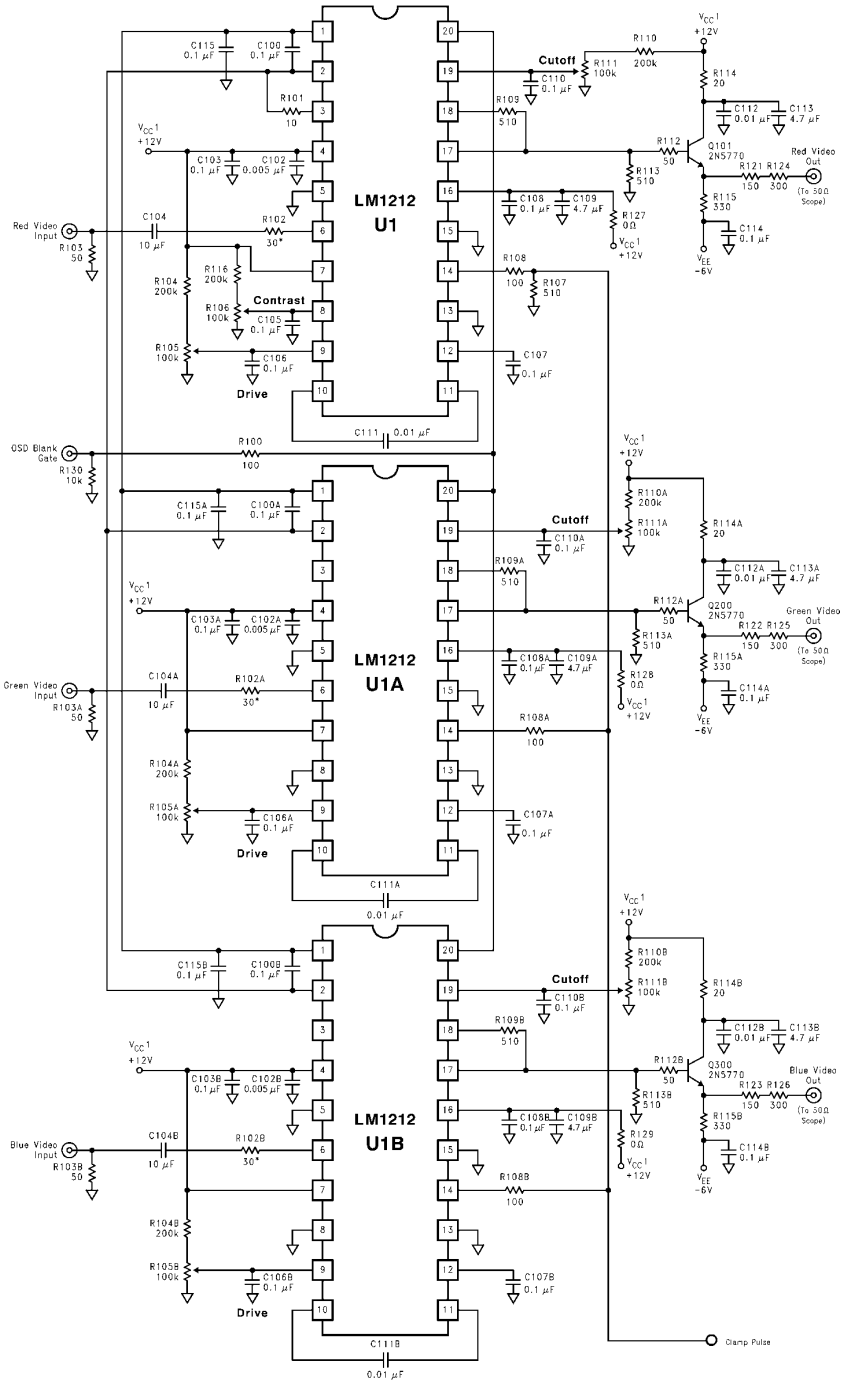
FIGURE 9. Typical LM1212 Application (Single Video Channel)

Applications of the LM1212 (Continued)



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* **Note:** All video inputs must have a series 30Ω resistor for protection against EOS (Electrical Over Stress).

FIGURE 10. LM1212 Video Preamp Demonstration Board Schematic

Applications of the LM1212 (Continued)

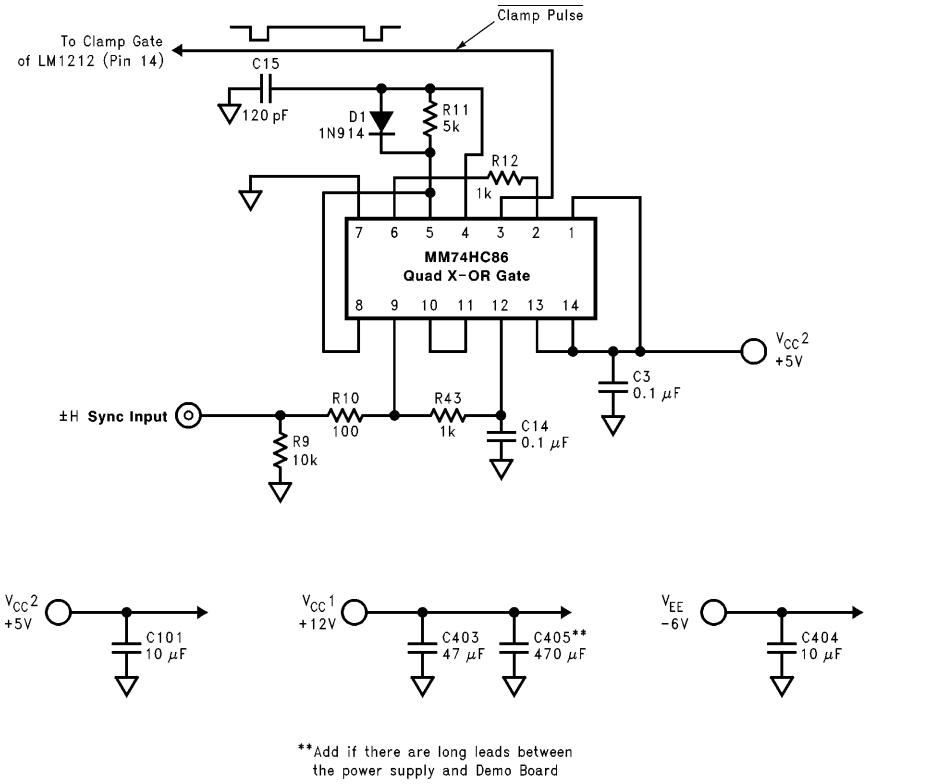

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FIGURE 10. LM1212 Video Preamp Demonstration Board Schematic (Continued)

Power Down Characteristics

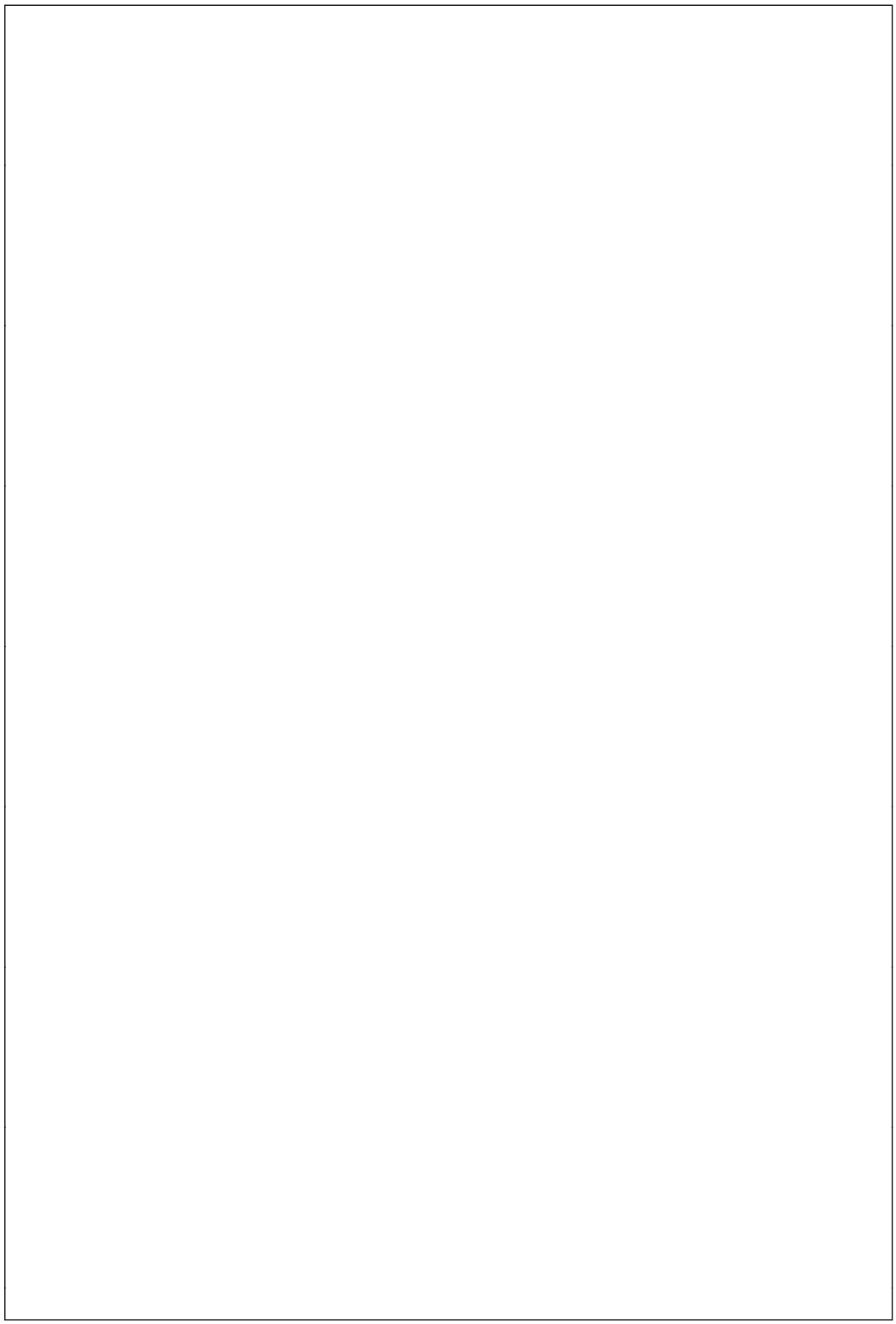
The LM1212 includes a built-in power down spot killer to prevent a flash on the screen upon power down. The LM1212's output voltage decreases as the device is being powered down, thus preventing a flash on the screen. In some preamplifiers, the video output signal may go high as the device is being powered down. This may cause a whiter-than-white level at the output of the CRT driver, thus causing a flash on the screen.

PC Board Layout Considerations

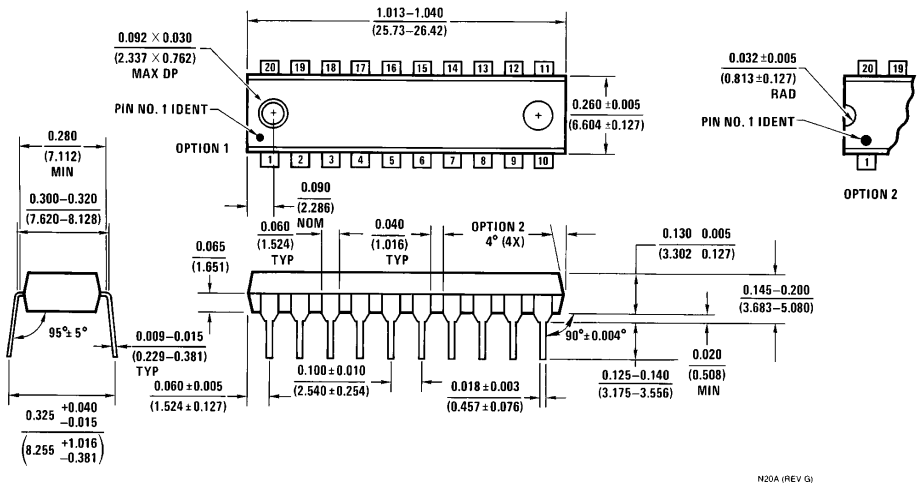
For optimum performance and stable operation, a double-sided printed circuit board with adequate ground plane and power supply decoupling as close to the V_{CC} pins as possible is recommended. For suggestions on optimum PC board layout, please see the reference section below.

Reference

Ott, Henry W, *Noise Reduction Techniques in Electronic Systems*, John Wiley & Sons, New York, 1976.



Physical Dimensions inches (millimeters) unless otherwise noted



Order Number LM1212N
NS Package Number N20A

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