National Semiconductor

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# LM1044 Analog Video Switch

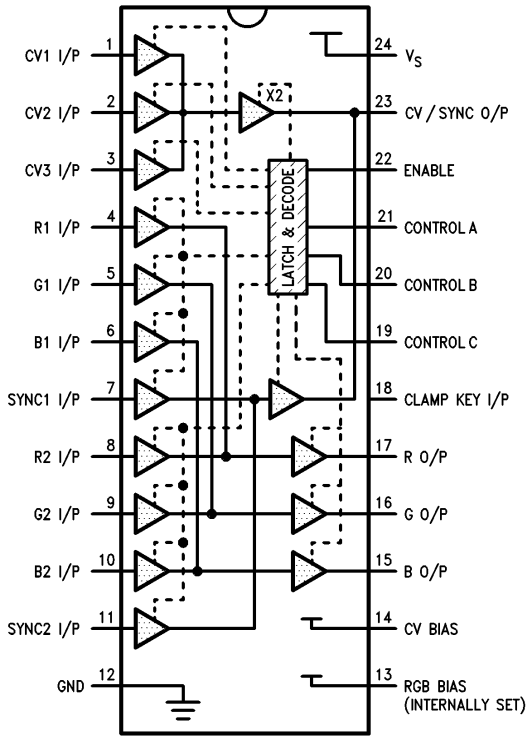
## General Description

Primarily intended for, but not restricted to, the switching of video signals, the LM1044 is a monolithic DC controlled analog switch with buffered outputs, allowing the selection of three 5 MHz bandwidth, 6 dB gain channels, or two RGB + Sync, 30 MHz bandwidth, 0 dB gain channels. Channel selection is achieved via latched, TTL compatible, logic inputs which may be controlled by microprocessor derived signals. The device is supplied in a 24 pin dual in line plastic package.

## Features

- Wide RGB bandwidth, typically 30 MHz
- High signal to noise ratio, typically 60 dB
- Excellent channel isolation typically −60 dB @ 5 MHz
- High RGB output currents; typically 4 mA peak
- RGB channels may be DC restored or clamped
- Logically compatible with the LM1038 stereo audio switch IC

## Block Diagram

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**Order Number LM1044N**
**See NS Package Number N24A**

RRD-B30M115/Printed in U. S. A.

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_S$) | 17V |
| Package Dissipation at $T_A = 25°C$ (Note 8) | 2.0W |
| Voltage at Control and Signal Inputs | −0.2V to Vs +0.2V |
| Output Current, $I_{23}$, $I_{17}$, $I_{16}$, $I_{15}$ | 10 mA |
| ESD Susceptibility (Note 5) | 2000V |
| Operating Temperature | 0°C to +70°C |
| Storage Temperature | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 265°C |
| Junction Temperature | 150°C |

## Electrical Characteristics $V_S = 12V$, $R_L = 600\Omega$, $C_L = 20$ pF, $T_A = 25°C$ unless otherwise stated

| Parameter | Conditions | Test Limit (Note 6) | | Design Limit (Note 7) | | | Units |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Typ | Max | |
| Supply Voltage, Vs | | 8 | 16 | 8 | 12 | 16 | V |
| Supply Current | RGB1 Channel Selected with No Input Signals Applied | | 60 | | 42 | 60 | mA |
| Control Inputs Logic High Level<br>Control Inputs Logic Low Level | Control Inputs A, B, C and Enable Input | 2.0 | <br>0.8 | 2.0 | | <br>0.8 | V<br>V |
| Enable Input Current, Pin 22 | 0V to Vs | | | | 2 | 10 | μA |
| Control Input Current | 0V Logic Level<br>5V Logic Level | | | | 20<br>250 | 50<br>500 | μA<br>μA |
| Enable Pulse Width | | | | 5 | | | μs |
| Channel Select Time | | | | | 5 | 7 | μs |
| **COMPOSITE VIDEO CHANNELS** | Inputs—Pins 1, 2, 3<br>Output—Pin 23 | | | | | | |
| Maximum Input Voltage Swing | For Output THD = 1% @ 1 kHz | | | 1.2 | | | $V_{p-p}$ |
| Input Impedance | | | | 1.2 | 1.5 | 1.7 | kΩ |
| Dynamic Output Impedance | | | | | 10 | | Ω |
| Voltage Gain | Input Signal = 0.5 $V_{p-p}$ @ 100 kHz | 5.3 | | 5.3 | 5.8 | 6.3 | dB |
| Bandwidth | Input Signal = 0.5 $V_{p-p}$, −3 dB, | 4.0 | | 4.0 | 5.0 | | MHz |
| Signal to Noise Ratio | Bandwidth = 5 MHz | | | | 60 | | dB |
| Channel Isolation (Note 1) | Input Signal = 0.5 $V_{p-p}$ @ 3 MHz | | | | 60 | | dB |
| Crosstalk (Note 2) | Input Signal = 0.5 $V_{p-p}$ @ 3 MHz | | | | −60 | | dB |
| Load Resistance (Note 3) | AC Coupled<br>DC Coupled to GND | | | 600<br>2 | | | Ω<br>kΩ |
| Power Supply Rejection Ratio | $V_S$ Modulated 1 $V_{p-p}$ @ 1 kHz | 40 | | | 50 | | dB |
| CV Bias (Pin 14) Input Impedance | | | | | 1.0 | | kΩ |

## Electrical Characteristics

$V_S$ = 12V, $R_L$ = 600Ω, $C_L$ = 20 pF, $T_A$ = 25°C unless otherwise stated (Continued)

| Parameter | Conditions | Test Limit (Note 6) | | Design Limit (Note 7) | | | Units |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Typ | Max | |
| **RGB CHANNELS** | Inputs—Pins 4, 5, 6, 8, 9, 10<br>Outputs—Pins 15, 16, 17 | | | | | | |
| CLAMP INPUT-Pin 18<br>Minimum Input Voltage<br>Maximum Input Voltage | <br>For Clamp on<br>For Clamp off | | | <br>9 | | <br>5 | <br>V<br>V |
| Input Current | Pin 18 = 0V | | | | | 10 | μA |
| Clamp Pulse Delay (Note 4) | | | | | | 0.2 | μs |
| Maximum Input Voltage Swing | for Output THD = 1% @ 1 kHz | | | 3.0 | | | $V_{p-p}$ |
| Input Bias Current | Clamp off, Channel Selected | | | | 20 | | μA |
| Dynamic Output Impedance | | | | | 20 | | Ω |
| Voltage Gain | Input Signal = 1 $V_{p-p}$ @ 100 kHz | −0.5 | | −0.5 | 0 | +0.5 | dB |
| Bandwidth | Input Signal = 1 $V_{p-p}$, −3 dB | 6.0 | | 24 | 30 | | MHz |
| Signal to Noise Ratio | $R_{IN}$ = 50Ω, Bandwidth = 10 MHz | | | | 60 | | dB |
| Load Resistance (Note 3) | AC Coupled 3 $V_{p-p}$<br>DC Coupled to GND | | | 600<br>2 | | | Ω<br>kΩ |
| Channel Isolation (Note 1) | Input Signal = 1 $V_{p-p}$ @ 5 MHz | | | | 60 | | dB |
| Crosstalk (Note 2) | Input Signal = 1 $V_{p-p}$ @ 5 MHz | | | | −50 | | dB |
| Power Supply Rejection Ratio | $V_S$ Modulated 1 $V_{p-p}$ @ 1 kHz | | | | 50 | | dB |
| Pin 13 Output Impedance | | | | | 60 | | Ω |
| **SYNC CHANNELS** | Inputs—Pins 7, 11<br>Outputs—Pin 23 | | | | | | |
| Maximum Input Voltage Swing | for Output THD = 1% @ 1 kHz | | | 3.0 | | | $V_{p-p}$ |
| Input Impedance | | | | 1.8 | 2.3 | 2.8 | kΩ |
| Dynamic Output Impedance | | | | | 40 | | Ω |
| Voltage Gain | Input Signal = 1 $V_{p-p}$ @ 100 kHz | −1.0 | | −1.0 | −0.4 | +0.2 | dB |
| Bandwidth | Input Signal = 1 $V_{p-p}$, −3 dB, | 6.0 | | 18 | 24 | | MHz |
| Signal to Noise Ratio | $R_{IN}$ = 50Ω, Bandwidth = 10 MHz | | | | 60 | | dB |

**Note 1:** CV channels defined with a CV mute condition set up (ABC = 001) and all CV inputs driven. Isolation is the output measured with respect to the input level for $R_L$ of 600Ω. Channel isolation for RGB channels is measured in the same way with signals applied to the R, G or B inputs while a RGB mute condition is selected.

**Note 2:** CV crosstalk measured with selected channel input AC grounded and with signal applied to the other CV inputs. Resulting output voltage is measured with $R_L$ of 600Ω. RGB crosstalk is measured similarly with signals applied to unselected channel inputs and measuring the selected channel output. Note that high frequency crosstalk measurements are very dependent on board layout. An effective ground plane and input to input shielding are required.

**Note 3:** DC output current sourced from device to load should not exceed 10 mA, care should be taken to avoid shorting outputs to GND.

**Note 4:** Delay between clamp pulse input at Pin 18 and resulting clamping action as seen at RGB inputs.

**Note 5:** Human body model, 100 pF discharged through a 1.5 kΩ resistor.

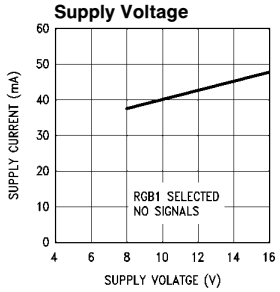
**Note 6:** Guaranteed and 100% production tested.

**Note 7:** Design limits are guaranteed to National's AOQL, but are not 100% production tested.

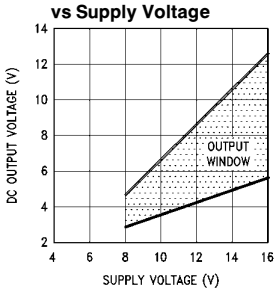
**Note 8:** When operating at elevated temperatures, the maximum power dissipation must be derated based on a maximum junction temperature of 150°C and $\theta_{JA}$ = 60°C/W.

## Typical Performance Characteristics

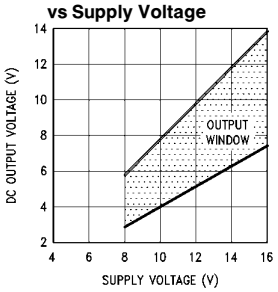
**Supply Current vs Supply Voltage**



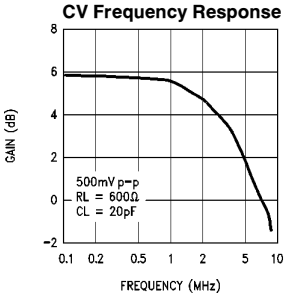

**CV Output Signal Range vs Supply Voltage**



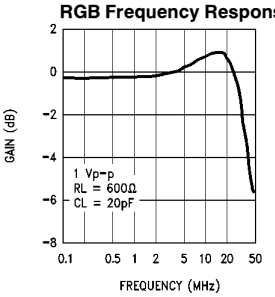

**RGB Output Signal Range vs Supply Voltage**



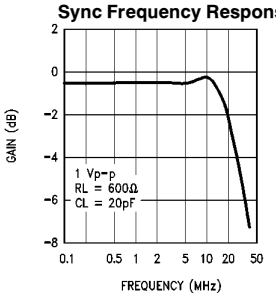

**CV Frequency Response**



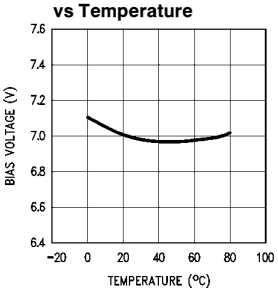

**RGB Frequency Response**



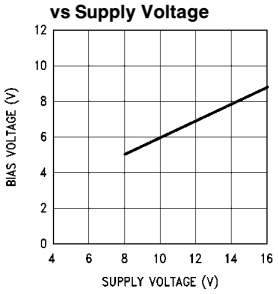

**Sync Frequency Response**




**CV and RGB Bias vs Temperature**




**CV and RGB Bias vs Supply Voltage**

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## Pin Description

**Note:** The pin designations CV, R, G, B, and Sync are assigned for the convenience of description and are not intended to be a limitation. For example RGB could be YUV, or they could all be independent signal sources.

| | |
|---|---|
| Pin 1 | Composite video input 1 (CV1), biased internally via 1.8 kΩ to $\frac{V_S}{2} + 1V$. |
| Pin 2 | Composite video input 2 (CV2), biased as for pin 1 (CV1) above. |
| Pin 3 | Composite video input 3 (CV3), biased as for pin 1 (CV1) above. |
| Pin 4 | RGB input R1. This pin is internally biased via a clamp circuit to $\frac{V_S}{2} + 1V$ and should be AC coupled to a low impedance source. The input coupling capacitor also acts as a clamp capacitor, see application notes. |
| Pin 5 | RGB input G1, biased as for pin 4 (R1) above. |
| Pin 6 | RGB input B1, biased as for pin 4 (R1) above. |
| Pin 7 | Sync input S1, biased internally via 2.5k to $\frac{V_S}{2} + 1V$. |
| Pin 8 | RGB input R2, biased as for pin 4 (R1) above. |
| Pin 9 | RGB input G2, biased as for pin 4 (R1) above. |
| Pin 10 | RGB input B2, biased as for pin 4 (R1) above. |
| Pin 11 | Sync input S2, biased as for pin 7 (S1) above. |
| Pin 12 | Negative supply (GND) |
| Pin 13 | Connect a capacitor to GND to decouple the internal bias of the RGB amplifiers. |
| Pin 14 | Internal bias for the CV and Sync Amplifiers, decouple with a capacitor to GND. |
| Pin 15 | B Output. |
| Pin 16 | G Output. |
| Pin 17 | R Output. |
| Pin 18 | This is the clamp pulse input pin. A positive going pulse activates the RGB input bias clamps. See application notes. |
| Pin 19 | Channel select input, control C. |
| Pin 20 | Channel select input, control B. |
| Pin 21 | Channel select input, control A. |
| Pin 22 | Enable input for control latches. Channel selection is locked while this input is low and is updated when high. The minimum enable pulse width is 5 μs. |
| Pin 23 | CV output or Sync output when an RGB channel is selected. |
| Pin 24 | Supply pin ($V_S$). This pin should be well decoupled at high frequencies, a 100 nF capacitor connected close to the supply pins is normally adequate. |

## Application Notes

### DEVICE DESCRIPTION

The LM1044 video switch circuit has a configuration as illustrated in *Figure 1* and consists of a 3 input to 1 output, 5 MHz switch with 6 dB gain, three 2 input to 1 output, 30 MHz, 0 dB gain switches, coupled together with a 2 input to 1 output switch sharing the 3 way switch output. All switch stages are current switched differential amplifers with feedback, providing low impedance buffered outputs. Latched logic inputs with control decoding are provided for switch control and a DC clamp facility is available on the 30 MHz channels.

The principle application of this device is the selection between various composite video (CV) or Red, Green, and Blue (RGB) sources now found in video systems using various signal sources, e.g., VCR's, satellite receivers, home computers and video games. Other possible application examples, for example security camera switching, are shown towards the end of these notes.

The 5 MHz channels are ideally suited for the switching of composite video sources and have a gain of 6 dB to allow amplification from terminated inputs back up to internal signal levels. The 30 MHz channels are suitable for direct RGB inputs to display high quality graphics and will also handle high quality linear signals. The fourth switch channel shares the CV output pin and is ideal for routing synchronization signals from the RGB/YUV sources into the path to the sync separator and timebase circuits.

### CHANNEL SELECTION

The switch selections are made via the enable and 3 logic control inputs, according to the truth table shown on the following page. This gives a choice of 3 CV video signal sources or 2 RGB plus Sync signals on the video display.

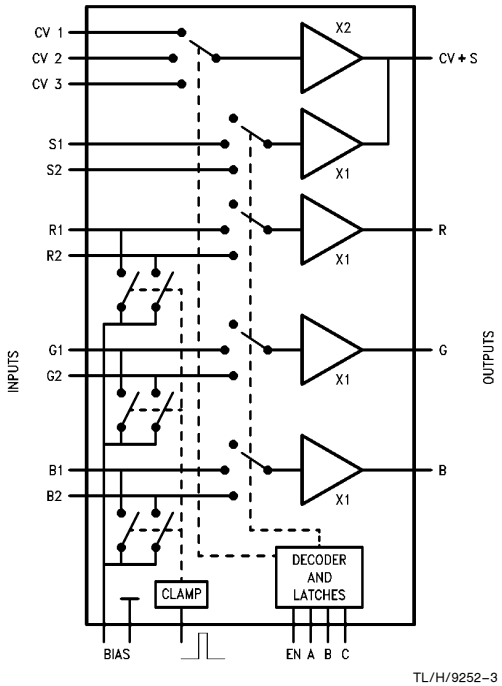


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**FIGURE 1**

## Application Notes (Continued)

**Truth Table**

| Control Logic | | | | Channel Selected |
|---|---|---|---|---|
| EN 22 | C 19 | B 20 | A 21 | |
| 1 | 0 | 0 | 0 | CV1, RGB Outputs Muted |
| 1 | 0 | 0 | 1 | CV2, RGB Outputs Muted |
| 1 | 0 | 1 | 0 | CV3, RGB Outputs Muted |
| 1 | 0 | 1 | 1 | RGB1 with Sync1 |
| 1 | 1 | 1 | 1 | RGB2 with Sync2 |
| 1 | 1 | 1 | 0 | Mute |
| 1 | 1 | 0 | 1 | Mute |
| 1 | 1 | 0 | 0 | Mute |
| 0 | X | X | X | Previous selection retained |

The shaded section of the truth table indicates selection compatible with the LM1038 four channel stereo audio switch logic to give a possible selection of CV1 + Audio1, CV2 + Audio2, CV3 + Audio3, RGB1 + Audio4 and RGB2 + Mute or Audio4; see *Figure 3.*

The mute conditions in the table correspond to disabled CV/Sync (output pulled low) and high impedance RGB outputs which may be connected in parallel with other device outputs for further expansion of the switch system. If all the RGB inputs are being used to switch composite video signals then the RGB outputs can be connected into the CV inputs to allow multiplexing down to 1 output from a large number of input signals.

### LOGIC AND ENABLE INPUTS

If undriven the enable input will assume a high impedance logic 1 condition and should be defined externally. The Logic selection inputs have internal pulldowns, typically 20 kΩ, which will define logic low levels if unconnected, giving CV1 in default of any other control input.

### INPUT BIAS FOR CV CHANNELS

The CV and Sync inputs are biased via internal 1.5 kΩ and 2.3 kΩ resistors, respectively, to the internally generated 7V bias ($V_S$ = 12V) level at pin 14. Input coupling capacitors need to be chosen to give an adequate low frequency response when driving the 1.5 kΩ input impedance, for example, for less than 2% tilt on a frame rate waveform 330 μF will be required. Depending on the effectiveness of any following clamp circuitry the input coupling capacitors may be reduced in value. These inputs may also be driven with DC coupled signals, provided the standing DC level is sufficiently near to 7V to maintain the output within the output signal range (4.5 to 8.5V for $V_S$ = 12V).

The bias at pin 14 has a DC output resistance typically of 1 kΩ and requires a decoupling capacitor to properly define the gain and crosstalk. To ensure an adequate low frequency response this capacitor should be 100 μF or more. This pin may also be biased from an external voltage source provided the output remains within the output window. Note this bias will also affect the voltage at pin 13.

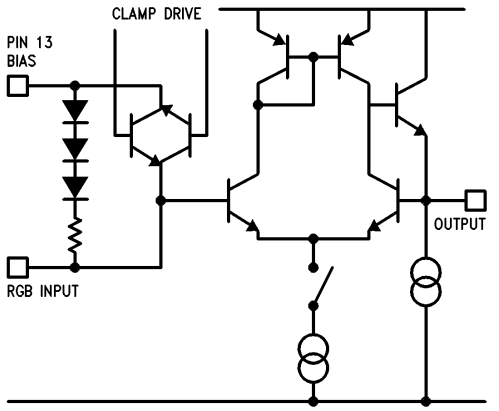
### INPUT BIAS FOR RGB CHANNELS

The 6 RGB inputs may be biased in one of three ways;

1) DC restored above an internal 4.5V level
2) Clamped to an internal 7V bias level
3) Driven directly with DC coupled signals

With an AC coupled input signal and the clamp pulse held low the negative going peaks will DC restore to a level greater than 3 diode drops below the reference bias level at pin 13, typically 4.5V for $V_S$ = 12V. The source resistance of the diode restoring path is 1 kΩ for currents below 200 μA.

**Simplified Schematic of RGB Stage**

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The simplified schematic of the CV stage is virtually identical to the RGB stage except that the CV stage does not incorporate the clamp circuitry.

Clamping to the internal 7V bias is arranged by applying a positive going clamp pulse to pin 18 during a time when the input signals are at a black reference level. This is usually during the back porch or during the blanking period of signals without syncs. The clamp pulse width should not be less than 3 μs. During the time pin 18 is high all six inputs R1, R2, G1, G2, B1 and B2 are connected to the RGB bias voltage developed at pin 13, charging the input coupling capacitors to this level. These coupling capacitors are chosen to optimize value versus tilt introduced during the active line period. A value of 330 μF gives less than 1% tilt for input currents less than 20 μA. The effective impedance of the clamp path when conducting is 300Ω. The voltage at pin 13 is a low impedance, 60Ω, buffered version of the CV bias voltage at pin 14 and decoupling is required to remove high frequencies and maintain channel separation. The voltage at pin 13 may be changed by driving pin 14 as described for CV bias.

## Application Notes (Continued)

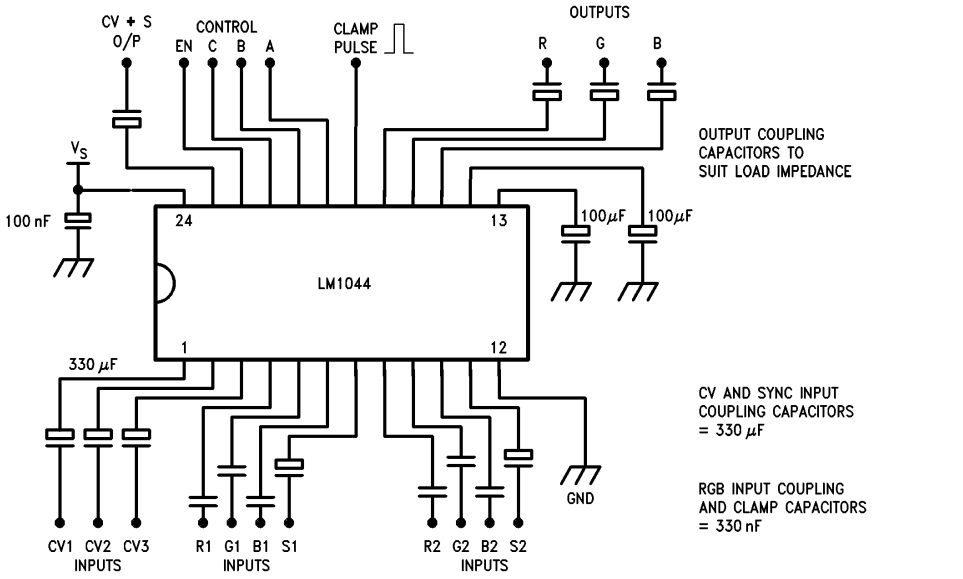


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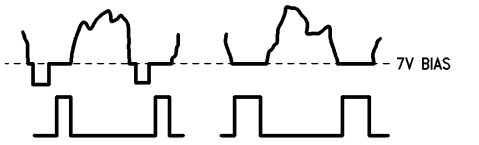
**FIGURE 2. LM1044 Basic Application Circuit**

**Relation of Clamp Pulse to Video**

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If the clamp pulse input is held low the RGB inputs may be driven directly with DC coupled signals provided the levels are such as to remain within the output window. Such signals could be directly coupled from the RGB outputs of a preceeding LM1044, avoiding the need for coupling capacitors when expanding the switching capability. External resistive biasing to the bias voltage available at pin 13 may also be used for a mean level bias with AC coupled signals not having reference levels.

**OPERATION AT SUPPLIES OTHER THAN 12V**

The LM1044 may be operated at supply voltages between 8V and 16V. Note that the CV and RGB bias voltages, together with the clamp pulse threshold, will track with supply variations whilst the logic input thresholds will remain essentially constant. At lower supply voltages the signal handling may be optimized with an external bias voltage to pin 14.

## Application Notes (Continued)

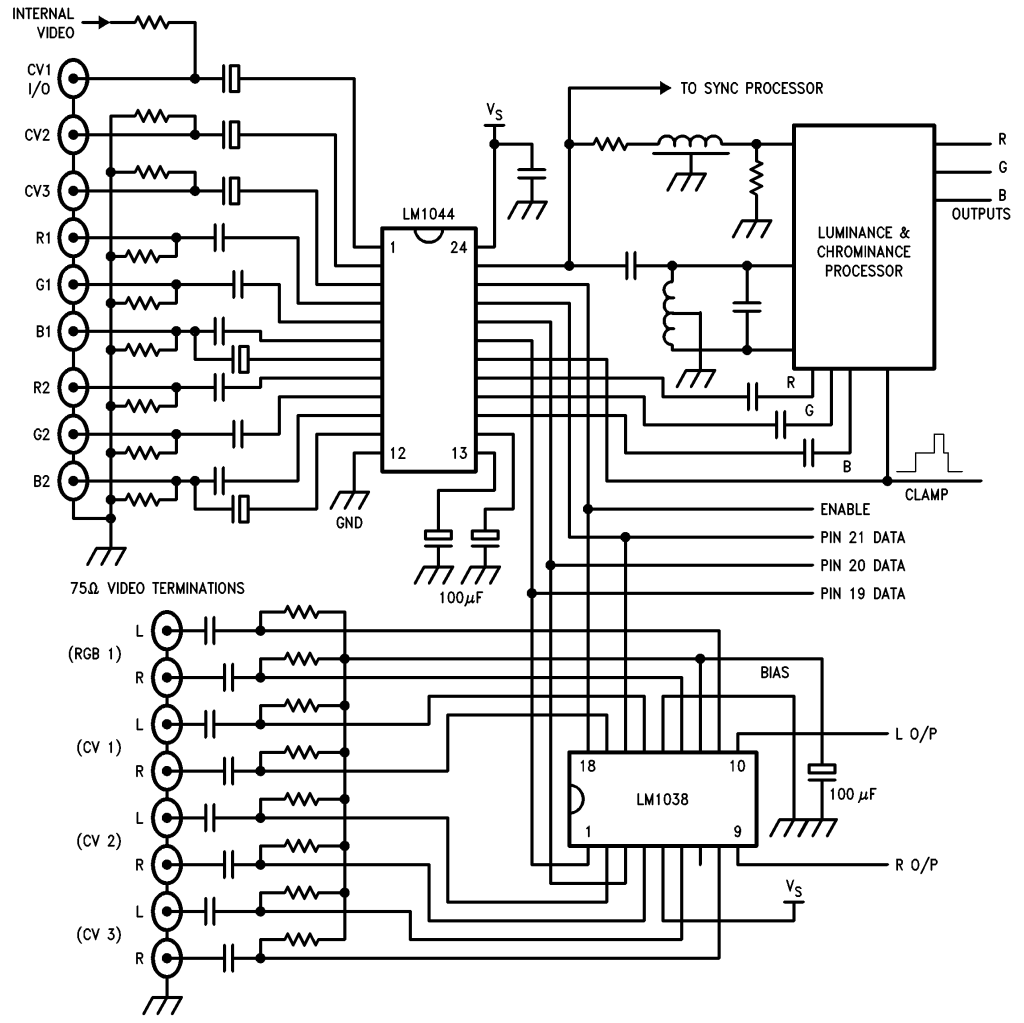


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**FIGURE 3. LM1044 Application Circuit Showing System Interfacing and LM1038**

### OPERATION WITH SPLIT SUPPLIES

The LM1044 may be operated with split supplies with due regard to the maximum supply voltage (16V) and output signal range. An example of operation in this way is illustrated below. With ±5V and pin 14 held at 0V the RGB outputs can swing +2V, −1.5V and the CV and Sync output can swing +1.3V, −1.3V. Similarly with +10V, −5V supplies, pin 14 to 0V, RGB output swings of +5.5V, −1.5V and CV/Sync swings of +4.5V and −1.5V can be obtained. This supply configuration has the advantage that pin 14 can be grounded and all signals may be DC coupled avoiding the need for coupling capacitors. Offsets introduced are typically −30 mV for CV and RGB channels, and −140 mV for Sync channels.

### OTHER APPLICATIONS

The LM1044 can be used in other than the standard CV with RGB circuit and an example is given below of a dual 6 input to 1 output multiplexer for video or indeed any kind of signals up to 2 $V_{p-p}$. In this particular example the RGB outputs are cross-coupled into the CV inputs of the other channel to complete the multiplexing down to 2 outputs. The clamp circuits are disabled to allow direct drive on the inputs. Such circuits are ideal for security cameras and other multiple video source monitoring systems.

## Application Notes (Continued)

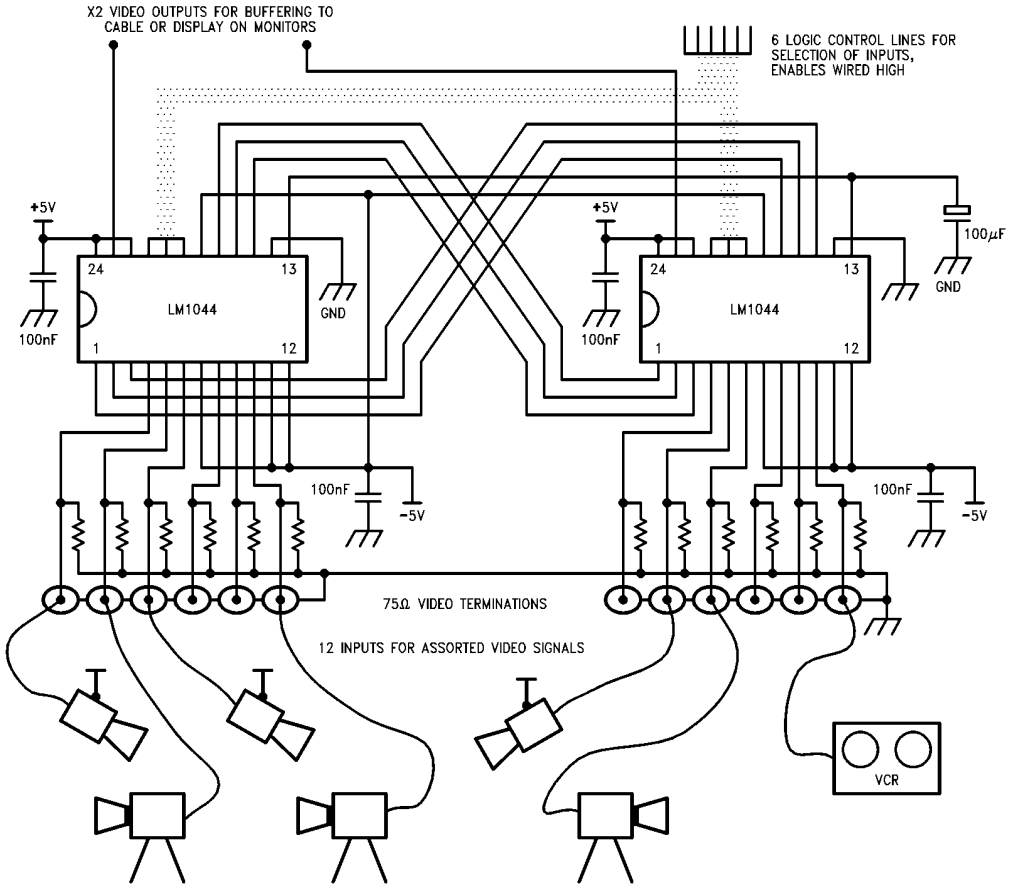


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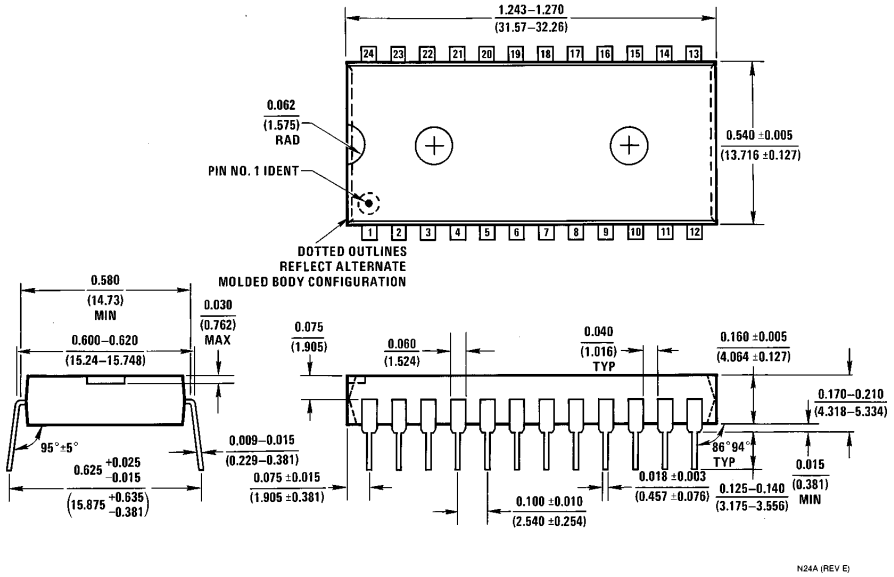
**FIGURE 4. Application Circuit Example Using Two LM1044 Devices as a Dual 6 Channel Multiplexer and Illustrating Use of Split Supplies**

## Physical Dimensions inches (millimeters)




**Molded Dual-In-Line Package (N)**
**Order Number LM1044N**
**NS Package Number N24A**

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