SCLS304B - JANUARY 1996 - REVISED DECEMBER 2002

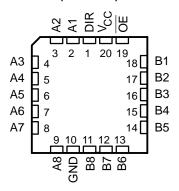
- Wide Operating Voltage Range of 2 V to 6 V
- **High-Current 3-State Outputs Can Drive Up** To 15 LSTTL Loads
- Low Power Consumption, 80-μA Max I_{CC}

SN54HC645...J OR W PACKAGE SN74HC645 . . . DW, N, OR NS PACKAGE (TOP VIEW)

DIR [1	\bigcup_{20}] v _{cc}
A1 [2	19	OE
A2 [3	18	B1
A3 [4	17	B2
A4 [5	16] B3
A5 [6	15] B4
A6 [7	14] B5
A7 [8	13] B6
A8 [9	12] B7
GND [10	11] B8

- Typical $t_{pd} = 12 \text{ ns}$
- ±6-mA Output Drive at 5 V
- Low Input Current of 1 µA Max
- **True Logic**

SN54HC645...FK PACKAGE (TOP VIEW)



description/ordering information

These octal bus transceivers are designed for asynchronous two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the device so the buses are effectively isolated.

ORDERING INFORMATION

TA	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube	SN74HC645N	SN74HC645N
4000 1- 0500	2010 PW	Tube	SN74HC645DW	110045
-40°C to 85°C	SOIC – DW	Tape and reel	SN74HC645DWR	HC645
	SOP - NS	Tape and reel	SN74HC645NSR	HC645
	CDIP – J	Tube	SNJ54HC645J	SNJ54HC645J
–55°C to 125°C	CFP – W	Tube	SNJ54HC645W	SNJ54HC645W
	LCCC – FK Tube		SNJ54HC645FK	SNJ54HC645FK

[†]Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

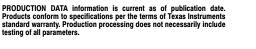
FUNCTION TABLE

INP	UTS	ODED ATION							
Œ	DIR	OPERATION							
L	L	B data to A bus							
L	Н	A data to B bus							
Н	X	Isolation							

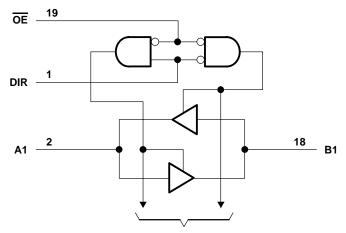


testing of all parameters.

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logic diagram (positive logic)



To Seven Other Transceivers

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC}) (see Note	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC}) (see	Note 1) ±20 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±35 mA
Continuous current through V _{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 2): DW p	ackage 58°C/W
N pac	kage 69°C/W
NS pa	ackage 60°C/W
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

			SI	N54HC64	15	SN	174HC64	5	UNIT	
			MIN	NOM	MAX	MIN	NOM	MAX	UNII	
VCC	Supply voltage		2	5	6	2	5	6	V	
		V _{CC} = 2 V	1.5			1.5				
ViH	High-level input voltage	V _{CC} = 4.5 V	3.15			3.15			V	
		V _{CC} = 6 V	4.2			4.2				
	Low-level input voltage	V _{CC} = 2 V			0.5			0.5		
٧ _{IL}		V _{CC} = 4.5 V			1.35			1.35	V	
		VCC = 6 V			1.8			1.8		
٧ı	Input voltage		0		VCC	0		VCC	V	
٧o	Output voltage		0		VCC	0		VCC	V	
		V _{CC} = 2 V			1000			1000		
Δt/Δν	Input transition rise/fall time	V _{CC} = 4.5 V			500			500	ns	
		V _{CC} = 6 V			400			400		
TA	Operating free-air temperature		-55		125	-40		85	°C	



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

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NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

D4.0	AMETER	TEOT 00	NOTIONO	v _{cc}	Т	A = 25°C	;	SN54H	IC645	SN74HC645		LINUT
PAR	AMETER	TEST CO	TEST CONDITIONS		MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
				2 V	1.9	1.998		1.9		1.9		
		VI = VIH or VIL	I _{OH} = -20 μA	4.5 V	4.4	4.499		4.4		4.4		
∨он				6 V	5.9	5.999		5.9		5.9		V
			$I_{OH} = -6 \text{ mA}$	4.5 V	3.98	4.3		3.7		3.84		
			$I_{OH} = -7.8 \text{ mA}$	6 V	5.48	5.8		5.2		5.34		
			2 V		0.002	0.1		0.1		0.1		
		$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 20 \mu A$	4.5 V		0.001	0.1		0.1		0.1	
VoL				6 V		0.001	0.1		0.1		0.1	V
			I _{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
			I _{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
II	DIR or OE	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
loz	A or B	VO = VCC or 0		6 V		±0.01	±0.5		±10		±5	μΑ
ICC		$V_I = V_{CC}$ or 0,	IO = 0	6 V			8		160		80	μΑ
Ci	DIR or OE			2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то		T,	Վ = 25° C	;	SN54H	IC645	SN74H	C645	LINUT
PARAMETER	(INPUT)	(OUTPUT)	vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V		40	105		160		130	
t _{pd}	A or B	B or A	4.5 V		15	21		32		26	ns
			6 V		12	18		27		22	
		A or B	2 V		125	230		340		290	
t _{en}	ŌĒ		4.5 V		23	46		68		58	ns
				6 V		20	39		58		49
		A or B	2 V		74	200		300		250	ns
^t dis	ŌĒ		4.5 V		25	40		60		50	
			_	6 V		21	34		51		43
		A or B	2 V		20	60		90		75	ns
t _t			4.5 V		8	12		18	·	15	
			6 V		6	10		15		13	

SN54HC645, **SN74HC645 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS**

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switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

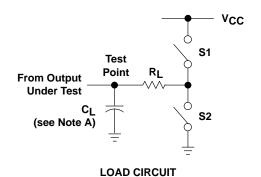
DADAMETED	FROM	то		T	√ = 25°C	;	SN54HC645		SN74HC645		UNIT
PARAMETER	(INPUT)	(OUTPUT)	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
		B or A	2 V		54	135		200		170	
^t pd	A or B		4.5 V		18	27		40		34	ns
·			6 V		15	23		34		29	
		A or B	2 V		150	270		405		335	ns
t _{en}	ŌĒ		4.5 V		31	54		81		67	
			6 V		25	46		69		56	
			2 V		45	210		315		265	
t _t		A or B	4.5 V		17	42		63		53	ns
			6 V		13	36		53		45	

operating characteristics, $T_A = 25^{\circ}C$

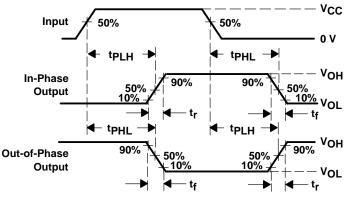
	PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per transceiver	No load	40	pF



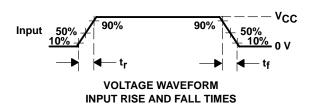
PARAMETER MEASUREMENT INFORMATION

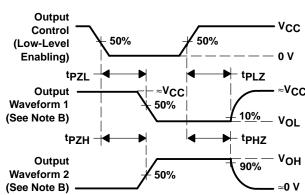


PARAI	METER	RL	CL	S1	S2
t _{PZH} 50 pF		Open	Closed		
t _{en}	tPZL	1 K22	150 pF	Closed	Open
4	tPHZ	1 k Ω	50 pF	Open	Closed
^t dis	tPLZ	1 K22	50 pr	Closed	Open
t _{pd} or	tŧ	l	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES





VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

- NOTES: A. C_L includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_O = 50 Ω , t_f = 6 ns, t_f = 6 ns.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms







i.com 6-Dec-2006

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN54HC645J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SN74HC645DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC645DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC645DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC645DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC645N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74HC645NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74HC645NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC645NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54HC645FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54HC645J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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