



**DDR SDRAM Module 256Mbyte (32Mx64bit), based on 32Mx8, 4Banks,
8K Ref., SO-DIMM**

Part No. HDD32M64B8

GENERAL DESCRIPTION

The HDD32M64B8 is a 32M x 64 bit Double Data Rate(DDR) Synchronous Dynamic RAM high-density memory module. The module consists of eight CMOS 32M x 8 bit with 4banks DDR SDRAMs in 66pin TSOP-II 400mil packages and 2K EEPROM in 8-pin TSSOP package on a 200-pin glass-epoxy. Four 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each DDR SDRAM. The HDD32M64B8 is a SO-DIMM(Small Outline Dual in line Memory Module) .Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allows the same device to be useful for a variety of high bandwidth, high performance memory system applications. All module components may be powered from a single 2.5V DC power supply and all inputs and outputs are SSTL_2 compatible.

FEATURES

- Part Identification

HDD32M64B8 – 10A : 100MHz (CL=2)

HDD32M64B8 – 13A : 133MHz (CL=2)

HDD32M64B8 – 13B : 133MHz (CL=2.5)

- 256MB(32Mx64) Unbuffered DDR SO-DIMM based on 32Mx8 DDR SDRSM
- 2.5V $\pm$ 0.2V VDD and VDDQ power supply
- Auto & self refresh capability (8192 Cycles/64ms)
- All input and output are compatible with SSTL_2 interface
- Data(DQ), Data strobes and write masks latched on the rising and falling edges of the clock
- All Addresses and control inputs except Data(DQ), Data strobes and Data masks latched on the rising edges of the clock
- MRS cycle with address key programs
 - Latency (Access from column address) : 2, 2.5
 - Burst length : 2, 4, 8
 - Data scramble : Sequential & Interleave
- Data(DQ), Data strobes and write masks latched on the rising and falling edges of the clock
- All Addresses and control inputs except Data(DQ), Data strobes and Data masks latched on the rising edges of the clock
- The used device is 8M x 8bit x 4Banks DDR SDRAM

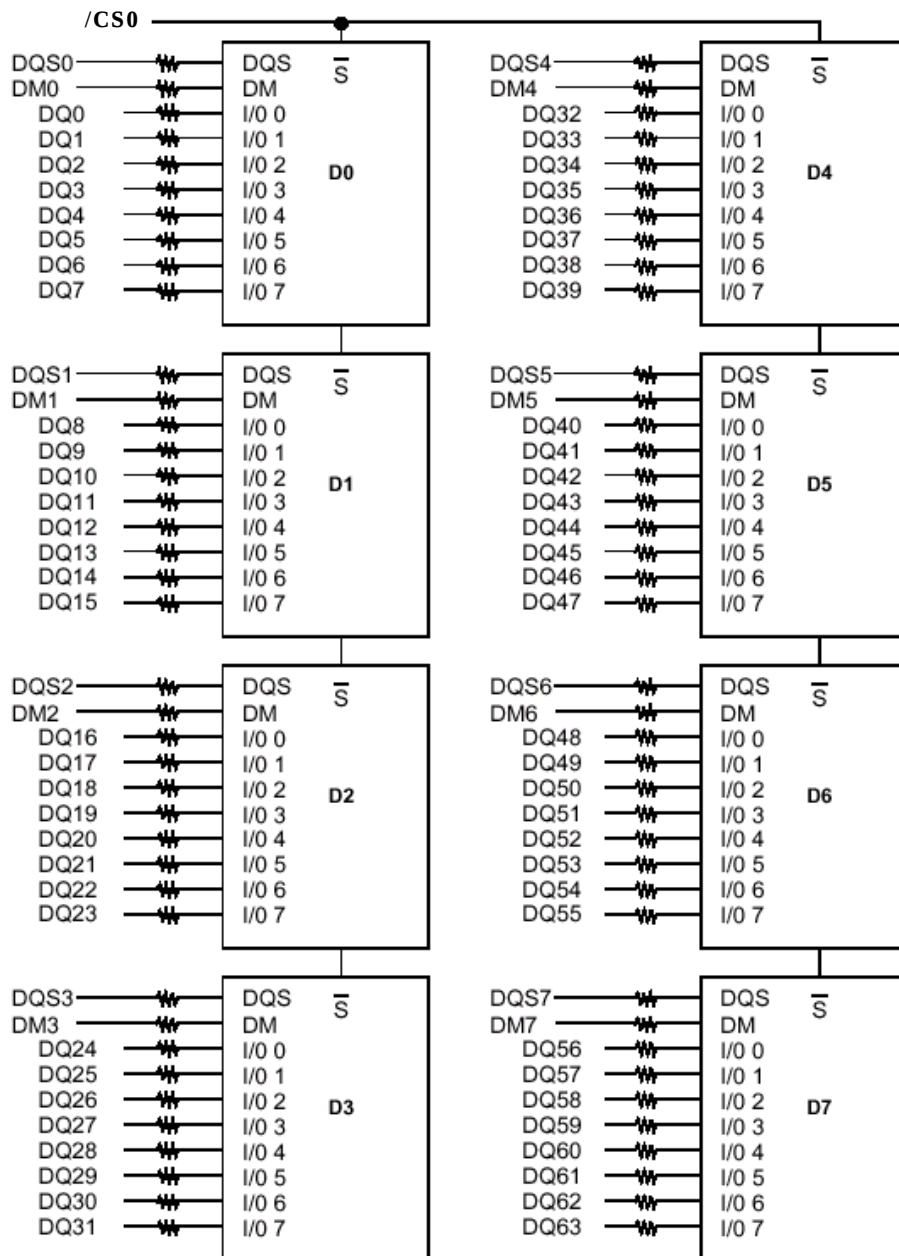
PIN ASSIGNMENT

PIN	Front	PIN	Back	PIN	Frontl	PIN	Back	PIN	Front	PIN	Back
1	VREF	2	VREF	67	DQ27	68	DQ31	133	DQS4	134	DM4
3	VSS	4	VSS	69	VDD	70	VDD	135	DQ34	136	DQ38
5	DQ0	6	DQ4	71	NC	72	NC	137	VSS	138	VSS
7	DQ1	8	DQ5	73	NC	74	NC	139	DQ35	140	DQ39
9	VDD	10	VDD	75	Vss	76	Vss	141	DQ40	142	DQ44
11	DQS0	12	DM0	77	NC	78	NC	143	VDD	144	VDD
13	DQ2	14	DQ6	79	NC	80	NC	145	DQ41	146	DQ45
15	VSS	16	VSS	81	VDD	82	VDD	147	DQS5	148	DM5
17	DQ3	18	DQ7	83	NC	84	NC	149	VSS	150	VSS
19	DQ8	20	DQ12	85	NC	86	NC(/RESET)	151	DQ42	152	DQ46
21	VDD	22	VDD	87	VSS	88	VSS	153	DQ43	154	DQ47
23	DQ9	24	DQ13	89	CK2	90	VSS	155	VDD	156	VDD
25	DQS1	26	DM1	91	/CK2	92	VDD	157	VDD	158	/CK1
27	VSS	28	VSS	93	VDD	94	VDD	159	VSS	160	CK1
29	DQ10	30	DQ14	95	CKE1	96	CKE0	161	VSS	162	VSS
31	DQ11	32	DQ15	97	NC(A13)	98	NC (BA2)	163	DQ48	164	DQ52
33	VDD	34	VDD	99	A12	100	A11	165	DQ49	166	DQ53
35	CK0	36	VDD	101	A9	102	A8	167	VDD	168	VDD
37	/CK0	38	VSS	103	VSS	104	VSS	169	DQS6	170	DM6
39	VSS	40	VSS	105	A7	106	A6	171	DQ50	172	DQ54
41	DQ16	42	DQ20	107	A5	108	A4	173	VSS	174	VSS
43	DQ17	44	DQ21	109	A3	110	A2	175	DQ51	176	DQ55
45	VDD	46	VDD	111	A1	112	A0	177	DQ56	178	DQ60
47	DQS2	48	DM2	113	VDD	114	VDD	179	VDD	180	VDD
49	DQ18	50	DQ22	115	A10/AP	116	BA1	181	DQ57	182	DQ61
51	VSS	52	VSS	117	BA0	118	/RAS	183	DQS7	184	DM7
53	DQ19	54	DQ23	119	/WE	120	/CAS	185	VSS	186	VSS
55	DQ24	56	DQ28	121	/CS0	122	NC	187	DQ58	188	DQ62
57	VDD	58	VDD	123	NC	124	NC	189	DQ59	190	DQ63
59	DQ25	60	DQ29	125	VSS	126	VSS	191	VDD	192	VDD
61	DQS3	62	DM3	127	DQ32	128	DQ36	193	*SDA	194	*SA0
63	VSS	64	VSS	129	DQ33	130	DQ37	195	*SCL	196	*SA1
65	DQ26	66	DQ30	131	VDD	132	VDD	197	*VSPD	198	*SA2
								199	VDDID	200	NC

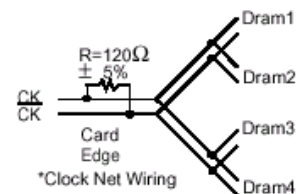
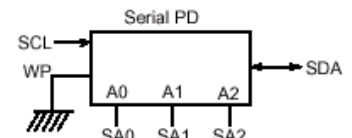
*These pins should be NC in the system which does not support SPD

PIN	PIN DESCRIPTION	PIN	PIN DESCRIPTION
A0~A12	Address input	VDD	Power supply(2.5V)
BA0~BA1	Bank Select Address	VDDQ	Power supply for DQs(2.5V)
DQ0~DQ63	Data input/output	VREF	Power supply for reference
DQS0~DQS7	Data Strobe input/output	VSPD	Serial EEPROM Power supply(3.3)
DM0~DM7	Data-in Mask	VSS	Ground
CK0~CK2,/CK0~/CK2	Clock input	SA0~SA2	Address in EEPROM
CKE0~CKE1	Clock enable input	SDA	Serial data I/O
/CS0	Chip Select input	SCL	Serial clock
/RAS, /CAS	Row / Column Address strobe	WP	Write protection
NC	No connection	VDDID	VDD identification flag

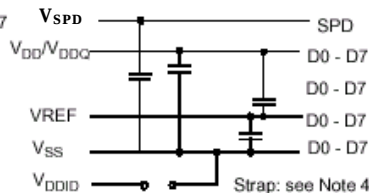
FUNCTIONAL BLOCK DIAGRAM



Clock Wiring	
Clock Input	SDRAMs
CK0/CK0	4 SDRAMs
CK1/CK1	4 SDRAMs
CK2/CK2	NC



BA0 - BA1 → BA0-BA1: DDR SDRAMs D0 - D7
A0 - A12 → A0- A11: DDR SDRAMs D0 - D7
RAS → RAS: SDRAMs D0 - D7
CAS → CAS: SDRAMs D0 - D7
CKE0 → CKE: SDRAMs D0 - D7
WE → WE: SDRAMs D0 - D7



Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/CS relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms.
4. VDDID strap connections (for memory device VDD, VDDQ):
STRAP OUT (OPEN): VDD = VDDQ
STRAP IN (VSS): VDD ≠ VDDQ.

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CK, /CK	Clock	CK and CK are differential clock inputs. All address and control input signals are sam-pled on the positive edge of CK and negative edge of CK. Output (read) data is referenced to both edges of CK. Internal clock signals are derived from CK/CK.
CKE	Clock Enable	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN(row ACTIVE in any bank). CKE is synchronous for all functions except for disabling outputs, which is achieved asynchronously. Input buffers, excluding CK, CK and CKE are disabled during power-down and self refresh modes, providing low standby power. CKE will recognizean LVCMOS LOW level prior to VREF being stable on power-up.
/CS	Chip Select	CS enables(registered LOW) and disables(registered HIGH) the command decoder. All commands are masked when CS is registered HIGH. CS provides for external bank selection on systems with multiple banks. CS is considered part of the command code.
A0 ~ A12	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : CA0 ~ CA9
BA0 ~ BA1	Bank select address	BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRE-CHARGE command is being applied.
/RAS	Row address strobe	Latches row addresses on the positive going edge of the CLK with /RAS low. Enables row access & precharge.
/CAS	Column address strobe	Latches column addresses on the positive going edge of the CLK with /CAS low. Enables column access.
/WE	Write enable	Enables write operation and row precharge. Latches data in starting from /CAS, /WE active.
DQS0 ~ 7	Data Strobe	Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data.
DM0~7	Input Data Mask	DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. DM pins include dummy loading internally, to matches the DQ and DQS load-ing.
DQ0 ~ 63	Data input/output	Data inputs/outputs are multiplexed on the same pins.
VDDQ	Supply	DQ Power Supply : +2.5V $\pm$ 0.2V.
VDD	Supply	Power Supply : +2.5V $\pm$ 0.2V (device specific).
VSS	Supply	DQ Ground.
VREF	Supply	SSTL_2 reference voltage.
VSPD	Supply	Serial EEPROM Power Supply : 3.3v
VDDID		VDD identification Flag

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNTE
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}	-1.0 ~ 3.6	V
Voltage on V_{DDQ} supply relative to Vss	V_{DDQ}	-0.5 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	8.0	W
Short circuit current	I_{OS}	50	mA

Notes: Operation at above absolute maximum rating can adversely affect device reliability

DC OPERATING CONDITIONS

(Recommended operating conditions (Voltage referenced to Vss = 0V, $T_A = 0$ to 70°C))

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTE
Supply Voltage	V_{DD}	2.3	2.7	V	
I/O Supply Voltage	V_{DDQ}	2.3	2.7	V	
I/O Reference Voltage	V_{REF}	$V_{DDQ}/2-50mV$	$V_{DDQ}/2+50mV$	V	1
I/O Termination Voltage(system)	V_{TT}	$V_{REF} - 0.04$	$V_{REF} + 0.04$	V	2
Input High Voltage	$V_{IH}(DC)$	$V_{REF} + 0.15$	$V_{REF} + 0.3$	V	
Input Low Voltage	$V_{IL}(DC)$	-0.3	$V_{REF} - 0.15$	V	
Input Voltage Level, CK and /CK inputs	$V_{IN}(DC)$	-0.3	$V_{DDQ} + 0.3$	V	
Input Differential Voltage, CK and /CK inputs	$V_{ID}(DC)$	0.3	$V_{DDQ} + 0.6$	V	
Input leakage current	I_{LI}	-2	2	uA	3
Output leakage current	I_{OZ}	-5	5	uA	
Output High current ($V_{OUT} = 1.95V$)	I_{OH}	-16.8		mA	
Output Low current ($V_{OUT} = 0.35V$)	I_{OL}	16.8		mA	

Notes :

- Typically, the value of V_{REF} is expected to be about 0.5* V_{DD} of the transmitting device.
 V_{REF} is expected to track variation in V_{DDQ} .
- Peak to peak AC noise on V_{REF} may not exceed 2% $V_{REF}(DC)$.
- V_{TT} of the transmitting device must track V_{REF} of the receiving device.

CAPACITANCE ($V_{DD} = \text{min to max}$, $V_{DDQ} = 2.5V$ to 2.7V, $T_A = 25^\circ C$, $f = 100MHz$)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Input capacitance(A0~A12, BA0~BA1, /RAS, /CAS,/WE)	C_{IN1}	36	44	pF
Input capacitance(CKE0,CKE1)	C_{IN2}	36	44	pF
Input capacitance(/CS0)	C_{IN3}	34	42	pF
Input capacitance(CK0~CK2, /CK0~/CK2)	C_{IN4}	34	38	pF
Input capacitance(DM0~DM7)	C_{IN5}	8	9	pF
Data input/output capacitance (DQ0 ~ DQ63, DQS0~DQS7)	C_{OUT1}	8	9	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, $V_{DD} = 2.5V$, $T = 25^{\circ}C$)

PARAMETER	SYMBOL	TEST CONDITION	VERSION			UNIT	NOTE
			-10A	-13A	-13B		
Operating current (One bank active)	I_{DD1}	Burst length = 2 $t_{RC} \geq t_{RC(min)}$, $CL=2.5$ $I_{OUT} = 0mA$, Active-Read-Presharge	800	960	960	mA	
Precharge standby current in power-down mode	I_{DD2P}	$CKE \leq V_{IL(max)}$ $t_{CK} = t_{CK(min)}$, All banks idle	160	200	200	mA	
Precharge standby current in non power-down mode	I_{DD2N}	$CKE \geq V_{IH(min)}$ $/CS \geq V_{IH(min)}$, $t_{CK} = t_{CK(min)}$	280	320	320	mA	
Active standby current in power-down mode	I_{DD3P}	All banks idle, $CKE \leq V_{IL(max)}$, $t_{CK} = t_{CK(min)}$	280	320	320	mA	
Active standby current in non power-down mode (One bank active)	I_{DD3N}	One bank, Active-Read-Presharge, $t_{RC} = t_{RAS(max)}$, $t_{CK} = t_{CK(min)}$	360	440	440	mA	
Operating current (Read)	I_{DD4R}	Burst length = 2 $t_{RC} = t_{RC(min)}$, $I_{OUT} = 0mA$, $CL=2$	1200	1440	1440	mA	
Operating current (Write)	I_{DD4W}	Burst length = 2 $t_{RC} = t_{RC(min)}$, $CL=2$	1520	1920	1920	mA	
Auto refresh current	I_{DD5}	$t_{RC} \geq t_{REF(min)}$	1200	1440	1440	mA	
Self refresh current	Normal	I_{DD6} $CKE \leq 0.2V$	24	24	24	mA	
	Low Power		12	12	12	mA	

Notes: Operation at above absolute maximum rating can adversely affect device reliability

AC OPERATING CONDITIONS

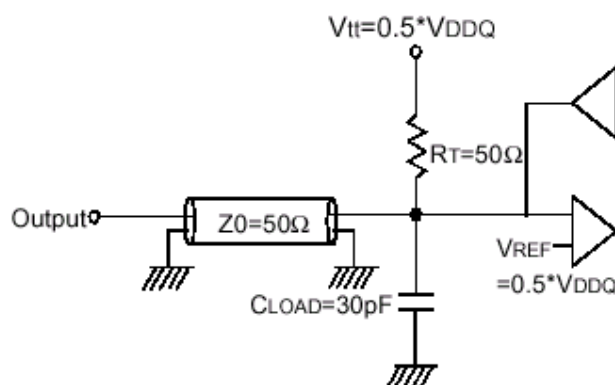
PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTE
Input High (Logic 1) Voltage, DQ, DQS and DM signals	$V_{IH(AC)}$	$V_{REF} + 0.35$			
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	$V_{IL(AC)}$		$V_{REF} - 0.31$	V	
Input Differential Voltage, CK and CK inputs	$V_{ID(AC)}$	0.7	$V_{DDQ} + 0.6$	V	1
Input Crossing Point Voltage, CK and CK inputs	$V_{IX(AC)}$	$0.5 * V_{DDQ} - 0.2$	$0.5 * V_{DDQ} + 0.2$	V	2

Notes:

1. V_{ID} is the magnitude of the difference between the input level on CK and the input on CK.
2. The value of V_{IX} is expected to equal $0.5 * V_{DDQ}$ of the transmitting device and must track variations in the DC level of the same

AC OPERATING TEST CONDITIONS

PARAMETER	VALUE	UNIT	NOTE
Input reference voltage for Clock	$0.5 * V_{DDQ}$	V	
Input signal maximum peak swing	1.5	V	
Input signal minimum slew rate	$V_{REF}+0.31/V_{REF}-0.31$	V	
Input Levels(V_{IH}/V_{IL})	$V_{REF}+0.35/V_{REF}$	V	
Input timing measurement reference level	V_{REF}	V	
Output timing measurement reference level	V_{TT}	V	
Output load condition	See Load Circuit	V	



(Fig. 1) Output Load Circuit (SSTL_2)

AC CHARACTERISTICS (These AC characteristics were tested on the Component)

PARAMETER		SYMBOL	DDR200		DDR266A		DDR266B		UNIT	NOTE
			-10A		-13A		-13B			
			MIN	MAX	MIN	MAX	MIN	MAX		
Row cycle time		t _{RC}	70		65		65		ns	1
Refresh row cycle time		t _{RFC}	80		75		75		ns	1,2
Row active time		t _{RAS}	48	120K	45	120K	45	120K	ns	1,2
/RAS to /CAS delay		t _{RCD}	20		20		20		ns	3
Row precharge time		t _{RP}	20		20		20		ns	3
Row active to Row active delay		t _{RRD}	15		15		15		ns	3
Write recovery time		t _{WR}	2		2		2		t _{CK}	3
Last data in to Read command		t _{CDLR}	1		1		1		t _{CK}	2
Col. address to Col. address delay		t _{CCD}	1		1		1		t _{CK}	
Clock cycle time	CL=2.0	t _{CK}	10	12	7.5	12	10	12	ns	
	CL=2.5			12	7.5	12	7.5	12	ns	
Clock high level width		t _{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t _{CK}	

Clock low level width	t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
DQS-out access time from CK/CK	t_{DQSK}	-0.8	+0.8	-0.75	+0.75	-0.75	+0.75	ns	
Output data access time from CK/CK	t_{AC}	-0.8	+0.8	-0.75	+0.75	-0.75	+0.75	ns	
Data strobe edge to output data edge	t_{DQSQ}	-	+0.6	-	+0.5	-	+0.5	ns	
Read Preamble	t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	
Read Postamble	t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	
Data out high impedance time from CK-/CK	t_{HZQ}	-0.8	+0.8	-0.75	+0.75	-0.75	+0.75	ns	2
CK to valid DQS-in	t_{DQSS}	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
DQS-in setup time	t_{WPRES}	0		0		0		ns	3
DQS-in hold time	t_{WPREH}	0.25		0.25		0.25		t_{CK}	
DQS-in falling edge to CK rising-setup time	t_{DSS}	0.2		0.2		0.2		t_{CK}	
DQS-in falling edge to CK rising hold time	t_{DSH}	0.2		0.2		0.2		t_{CK}	
DQS-in high level width	t_{DQSH}	0.35		0.35		0.35		t_{CK}	
DQS-in low level width	t_{DQSL}	0.35		0.35		0.35		t_{CK}	
DQS-in cycle time	t_{DSC}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	
Address and Control Input setup time	t_{IS}	1.1		0.9		0.9		ns	
Address and Control Input hold time	t_{IH}	1.1		0.9		0.9		ns	
Mode register set cycle time	t_{MRD}	16		15		15		ns	
DQ & DM setup time to DQS	t_{DS}	0.6		0.5		0.5		ns	
DQ & DM hold time to DQS	t_{DH}	0.6		0.5		0.5		ns	
DQ & DM input pulse width	t_{DIPW}	2		1.75		1.75		ns	
Power down exit time	t_{PDEX}	10		10		10		ns	
Exit self refresh to write command	t_{XSW}	116		95				ns	
Exit self refresh to bank active command	t_{XSA}	80		75		75		ns	
Exit self refresh to read command	t_{XSR}	200		200		200		Cycle	
Refresh interval time	T_{REF}	15.6		15.6		15.6		us	1
Output DQS valid window	T_{QH}	t_{HPmin} $-t_{QHS}$		t_{HPmin} $-t_{QHS}$		t_{HPmin} $-t_{QHS}$		t_{CK}	
DQS write postamble time	T_{WPST}	0.25		0.25		0.25		t_{CK}	4

Notes :

1. Maximum burst refresh of 8.
2. t_{HZQ} transitions occurs in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving.

- The specific requirement is that DQS be valid(High-Low) on or before this CK edge. The case shown(DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on t_{DQSS} .
- The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.

SIMPLIFIED TRUTH TABLE

COMMAND			CK E n-1	CK E n	/CS	/R A S	/C A S	/WE	DM	BA 0,1	A10/ AP	A11 A9~A0	NOTE
Register	Extended MRS		H	X	L	L	L	L	X	OP code			1,2
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column Address (A0 ~A9)	4
	Auto precharge eable										H		4
Write & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column Address (A0 ~ A9)	4
	Auto precharge enable							L			H		4,6
Burst Stop			H	X	L	H	H	L	X	X			7
Precharg e	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		5
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X	X			
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DM			H	X					V	X		8	
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes :

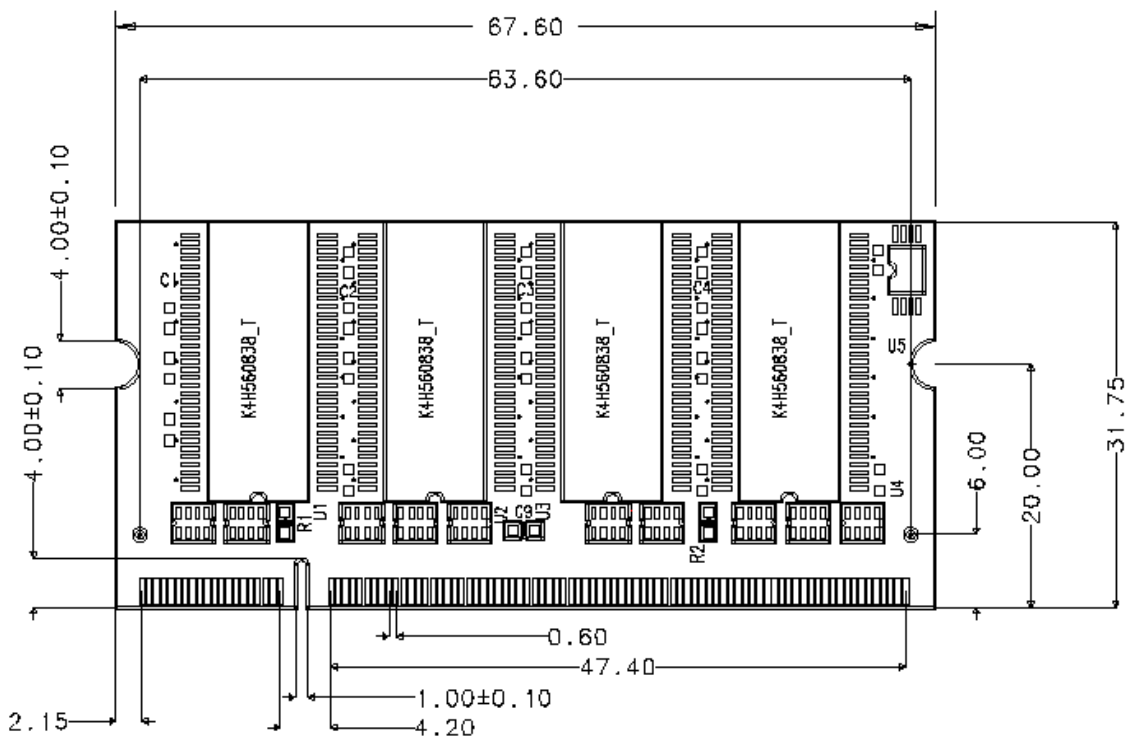
- OP Code : Operand code
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)
- MRS can be issued only at all banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.
- Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.
 If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
 If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
 If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
 If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
 If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
 Another bank read/write command can be issued after the end of burst.
 New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges
 (Write DM latency is 0)

PACKAGING INFORMATION

Unit : mm

Front -Side



ORDERING INFORMATION

Part Number	Density	Org.	Package	Ref.	Vcc	MODE	MAX.frq
HDD32M64B8-10A	256MByte	32M x 64	200PIN SO-DIMM	8K	2.5V	DDR	100MHz/CL2
HDD32M64B8-13A	256MByte	32M x 64	200PIN SO-DIMM	8K	2.5V	DDR	133MHz/CL2
HDD32M64B8-13B	256MByte	32M x 64	200PIN SO-DIMM	8K	2.5V	DDR	133MHz/CL2.5