

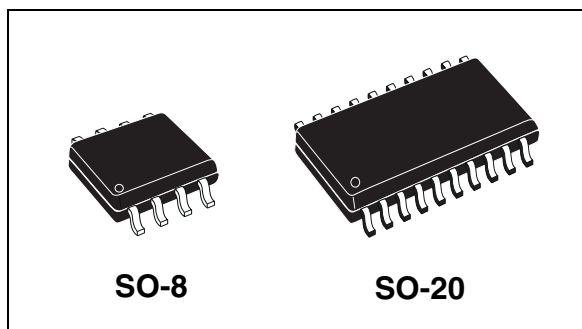
## Low drop voltage regulator

### Features

|                              |              |                  |
|------------------------------|--------------|------------------|
| Max DC supply voltage        | $V_S$        | 40V              |
| Max output voltage tolerance | $\Delta V_0$ | +/-2%            |
| Max dropout voltage          | $V_{dp}$     | 400 mV           |
| Output current               | $I_O$        | 150 mA           |
| Quiescent current            | $I_{qn}$     | 79 $\mu A^{(1)}$ |

1. Typical value with watchdog disabled.

- Operating DC supply voltage range 5.6V to 31V
- Reset circuit sensing the output voltage down to 1V
- Programmable reset pulse delay with external capacitor
- Watchdog
- Programmable watchdog timer with external capacitor
- Enable input for enabling/disabling the watchdog functionality
- Thermal shutdown and short circuit protection
- Wide temperature range ( $T_j = -40^{\circ}C$  to  $150^{\circ}C$ )



### Description

The L4993 is a monolithic integrated 5V Voltage regulator with a low drop voltage at currents up to 150mA. The output voltage regulating element consists in a p-channel MOS and the regulation is performed regardless of input voltage transients up to 40V. The high precision of the output voltage is obtained with a pre-trimmed reference voltage. The L4993 is protected against short circuit and an over-temperature protection switches off the device in case of extremely high power dissipation. The L4993 watchdog is active when the Enable is high. State of the art features like reset and watchdog make this device particularly suitable to supply microprocessor systems in automotive applications.

**Table 1. Device summary**

| Package        | Order codes |             |
|----------------|-------------|-------------|
|                | Tube        | Tape & reel |
| SO-8           | L4993D      | L4993DTR    |
| SO-20 (16+2+2) | L4993MD     | L4993MDTR   |

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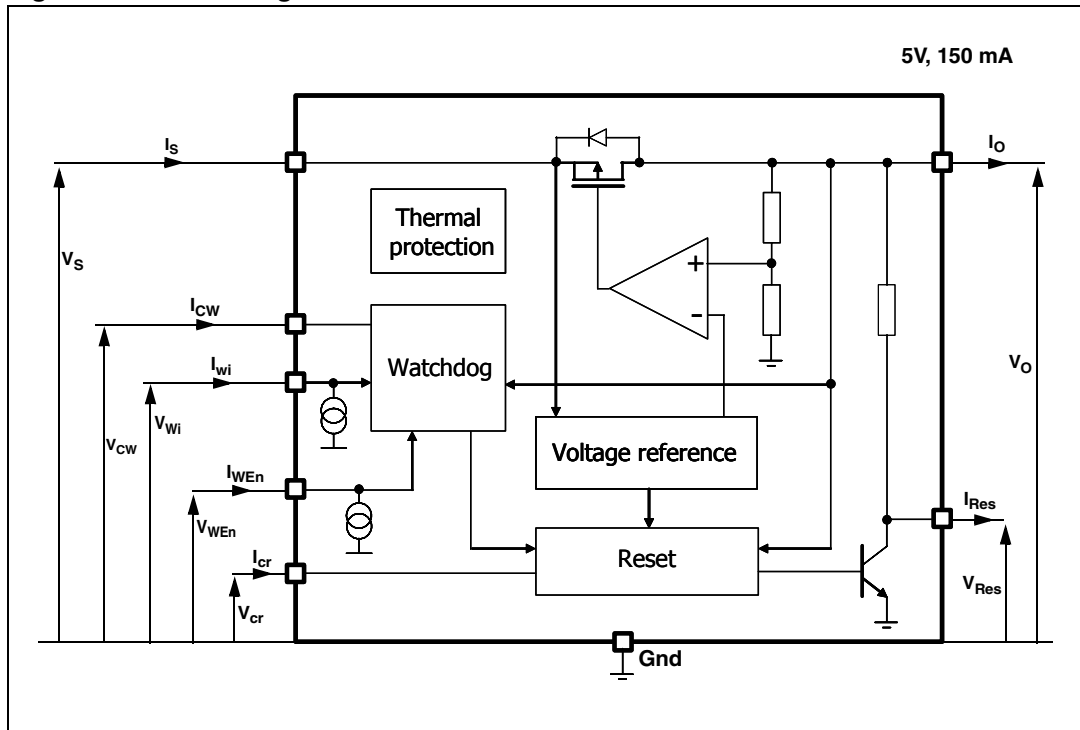
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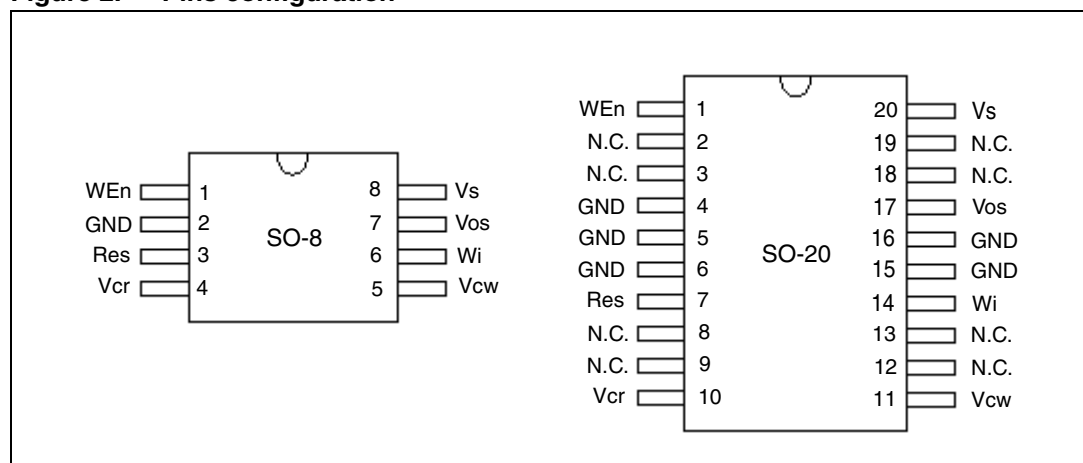
# 1 Block diagram and pins description

Figure 1. Block diagram



**Table 2. Pins description**

| Pin name  | SO-8 (D) | SO-20 (MD)                 | Function                                                                                                                                       |
|-----------|----------|----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------|
| WEn       | 1        | 1                          | Watchdog Enable input<br>If high watchdog functionality is active                                                                              |
| Gnd       | 2        | 4                          | Ground reference                                                                                                                               |
| Gnd       |          | 5, 6, 15, 16               | Ground<br>Connected these pins to a heat spreader ground                                                                                       |
| Res       | 3        | 7                          | Reset output.<br>It is pulled down when output voltage goes below $V_{o\_th}$ or frequency at $W_i$ is too low.<br>Leave floating if not used. |
| Vcr       | 4        | 10                         | Reset timing adjust.<br>A capacitor between Vcr pin and gnd, sets the reset delay time (trd)                                                   |
| Vcw       | 5        | 11                         | Watchdog timer adjust<br>A capacitor between Vcw pin and gnd, sets the time response of the watchdog monitor.                                  |
| Wi        | 6        | 14                         | Watchdog input.<br>If the frequency at this input pin is too low, the Reset output is activated.<br>Connect to ground if not used              |
| $V_{o_s}$ | 7        | 17                         | Voltage regulator output<br>Block to ground with a capacitor >100nF (needed for regulator stability)                                           |
| $V_s$     | 8        | 20                         | Supply voltage<br>Block to ground directly at IC pin with a capacitor                                                                          |
| N.C.      |          | 2, 3, 8, 9, 12, 13, 18, 19 | Not connected                                                                                                                                  |

**Figure 2. Pins configuration**

## 2 Electrical specifications

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 3. Absolute maximum ratings**

| Symbol     | Parameter                            | Value                  | Unit |
|------------|--------------------------------------|------------------------|------|
| $V_{VSDC}$ | DC supply voltage                    | -0.3 to 40             | V    |
| $I_{VSDC}$ | Input current                        | Internally limited     |      |
| $V_{VO}$   | DC output voltage                    | -0.3 to 6              | V    |
| $I_{VO}$   | DC output current                    | Internally limited     |      |
| $V_{Wi}$   | Watchdog input voltage               | -0.3 to $V_{VO} + 0.3$ | V    |
| $V_{Od}$   | Open drain output voltage            | -0.3 to $V_{VO} + 0.3$ | V    |
| $I_{Od}$   | Open drain output current            | Internally limited     |      |
| $V_{cr}$   | Reset delay voltage                  | -0.3 to $V_{VO} + 0.3$ | V    |
| $V_{cw}$   | Watchdog delay voltage               | -0.3 to $V_{VO} + 0.3$ | V    |
| $V_{WEi}$  | Watchdog Enable input voltage        | -0.3 to $V_{VO} + 0.3$ | V    |
| $T_j$      | Junction temperature                 | -40 to 150             | °C   |
| $V_{ESD}$  | ESD voltage level (HBM-MIL STD 883C) | ±2                     | kV   |
| $V_{ESD}$  | ESD voltage level (CDM AEC-Q100-011) | 750                    | V    |

*Note:* Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

### 2.2 Thermal data

For details, please refer to [Section 4.1: SO-8 thermal data](#) and [Section 4.2: SO-20 thermal data](#).

**Table 4. Thermal data<sup>(1)</sup>**

| Symbol        | Parameter                               | Value | Unit |
|---------------|-----------------------------------------|-------|------|
| $R_{th-jamb}$ | Thermal resistance Junction to Ambient: |       |      |
|               | SO-8                                    | 130   | °C/W |
|               | SO-20                                   | 51    | °C/W |

1. The values quoted are for PCB FR4 area= 58mm x 58mm, PCB thickness = 2mm, Cu thickness = 35µm , Copper areas: SO-8= 2 cm<sup>2</sup>, SO-20= 6 cm<sup>2</sup>.

## 2.3 Electrical characteristics

Values specified in this section are for  $V_s = 5.6\text{V}$  to  $31\text{V}$ ,  $T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$  unless otherwise stated.

**Table 5. General**

| Pin        | Symbol          | Parameter                                          | Test condition                                                          | Min. | Typ. | Max. | Unit             |
|------------|-----------------|----------------------------------------------------|-------------------------------------------------------------------------|------|------|------|------------------|
| Vo         | $V_{o\_ref}$    | Output voltage                                     | $V_s = 6$ to $31\text{V}$<br>$I_o = 1$ to $150\text{mA}$                | 4.9  | 5.0  | 5.1  | V                |
| Vo         | $I_{short}$     | Short circuit current                              | $V_s = 13.5\text{V}^{(1)}$                                              | 150  | 280  | 400  | mA               |
| Vo         | $I_{lim}^{(2)}$ | Output current limitation                          | $V_s = 13.5\text{V}^{(1)}$                                              | 150  | 320  | 500  | mA               |
| $V_s, V_o$ | $V_{line}$      | Line regulation voltage                            | $V_s = 6$ to $31\text{V}$<br>$I_o = 1$ to $150\text{mA}$                |      |      | 25   | mV               |
| Vo         | $V_{load}$      | Load regulation voltage                            | $I_o = 1$ to $150\text{mA}$                                             |      |      | 25   | mV               |
| $V_s, V_o$ | $V_{dp}^{(3)}$  | Drop voltage                                       | $I_o = 150\text{mA}$                                                    |      | 200  | 400  | mV               |
| $V_s, V_o$ | SVR             | Ripple rejection                                   | $f_r = 100\text{Hz}^{(4)}$                                              | 55   |      |      | dB               |
| $V_s, V_o$ | $I_{qn\_150}$   | Quiescent current                                  | $V_s = 13.5\text{V}$ ,<br>$I_o = 150\text{mA}$ ,<br>$WEn = \text{high}$ |      | 1.25 | 2    | mA               |
| $V_s, V_o$ | $I_{qn\_50}$    | Quiescent current                                  | $V_s = 13.5\text{V}$ ,<br>$I_o = 50\text{mA}$ ,<br>$WEn = \text{high}$  |      | 470  | 1000 | $\mu\text{A}$    |
| $V_s, V_o$ | $I_{qn\_1}$     | Quiescent current                                  | $V_s = 13.5\text{V}$ ,<br>$I_o < 1\text{mA}$ ,<br>$WEn = \text{high}$   |      | 100  | 180  | $\mu\text{A}$    |
| $V_s, V_o$ | $I_{qs}$        | Quiescent current with watchdog regulator disabled | $V_s = 13.5\text{V}$ ,<br>$I_o < 1\text{mA}$ ,<br>$WEn = \text{low}$    |      | 79   | 125  | $\mu\text{A}$    |
|            | $T_w$           | Thermal protection temperature                     |                                                                         | 150  |      | 190  | $^\circ\text{C}$ |
|            | $T_{w\_hy}$     | Thermal protection temperature hysteresis          |                                                                         |      | 10   |      | $^\circ\text{C}$ |

1. See [Figure 25](#).
2. Measured output current when the output voltage has dropped 100mV from its nominal value obtained at  $V_s = 13.5\text{V}$  and  $I_o = 75\text{mA}$ .
3.  $V_s - V_o$  measured when the output voltage has dropped 100mV from its nominal value obtained at  $V_s = 13.5\text{V}$  and  $I_o = 75\text{mA}$ .
4. Guaranteed by design.



**Table 6. Reset**

| Pin | Symbol       | Parameter                          | Test condition                                | Min. | Typ. | Max. | Unit               |
|-----|--------------|------------------------------------|-----------------------------------------------|------|------|------|--------------------|
| Res | Vres_l       | Reset output low voltage           | $R_{ext} = 5k\Omega$ to $V_o$ ,<br>$V_o > 1V$ |      |      | 0.4  | V                  |
| Res | $I_{Res\_h}$ | Reset output high leakage current  | $V_{Res} = 5V$                                |      |      | 1    | $\mu A$            |
| Res | R_p_u        | Pull up internal resistance        | With respect to $V_o$                         | 12   | 25   | 50   | $k\Omega$          |
| Res | $V_{o\_th}$  | $V_o$ out of regulation threshold  | $V_s = 6$ to $31V$ ,<br>$I_o = 1$ to $150mA$  | 6%   | 8%   | 10%  | Below $V_{o\_ref}$ |
| Vcr | Vrlth        | Reset delay circuit low threshold  | $V_s = 13.5V$                                 | 10%  | 13%  | 16%  | $V_{o\_ref}$       |
| Vcr | Vrhth        | Reset delay circuit high threshold | $V_s = 13.5V$                                 | 44%  | 47%  | 50%  | $V_{o\_ref}$       |
| Vcr | Icr          | Charge current                     | $V_s = 13.5V$                                 | 8    | 17.6 | 30   | $\mu A$            |
| Vcr | Idr          | Discharge current                  | $V_s = 13.5V$                                 | 8    | 17.6 | 30   | $\mu A$            |
| Res | Trr_2        | Reset reaction time <sup>(1)</sup> | $V_o = V_{o\_th} - 100mV$                     | 100  | 275  | 1000 | $\mu s$            |
| Res | Trd          | Reset delay time                   | $V_s = 13.5V$ ,<br>$C_{tr} = 1nF$             | 65   |      | 150  | ms                 |

1. When  $V_o$  becomes lower than 4V, the reset reaction time decreases down to 2 $\mu s$  assuring a faster reset condition in this particular case.

**Table 7. Watchdog**

| Pin | Symbol   | Parameter          | Test condition                     | Min. | Typ. | Max. | Unit         |
|-----|----------|--------------------|------------------------------------|------|------|------|--------------|
| Wi  | Vih      | Input high voltage | $V_s = 13.5V$                      | 3.5  |      |      | V            |
| Wi  | Vil      | Input low voltage  | $V_s = 13.5V$                      |      |      | 1.5  | V            |
| Wi  | Vih_hyst | Input hysteresis   | $V_s = 13.5V$                      |      | 500  |      | mV           |
| Wi  | li       | Pull down current  | $V_s = 13.5V$                      |      | 10   | 20   | $\mu A$      |
| Vcw | Vwhth    | High threshold     | $V_s = 13.5V$                      | 44%  | 47%  | 50%  | $V_{o\_ref}$ |
| Vcw | Vwlth    | Low threshold      | $V_s = 13.5V$                      | 10%  | 13%  | 16%  | $V_{o\_ref}$ |
| Vcw | Icwc     | Charge current     | $V_s = 13.5V$ ,<br>$V_{cw} = 0.1V$ | 4    | 8    | 14   | $\mu A$      |

**Table 7. Watchdog (continued)**

| Pin | Symbol | Parameter                | Test condition            | Min. | Typ. | Max. | Unit |
|-----|--------|--------------------------|---------------------------|------|------|------|------|
| Vcw | Icwd   | Discharge current        | Vs = 13.5V,<br>Vcw = 2.5V | 1.0  | 2.13 | 4.5  | μA   |
| Vcw | Twop   | Watchdog period          | Vs = 13.5V,<br>Ctw = 47nF | 25   | 50   | 90   | ms   |
| Res | twol   | Watchdog output low time | Vs = 13.5V,<br>Ctw = 47nF | 6    | 10.5 | 22   | ms   |

**Table 8. Watchdog Enable**

| Pin | Symbol               | Parameter                 | Test condition | Min. | Typ. | Max. | Unit |
|-----|----------------------|---------------------------|----------------|------|------|------|------|
| WEn | W <sub>En_low</sub>  | Enable input low voltage  |                |      |      | 1    | V    |
| WEn | W <sub>En_high</sub> | Enable input high voltage |                | 3    |      |      | V    |
| WEn | W <sub>En_hyst</sub> | Enable input hysteresis   |                | 500  | 800  | 1100 | mV   |
| WEn | I <sub>leak</sub>    | Pull down current         | WEn = 5V       | 2    | 8    | 20   | μA   |

## 2.4 Electrical characteristics curves

Figure 3. Output voltage vs.  $T_j$

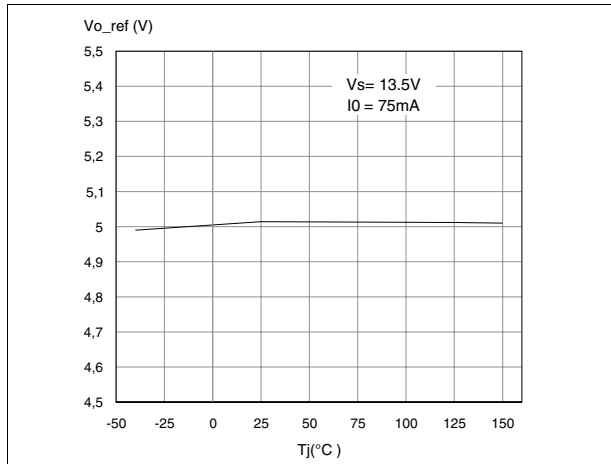


Figure 4. Output voltage vs.  $V_s$

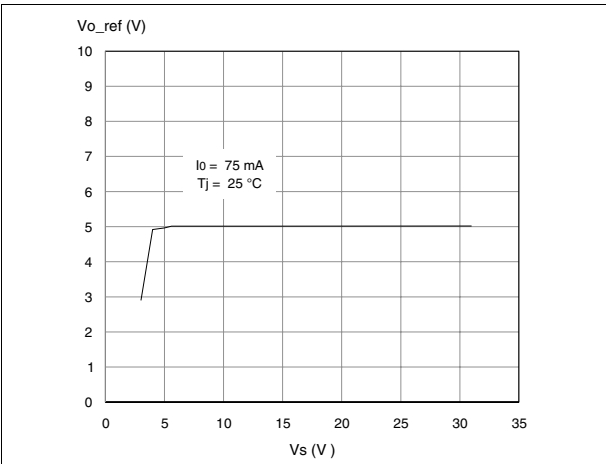


Figure 5. Drop Voltage vs. Output Current

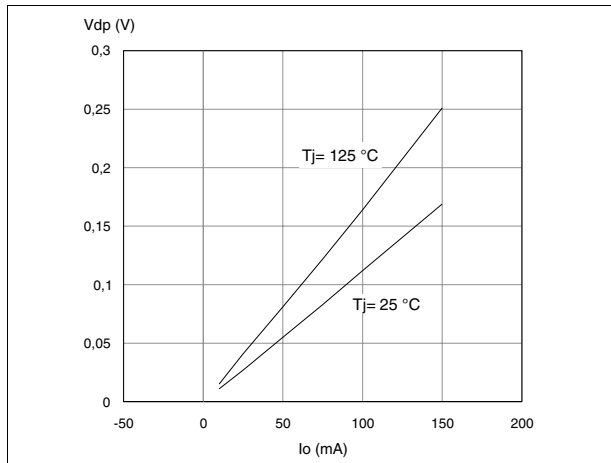


Figure 6. Current consumption vs. Output Current

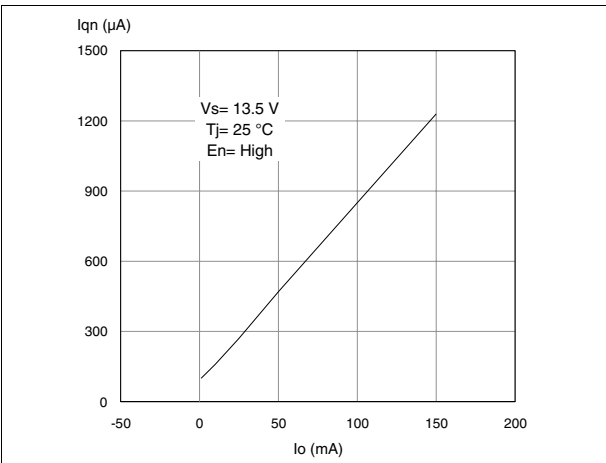


Figure 7. Current consumption vs. Input Voltage

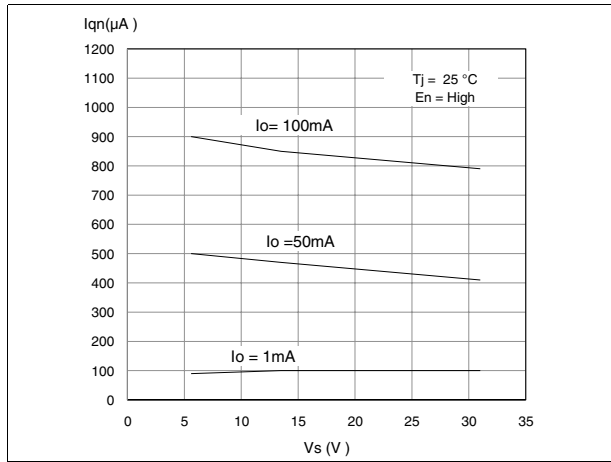


Figure 8. Current limitation vs.  $T_j$

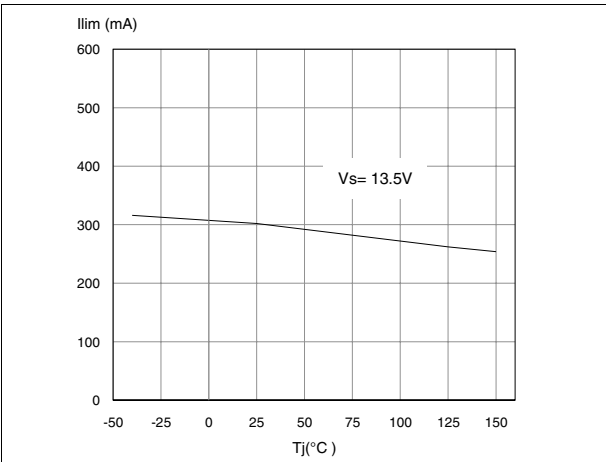


Figure 9. Current limitation vs. Input Voltage      Figure 10. Short Circuit Current vs. Tj

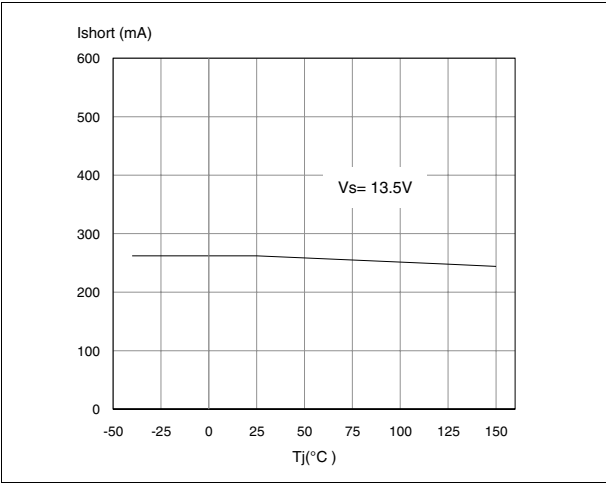
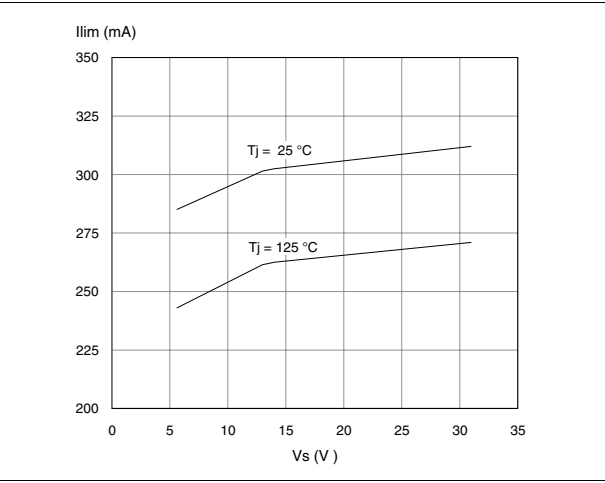


Figure 11. Short Circuit Current vs. Input Voltage

Figure 12. V<sub>WEn\_high</sub> vs. Tj

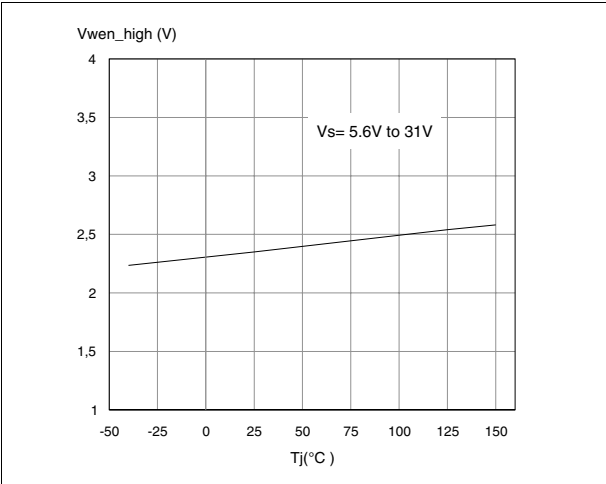
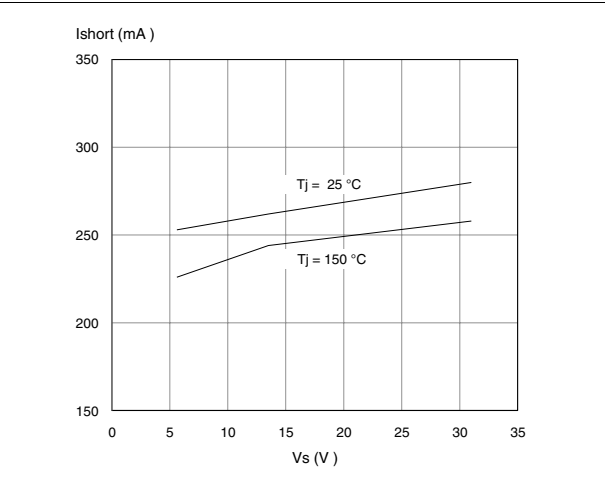


Figure 13. V<sub>WEN\_LOW</sub> vs. Tj

Figure 14. V<sub>rhth</sub> vs. Tj

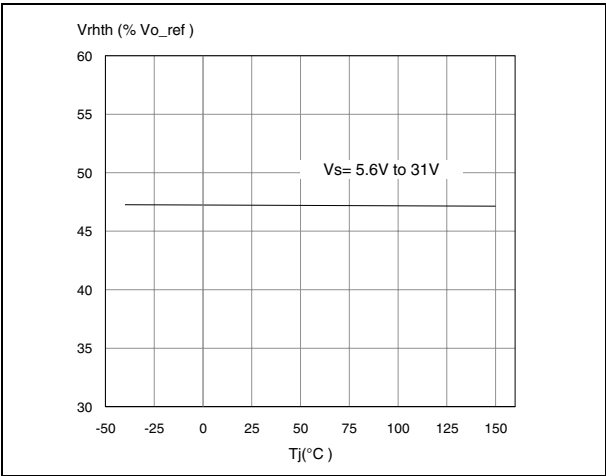
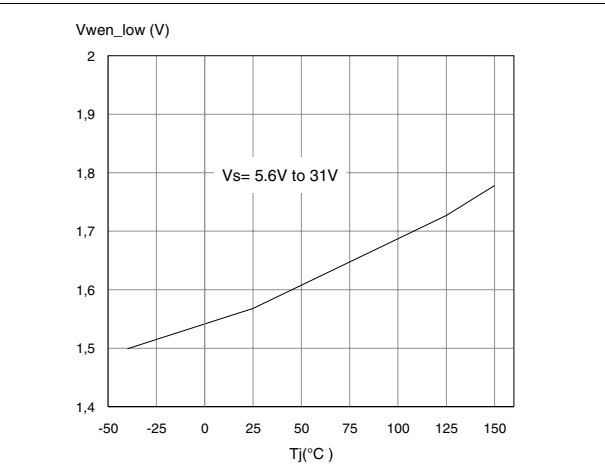


Figure 15.  $V_{rlth}$  vs.  $T_j$

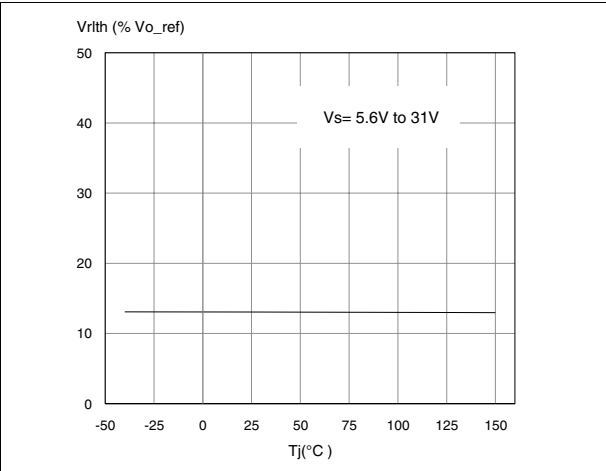


Figure 16.  $V_{whth}$  vs.  $T_j$

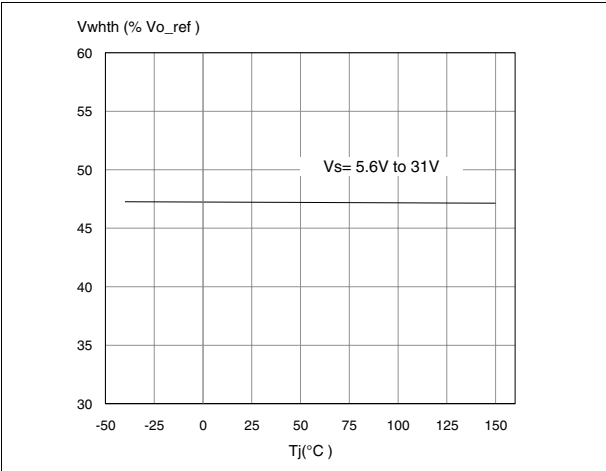


Figure 17.  $V_{wlth}$  vs.  $T_j$

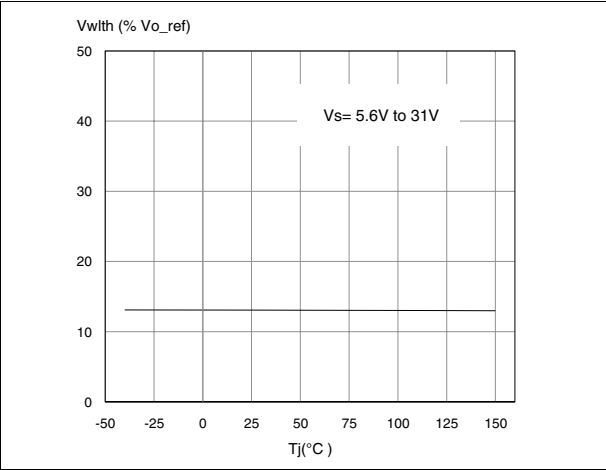


Figure 18.  $I_{cr}$  &  $I_{cwc}$  vs.  $T_j$

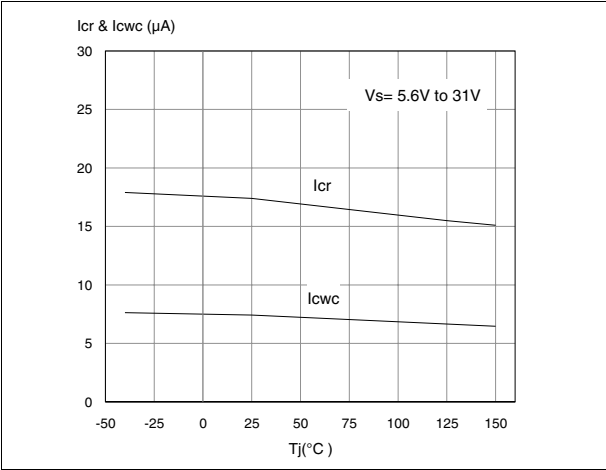


Figure 19.  $I_{dr}$  &  $I_{cwd}$  vs.  $T_j$

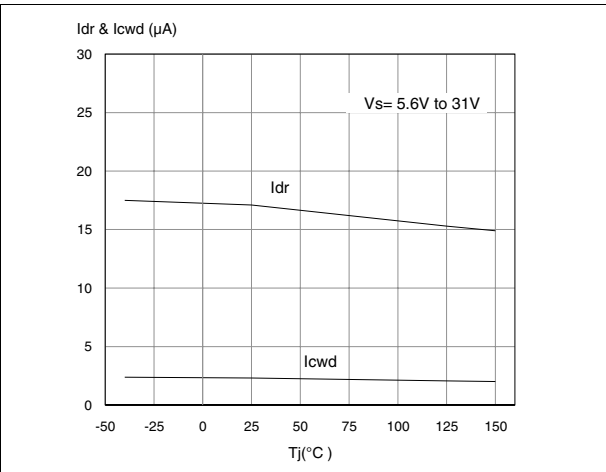


Figure 20.  $T_{wop}$  vs.  $T_j$

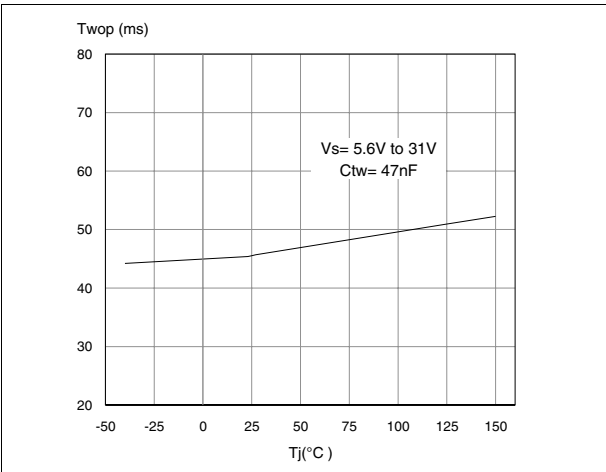
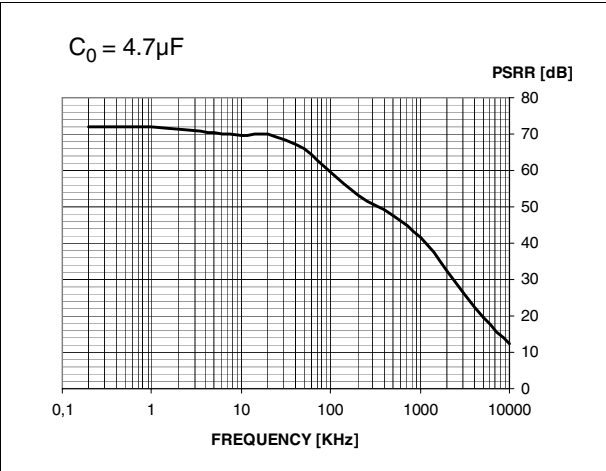


Figure 21. PSRR



## 2.5 Test circuit and waveforms plot

### 2.5.1 Load regulation

Figure 22. Load regulation test circuit

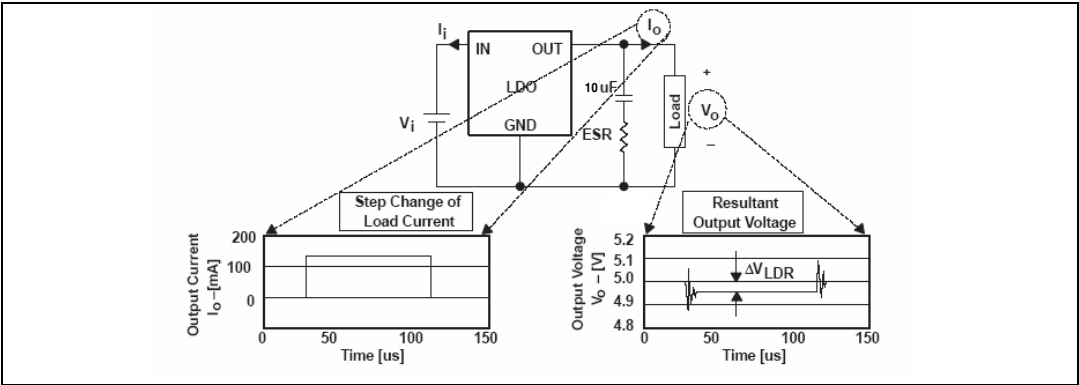
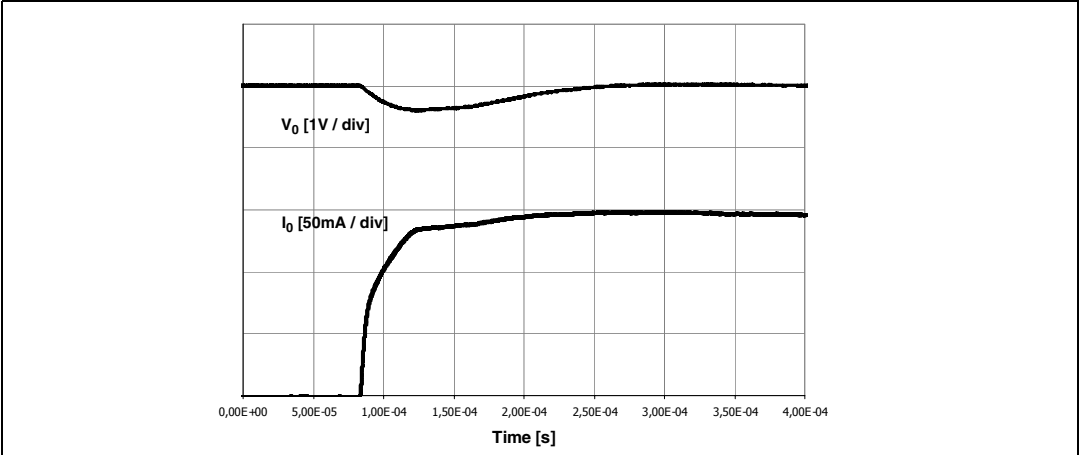
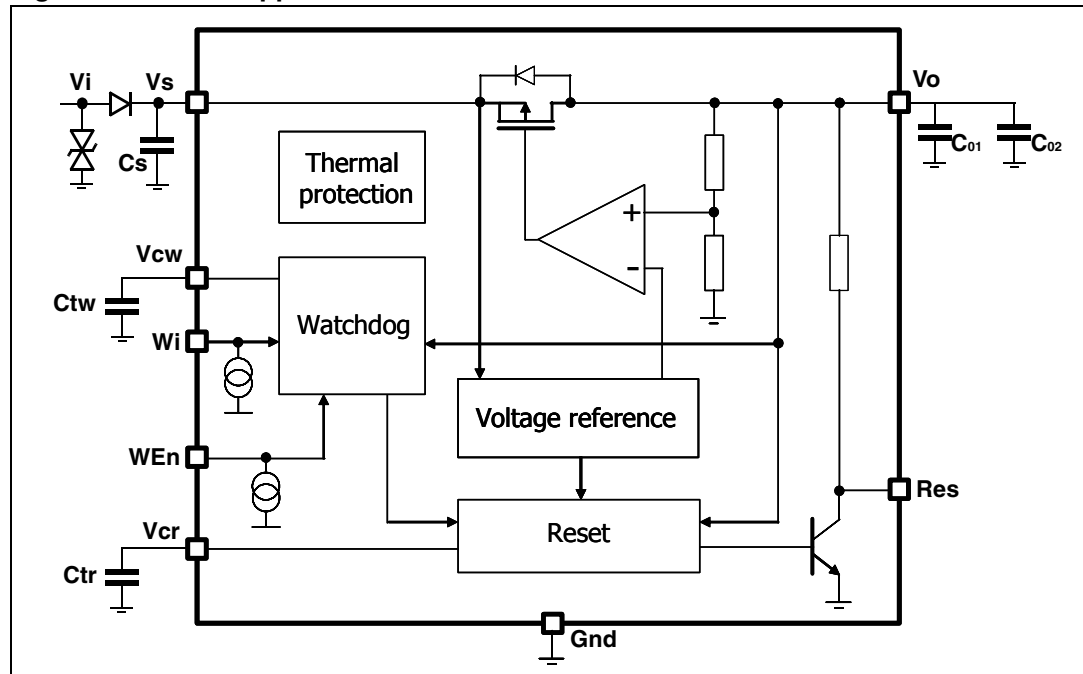


Figure 23. Maximum load variation response



### 3 Application information

Figure 24. L4993 application schematic

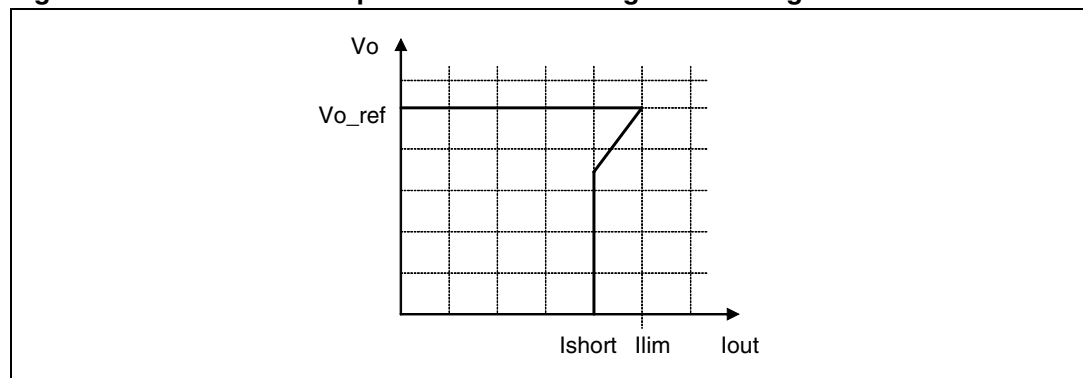


**Note:** The input capacitor  $C_s > 200\text{nF}$  is necessary for the smoothing of line disturbances. The output capacitor  $C_{01} > 100\text{nF}$  is necessary for the stability of the regulation loop. In order to damp output voltage oscillations during high load current surges, it is recommended put an additional electrolytic capacitor  $C_{02} > 10\mu\text{F}$  at the output pin.

#### 3.1 Voltage regulator

Voltage regulator uses a p-channel transistor as a regulating element. With this structure, very low dropout voltage at current up to 500mA is obtained. The output voltage is regulated up to transient input supply voltage of 40V. No functional interruption due to over-voltage pulses is generated. A short circuit protection to GND is provided. The voltage regulator watchdog functionality can be disabled by putting WEn low.

Figure 25. Behavior of output current versus regulated voltage  $V_o$



## 3.2 Reset

The reset circuit supervises the output voltage  $V_o$ . The  $V_{o\_th}$  reset threshold is defined with the in-ternal reference voltage and a resistor output divider. If the output voltage becomes lower than  $V_{o\_th}$  then Res goes low with a reaction time  $t_{rr}$ . The reset low signal is guaranteed for an output voltage  $V_o$  greater than 1V.

When the output voltage becomes higher than  $V_{o\_th}$  then Res goes high with a delay  $t_{rd}$ . This delay is obtained by an internal oscillator.

The oscillator period is given by:

$$T_{osc} = [(V_{rhth} - V_{rlth}) \times C_{tr}] / I_{cr} + [(V_{rhth} - V_{rlth}) \times C_{tr}] / I_{dr}$$

where:

$I_{cr}$ : is an internally generated charge current

$I_{dr}$ : is an internally generated discharge current

$V_{rhth}$ ,  $V_{rlth}$ : are two voltages defined with the output voltage and a resistor output divider

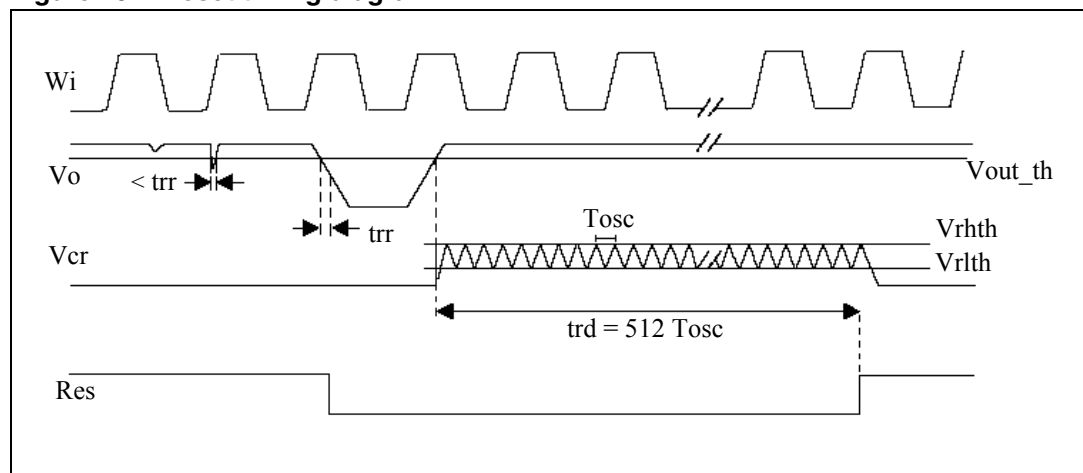
$C_{tr}$ : is an external capacitance.

$t_{rd}$  is given by:

$$t_{rd} = 512 \times T_{osc}$$

Reset is active when  $En$  is high.

**Figure 26. Reset timing diagram**





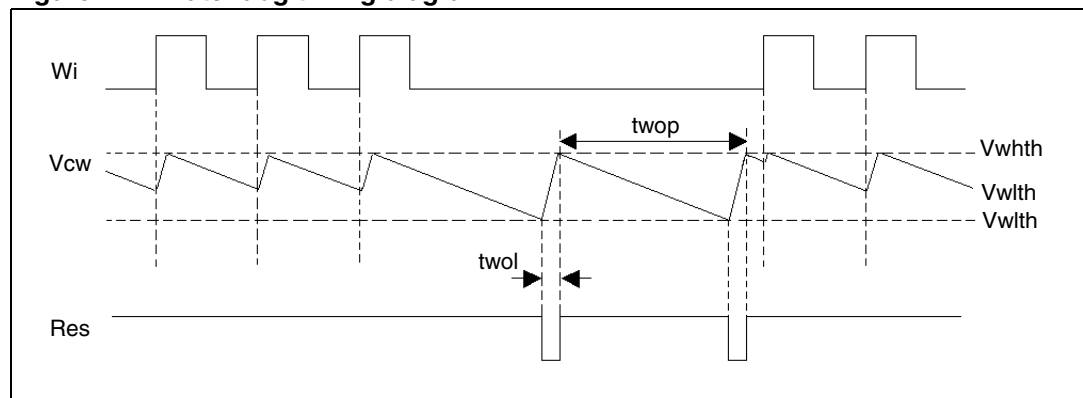
### 3.3 Watchdog

A connected microcontroller is monitored by the watchdog input  $W_i$ . If pulses are missing, the Reset output pin is set to low. The pulse sequence time can be set within a wide range with the external capacitor,  $C_{tw}$ . The watchdog circuit discharges the capacitor  $C_{tw}$ , with the constant current  $I_{wd}$ . If the lower threshold  $V_{wlth}$  is reached, a watchdog reset is generated. To prevent this the microcontroller must generate a positive edge during the discharge of the capacitor before the voltage has reached the threshold  $V_{wlth}$ . In order to calculate the minimum time  $t$ , during which the micro-controller must output the positive edge, the following equation can be used:

$$(V_{whth} - V_{wlth}) \times C_{tw} = I_{wd} \times t$$

Every  $W_i$  positive edge switches the current source from discharging to charging. The same happens when the lower threshold is reached. When the voltage reaches the upper threshold,  $V_{whth}$ , the current switches from charging to discharging. The result is a saw-tooth voltage at the watchdog timer capacitor  $C_{tw}$ .

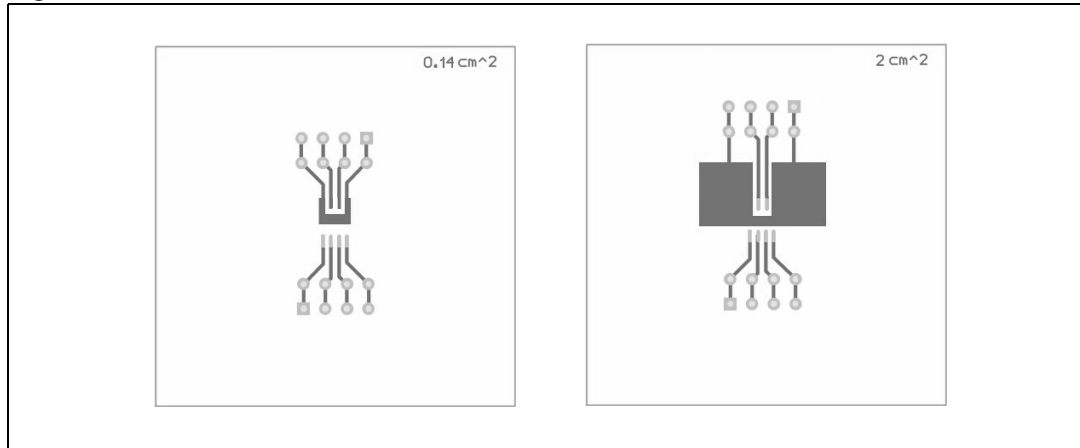
**Figure 27. Watchdog timing diagram**



## 4 Package and PCB thermal data

### 4.1 SO-8 thermal data

Figure 28. SO-8 PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area= 58mm x 58mm, PCB thickness = 2mm, Cu thickness = 35 $\mu$ m, Copper areas: from minimum pad lay-out to 2cm<sup>2</sup>).

Figure 29.  $R_{thj-amb}$  Vs. PCB copper area in open box free air condition

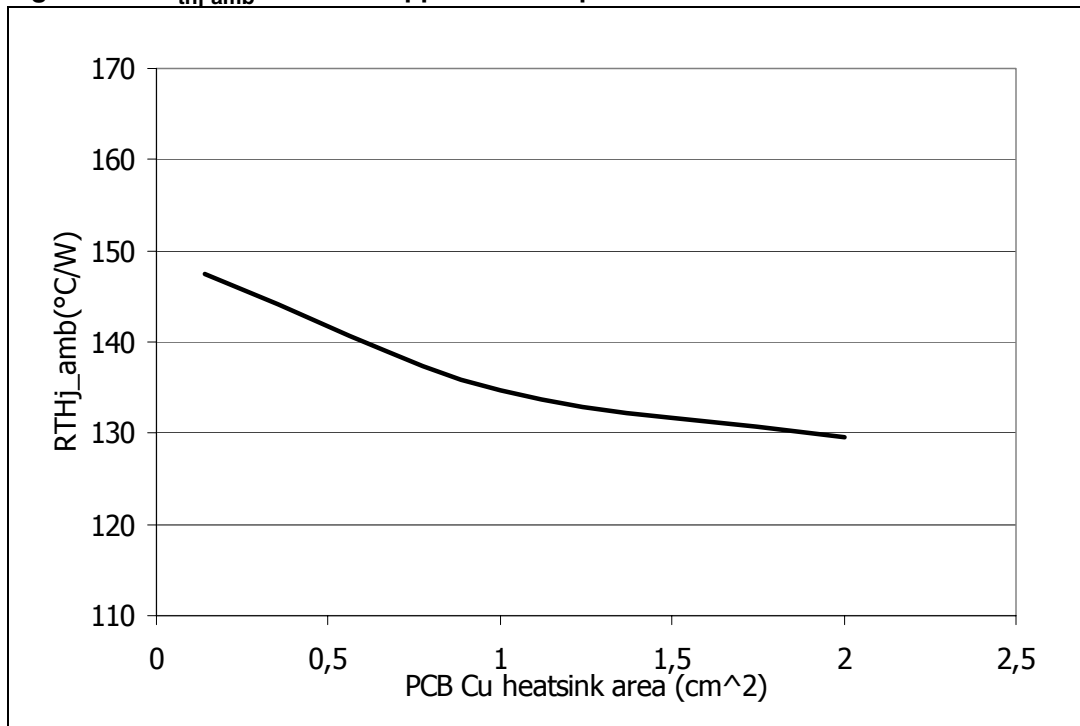
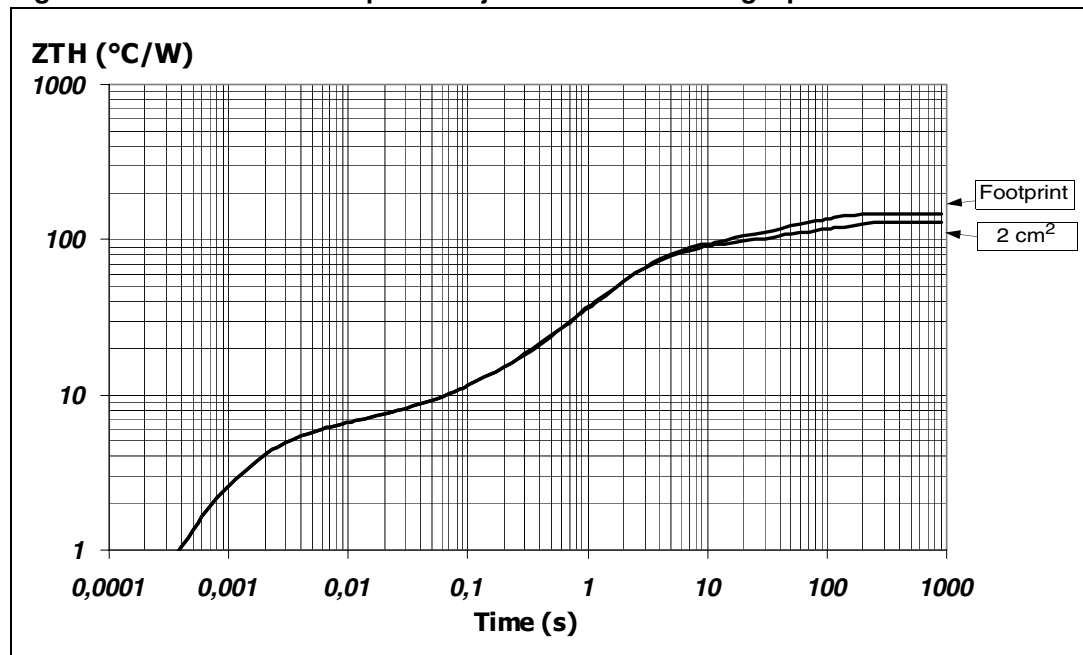


Figure 30. SO-8 thermal impedance junction ambient single pulse

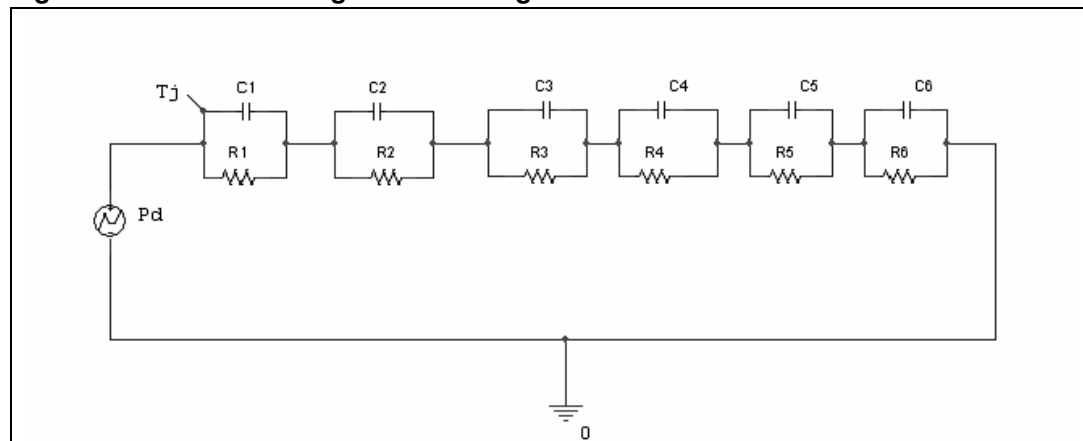


Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Figure 31. Thermal fitting model of Vreg in SO-8

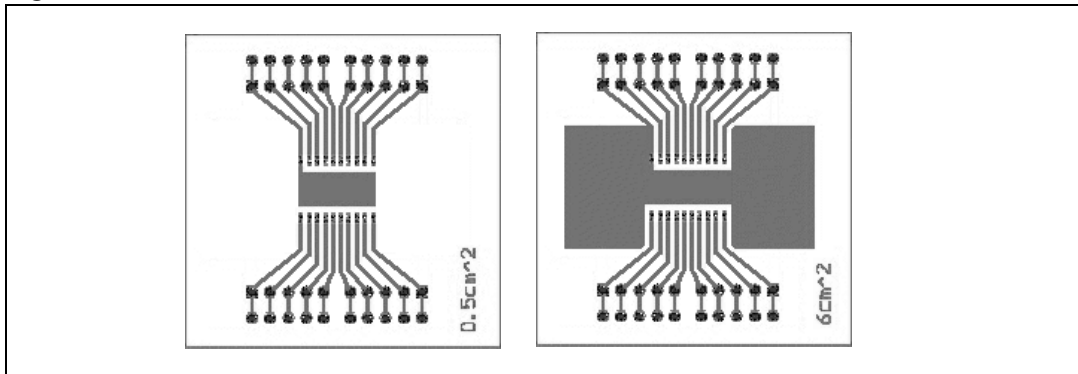


**Table 9. SO-8 thermal parameter**

| Area/island (cm <sup>2</sup> ) | Footprint | 2  |
|--------------------------------|-----------|----|
| R1 (°C/W)                      | 4.21      |    |
| R2 (°C/W)                      | 2.11      |    |
| R3 (°C/W)                      | 2         |    |
| R4 (°C/W)                      | 41        |    |
| R5 (°C/W)                      | 40        |    |
| R6 (°C/W)                      | 58        | 40 |
| C1 (W.s/°C)                    | 0.00029   |    |
| C2 (W.s/°C)                    | 0.0024    |    |
| C3 (W.s/°C)                    | 0.03      |    |
| C4 (W.s/°C)                    | 0.04      |    |
| C5 (W.s/°C)                    | 0.1       |    |
| C6 (W.s/°C)                    | 1.05      | 2  |

## 4.2 SO-20 thermal data

Figure 32. SO-20 PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area= 58mm x 58mm, PCB thickness = 2mm, Cu thickness=35 $\mu$ m, Copper areas: from minimum pad lay-out to 6cm<sup>2</sup>).

Figure 33.  $R_{thj-amb}$  Vs. PCB copper area in open box free air condition

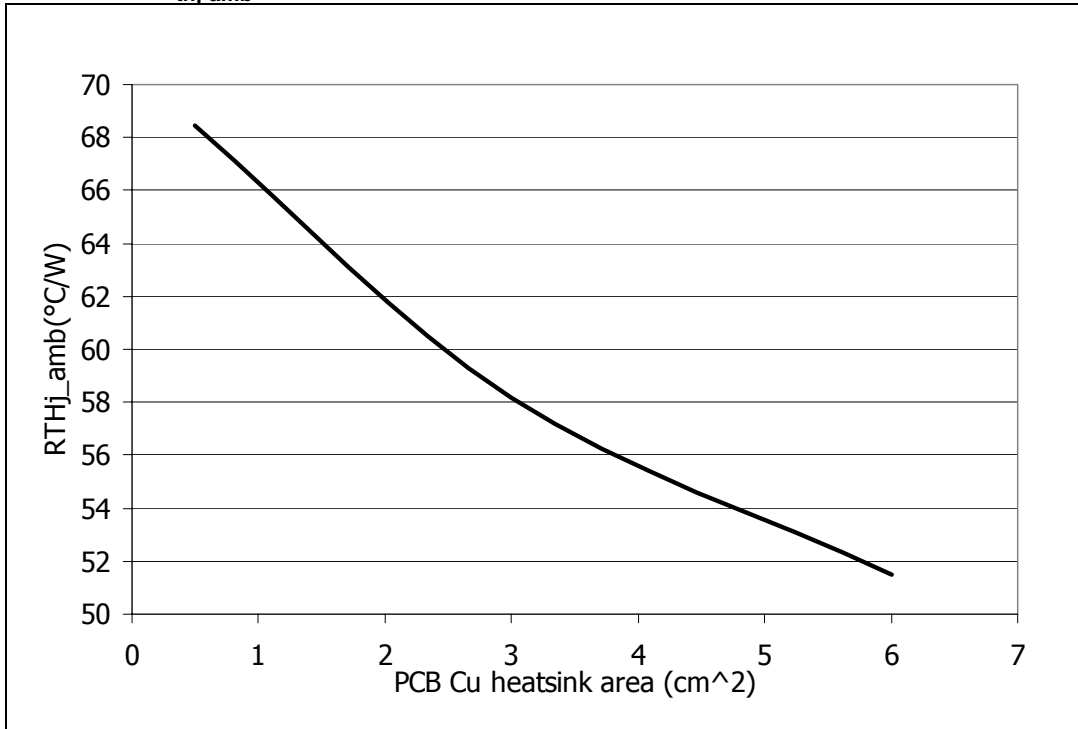
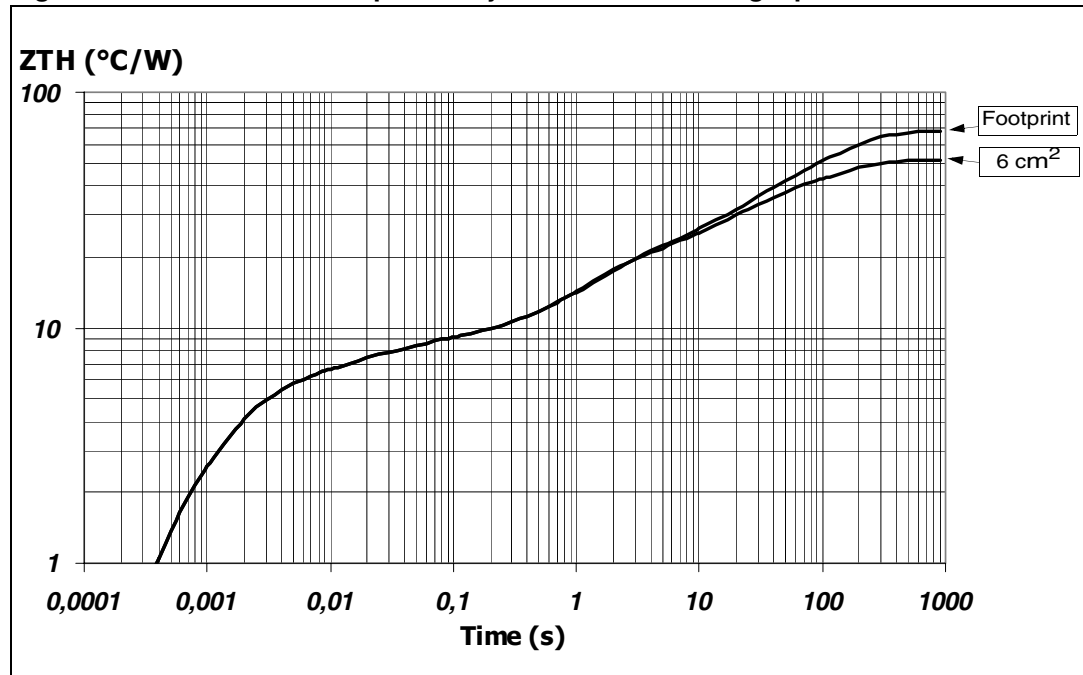


Figure 34. SO-20 thermal impedance junction ambient single pulse

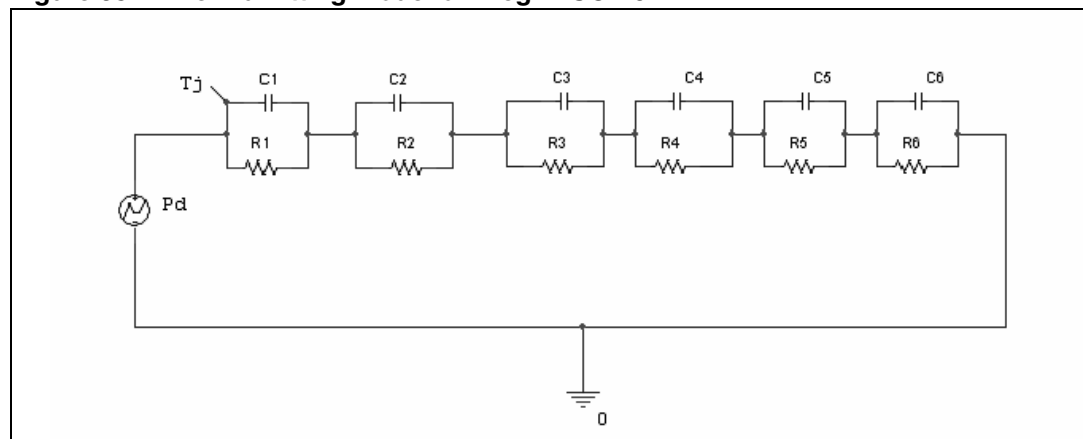


Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Figure 35. Thermal fitting model of Vreg in SO-20



**Table 10. SO-20 thermal parameter**

| Area/island (cm <sup>2</sup> ) | Footprint | 2  |
|--------------------------------|-----------|----|
| R1 (°C/W)                      | 4.21      |    |
| R2 (°C/W)                      | 2.11      |    |
| R3 (°C/W)                      | 2.2       |    |
| R4 (°C/W)                      | 10        |    |
| R5 (°C/W)                      | 15        |    |
| R6 (°C/W)                      | 35        | 18 |
| C1 (W.s/°C)                    | 0.00029   |    |
| C2 (W.s/°C)                    | 0.0024    |    |
| C3 (W.s/°C)                    | 0.015     |    |
| C4 (W.s/°C)                    | 0.15      |    |
| C5 (W.s/°C)                    | 1.5       |    |
| C6 (W.s/°C)                    | 4         | 7  |

## 5 Package and packing information

### 5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

### 5.2 SO-8 package information

Figure 36. SO-8 package dimensions

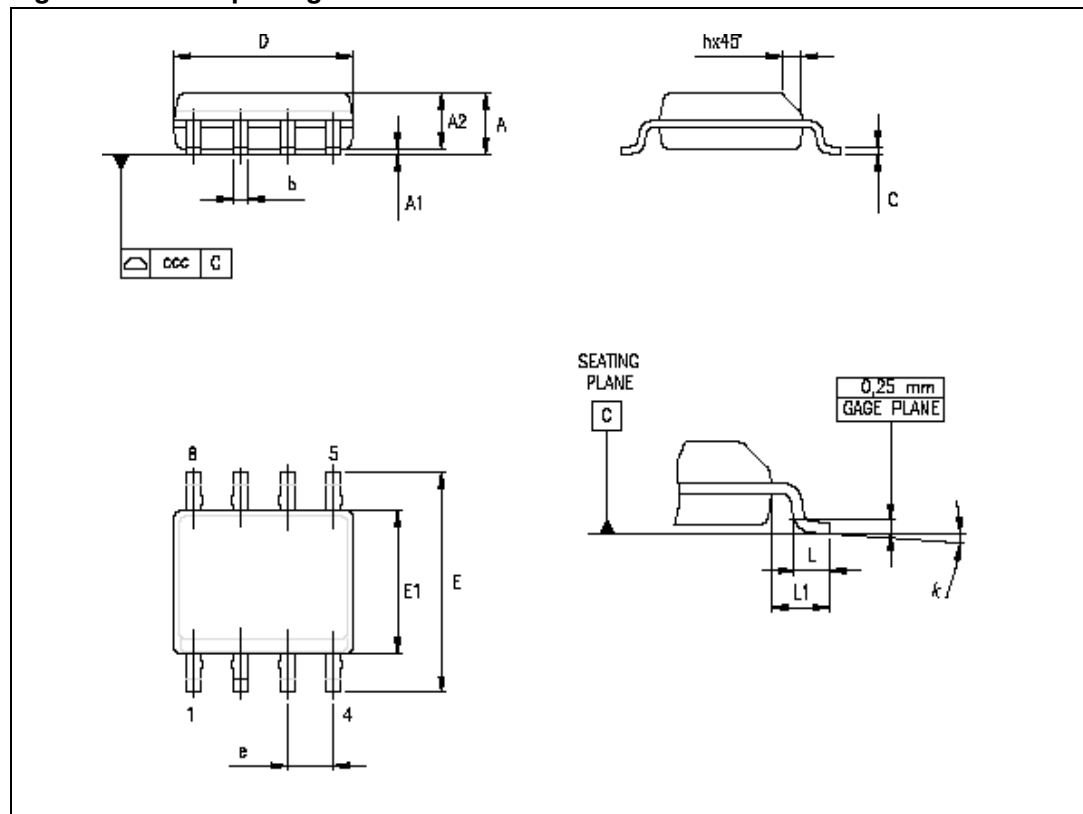




Table 11. SO-8 mechanical data

| Symbol            | Millimeters |      |      |
|-------------------|-------------|------|------|
|                   | Min.        | Typ. | Max. |
| A                 |             |      | 1.75 |
| A1                | 0.10        |      | 0.25 |
| A2                | 1.25        |      |      |
| b                 | 0.28        |      | 0.48 |
| c                 | 0.17        |      | 0.23 |
| D <sup>(1)</sup>  | 4.80        | 4.90 | 5.00 |
| E                 | 5.80        | 6.00 | 6.20 |
| E1 <sup>(2)</sup> | 3.80        | 3.90 | 4.00 |
| e                 |             | 1.27 |      |
| h                 | 0.25        |      | 0.50 |
| L                 | 0.40        |      | 1.27 |
| L1                |             | 1.04 |      |
| k                 | 0°          |      | 8°   |
| ccc               |             |      | 0.10 |

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm in total (both side).
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

### 5.3 SO-20 package information

Figure 37. SO-20 package dimensions

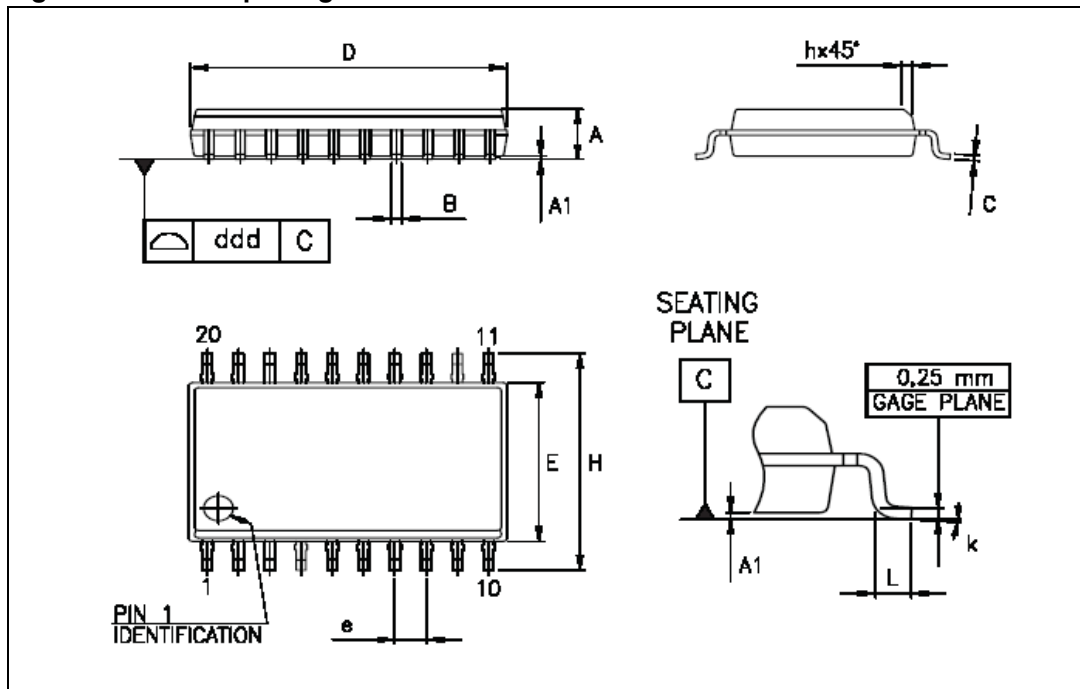


Table 12. SO-20 mechanical data

| Symbol           | Millimeters |      |       |
|------------------|-------------|------|-------|
|                  | Min.        | Typ. | Max.  |
| A                | 2.35        |      | 2.65  |
| A1               | 0.10        |      | 0.30  |
| B                | 0.33        |      | 0.51  |
| C                | 0.23        |      | 0.32  |
| D <sup>(1)</sup> | 12.60       |      | 13.00 |
| E                | 7.40        |      | 7.60  |
| e                |             | 1.27 |       |
| H                | 10.0        |      | 10.65 |
| h                | 0.25        |      | 0.75  |
| L                | 0.40        |      | 1.27  |
| k                | 0°          |      | 8°    |
| ddd              |             |      | 0.10  |

1. "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

## 5.4 SO-8 packing information

Figure 38. SO-8 tube shipment (no suffix)

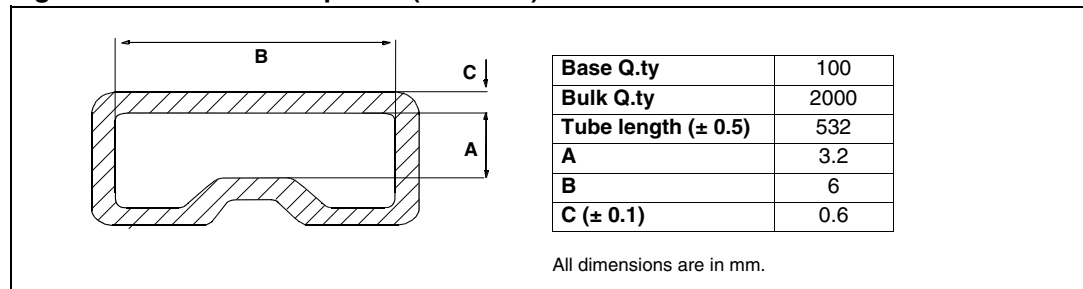
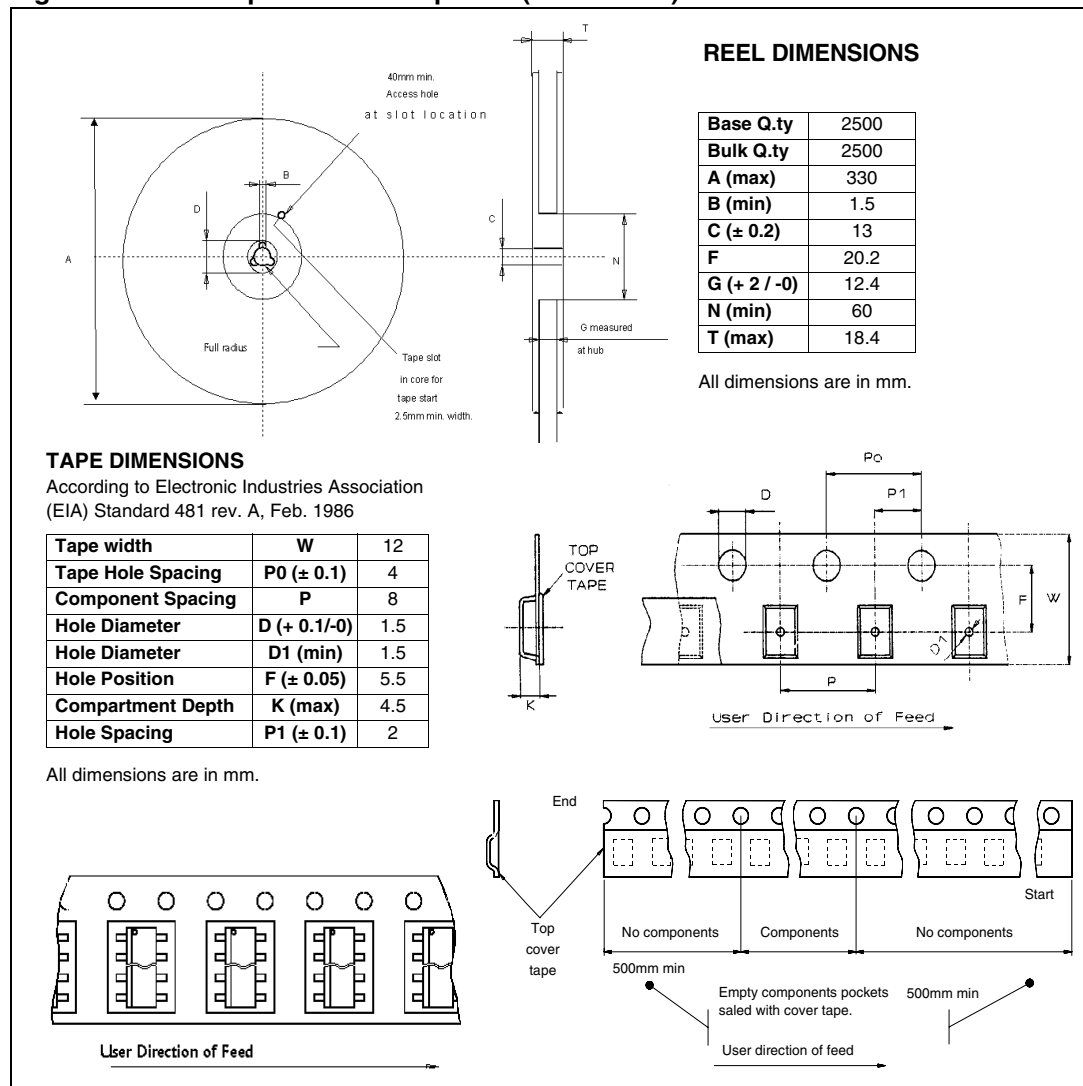


Figure 39. SO-8 tape and reel shipment (suffix "TR")



## 5.5 SO-20 packing information

Figure 40. SO-20 tube shipment (no suffix)

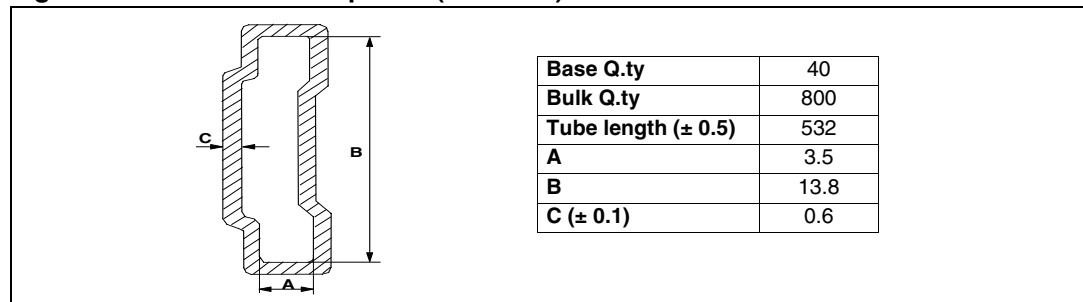
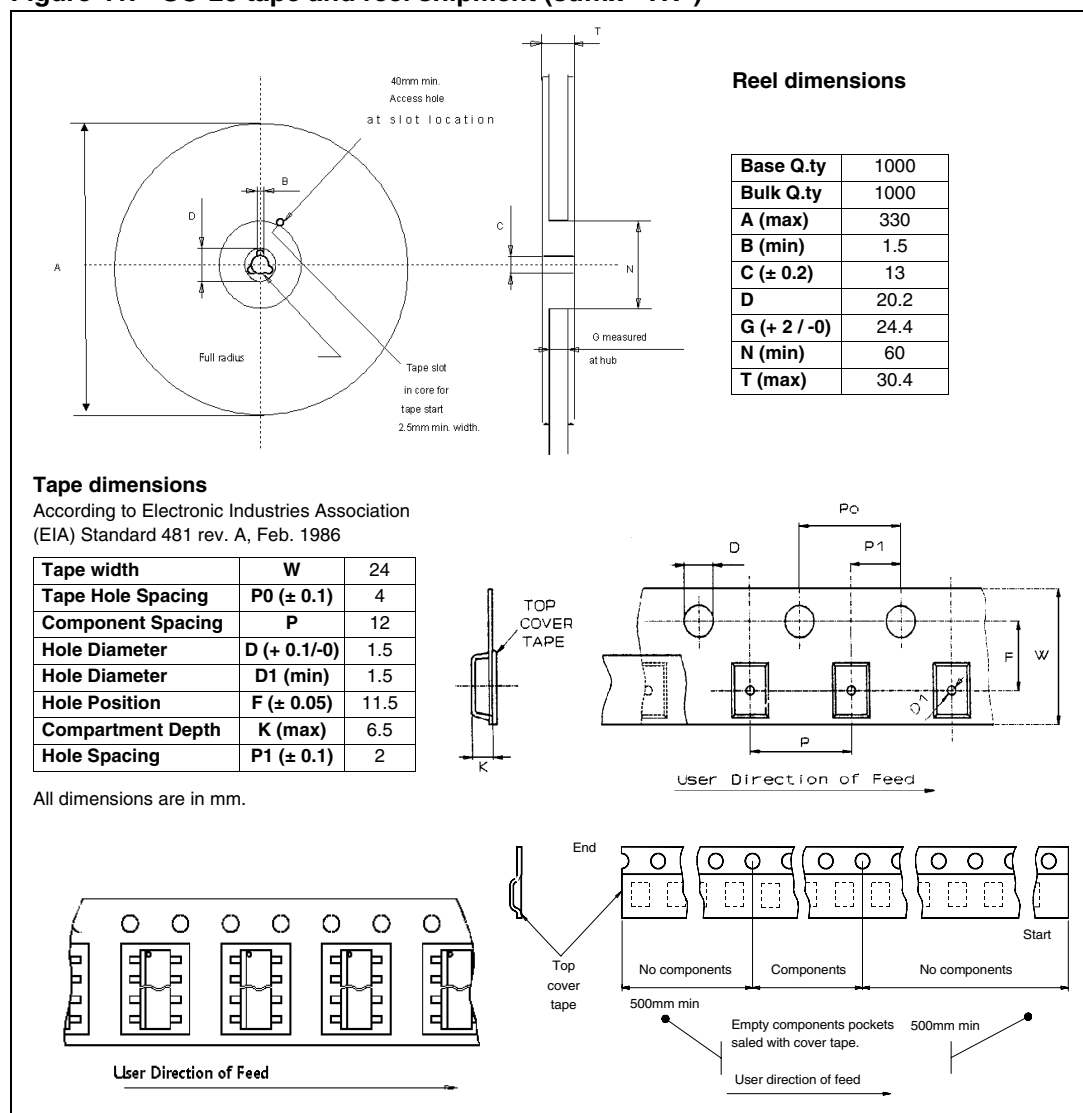


Figure 41. SO-20 tape and reel shipment (suffix "TR")



## 6 Revision history

**Table 13. Document revision history**

| Date        | Revision | Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| June-2004   | 1        | Initial release.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 18-Jan-2007 | 2        | Updated <a href="#">Table 5.</a> , <a href="#">6</a> , <a href="#">7</a> and <a href="#">8</a> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 01-Jun-2007 | 3        | Document put in corporate technical literature template.<br>Updated <a href="#">Table 4</a> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 22-Aug-2007 | 4        | <a href="#">Table 5: General</a> : updated $I_{short}$ , $I_{lim}$ , $I_q$ , $T_{rr2}$ , $V_{ih\_hist}$ parameters.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 29-Aug-2007 | 5        | Added list of tables and figures.<br>Added <a href="#">Section 4: Package and PCB thermal data</a> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 08-Apr-2008 | 6        | Document restructured.<br>Changed <a href="#">Figure 1: Block diagram</a> .<br>Updated <a href="#">Table 5: General</a> :<br><ul style="list-style-type: none"> <li>– changed <math>I_{short}</math> max value from 4000 mA to 400 mA</li> <li>– changed <math>I_{qn\_150}</math> typ. value from 1.45 mA to 1.25 mA</li> <li>– changed <math>I_{qn\_50}</math> typ. value from 538 <math>\mu</math>A to 470 <math>\mu</math>A</li> <li>– changed <math>I_{qn\_1}</math> typ. value from 120 <math>\mu</math>A to 100 <math>\mu</math>A.</li> </ul> Updated <a href="#">Table 6: Reset</a> :<br><ul style="list-style-type: none"> <li>– corrected trd formula.</li> </ul> Updated <a href="#">Table 7: Watchdog</a> :<br><ul style="list-style-type: none"> <li>– changed <math>V_{wlth}</math> values in <math>V_{o\_ref}</math> percentages</li> <li>– changed <math>V_{whth}</math> values in <math>V_{o\_ref}</math> percentages.</li> </ul> Added <a href="#">Figure 24: L4993 application schematic</a> .<br>Added <a href="#">Section 2.4: Electrical characteristics curves</a> .<br>Added <a href="#">Section 2.5: Test circuit and waveforms plot</a> . |

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