CJ4558CP--DUAL OPERATONAL AMPLIFIER

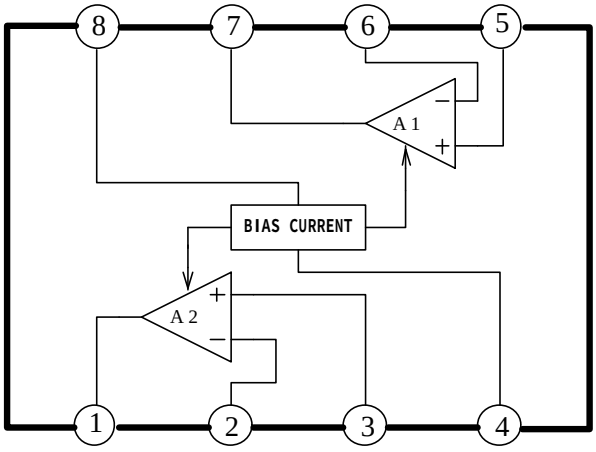
1. Overview

The CJ4558CP is a dual operational amplifier designed for use as ripple filter, compensation amplifier, audio pre-amplifier and linear amplifier in electronic devices. Its **features** are:

- Built-in phase compensation circuit
- Low noise: V_{NI} = 2.5uV
- Wide bandwidth and high speed, BW = 3MHz
- SOP-8

2. Block Diagram and Pin Description

2. 1 Block Diagram



2. 2 Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	OUT_1	Output 1	5	IN_{2+}	Positive Input 2
2	IN_{1-}	Negative Feedback1	6	IN_{2-}	Negative Input 2
3	IN_{1+}	Positive Input 1	7	OUT_2	Output 2
4	V_{EE}	V_{EE}	8	V_{CC}	V_{CC}

3. Electrical Characteristics

3. 1 Absolute Maximum Ratings

Unless otherwise specified, T_{amb}= 25℃

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}/V_{EE}	±18	V
Input Differential Voltage	V_{ID}	±30	V
Input Common-mode Voltage	V_{IC}	±15	V
Power Dissipation	P_D	500	mW
Operating Temperature	T_{amb}	-30~75	℃
Storage Temperature	T_{stg}	-55~125	℃

3. 2 Electrical Characteristics

Unless otherwise specified, T_{amb}= 25℃， V_{CC} = 15V， V_{EE} = -15V

Parameter	Symbol	Test Conditions	Value			Unit	Figs
			Min	Typ	Max		
Supply Current	I_{CC}/I_{EE}			4.0	6.0	mA	4.5
Input Offset Current	I_{IO}			5	200	nA	4.2
Input Bias Current	I_{IB}			60	500	nA	4.2
Input Common-mode Voltage	V_{IC}		±12	±14		V	4.3
Max. Output Voltage	V_{OM}	R_L≥10kΩ	±12	±14		V	4.4
		R_L≥2kΩ	±10	±13		V	4.4
Output Shot Current	I_{OS}			40		mA	4.4
Output Sink Current	I_{Osink}			40		mA	4.4
Open Loop Voltage Gain	A_{VO}	V_O=±10V R_L≥2kΩ	86	100		dB	4.7
Common-mode Rejection Ratio	CMRR	R_S ≤10kΩ	70	90		dB	4.3
Supply Voltage Rejection Ratio	K_{SVR}	R_S ≤10kΩ		30	150	uV/V	4.1
Input Offset Voltage	V_{IO}	R_S ≤10kΩ		0.5	6	mV	4.1
Slew Rate	S_R	A_V=1 R_L≥2kΩ		1.0		V/uS	4.6
Bandwidth	BW			3.0		MHz	4.7
Equivalent Input Noise Voltage	V_{NI}	R_S=1kΩ f=30Hz~30kHz		2.5		uV	

4. Test Circuit

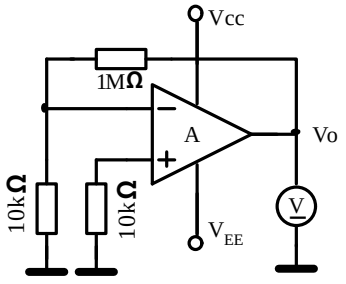


Fig 4.1

V_{IO}:

$V_{IO}=V_O$ / 100 (V)

K_{SVR}:

$K_{SVR}= (V_{IO1}-V_{IO2})$ /5 (uV/V)

V_{IO1}: V_{CC}=17.5V， V_{EE}= -17.5V

V_{IO2}: V_{CC}=12.5V， V_{EE}= -12.5V

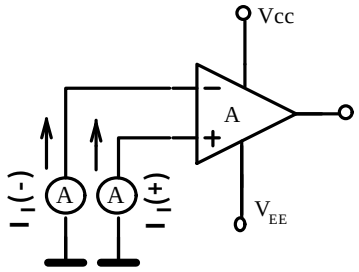


Fig 4.2

I_{IO}:
I_{IO}= | I_I(+)-I_I(-) |

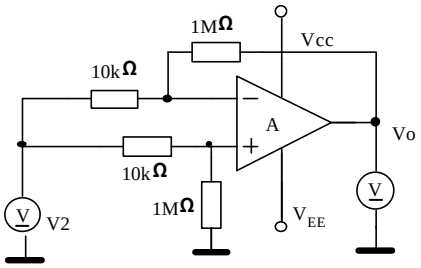


Fig 4.3

V_{IC}:
V_2 is adjustable voltage， V_O = 1V

K_{CMR}:
Differential Voltage Gain to Common-mode Voltage Gain Ratio

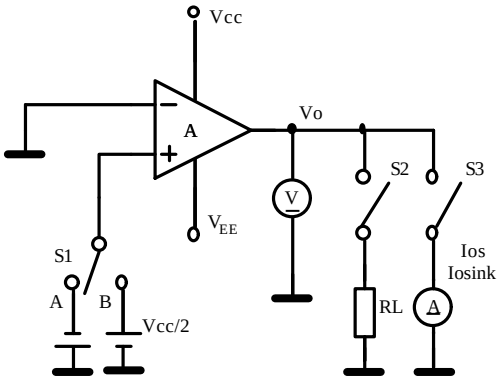


Fig 4.4

$V_{OM\ 1+}$:
S1=B，S2 OFF，S3 OFF
$V_{OM\ 1-}$:
S1=A，S2 OFF，S3 OFF
$V_{OM\ 2+}$:
S1=B，S2 ON，S3 OFF
$V_{OM\ 2-}$:
S1=A，S2 OFF，S3 ON
Iosink:
S1=A，S2 OFF，S3 ON
Ios:
S1=B，S2 OFF，S3 ON

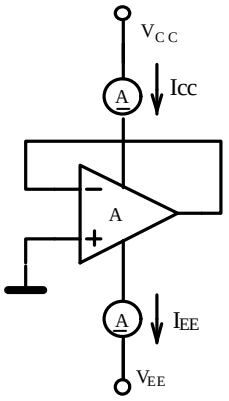


Fig 4.5

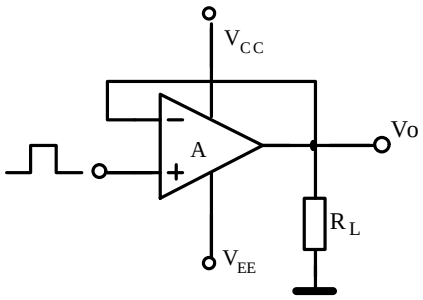
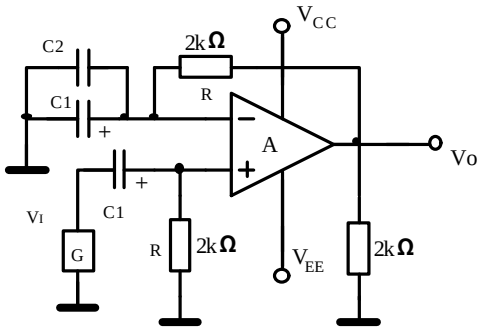


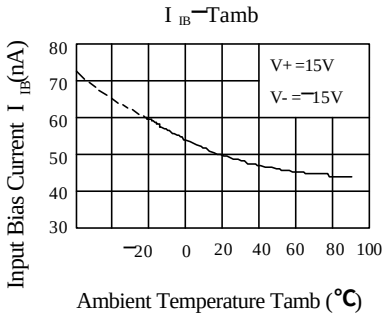
Fig 4.6

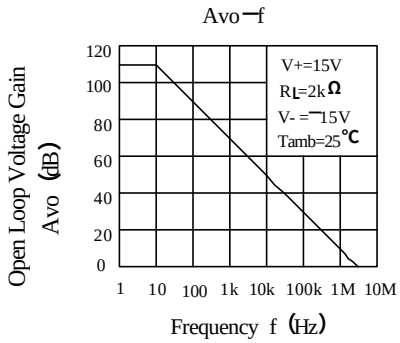


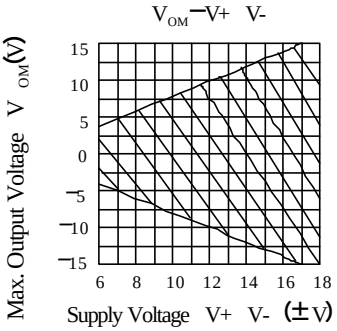
$A_{VD}=20\log(V_O/V)$
BW is the frequency of V_I when $V_O=V_I$

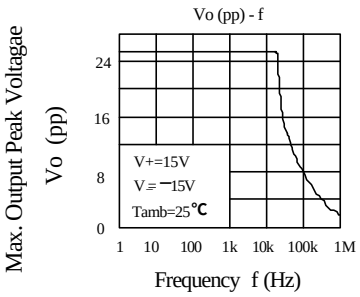
Fig 4.7

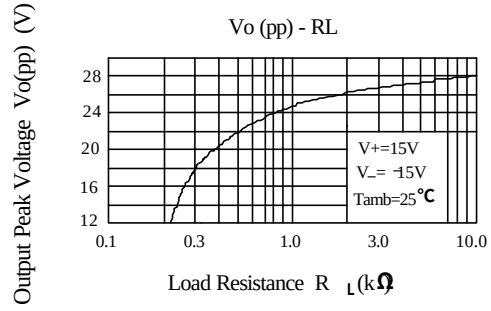
5. Characteristics Curve

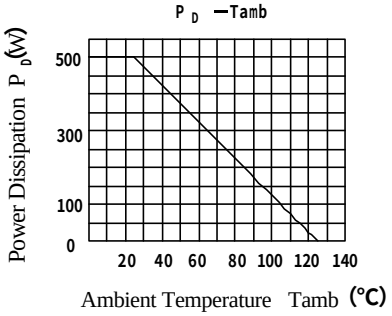




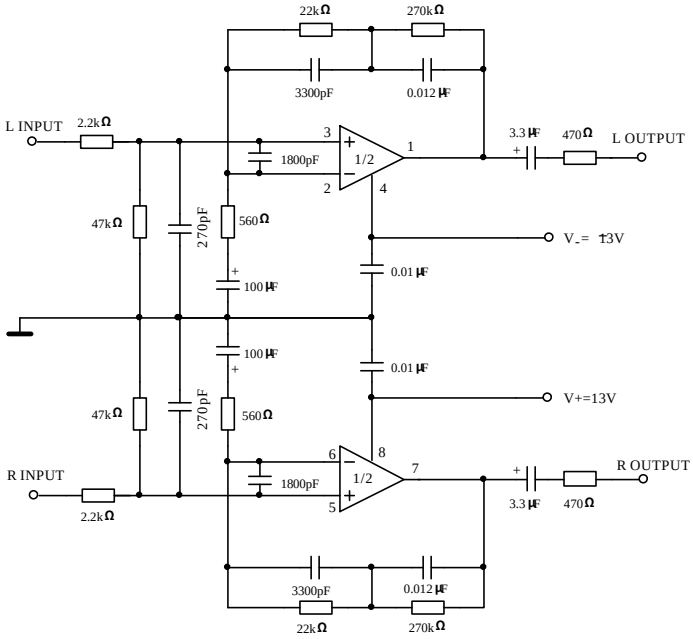








6. Application Circuit



7.Mechanical Dimensions

Package

SOP-8