



JIANGSU CHANGJIANG ELECTRONICS TECHNOLOGY CO.,LTD.

CJ4558CP--DUAL OPERATONAL AMPLIFIER

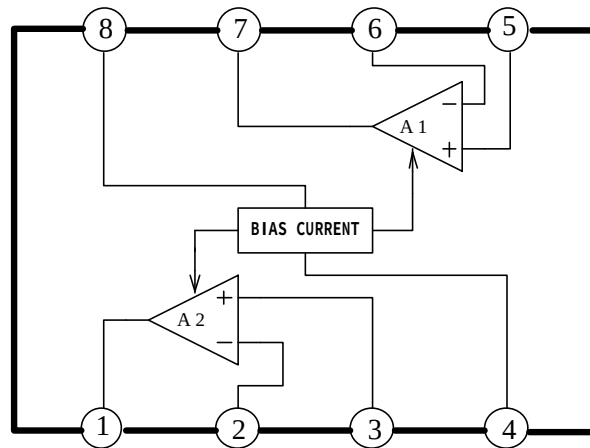
1. Overview

The CJ4558CP is a dual operational amplifier designed for use as ripple filter, compensation amplifier, audio pre-amplifier and linear amplifier in electronic devices. Its **features** are:

- Built-in phase compensation circuit
- Low noise: $V_{NI} = 2.5\mu V$
- Wide bandwidth and high speed, $BW = 3MHz$
- SOP-8

2. Block Diagram and Pin Description

2. 1 Block Diagram



2. 2 Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	OUT ₁	Output 1	5	IN ₂₊	Positive Input 2
2	IN ₁₋	Negative Feedback1	6	IN ₂₋	Negative Input 2
3	IN ₁₊	Positive Input 1	7	OUT ₂	Output 2
4	V _{EE}	V _{EE}	8	V _{CC}	V _{CC}

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3. Electrical Characteristics

3. 1 Absolute Maximum Ratings

Unless otherwise specified, $T_{amb} = 25^{\circ}\text{C}$

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}/V_{EE}	± 18	V
Input Differential Voltage	V_{ID}	± 30	V
Input Common-mode Voltage	V_{IC}	± 15	V
Power Dissipation	P_D	500	mW
Operating Temperature	T_{amb}	$-30\sim 75$	$^{\circ}\text{C}$
Storage Temperature	T_{stg}	$-55\sim 125$	$^{\circ}\text{C}$

3. 2 Electrical Characteristics

Unless otherwise specified, $T_{amb} = 25^{\circ}\text{C}$, $V_{CC} = 15\text{V}$, $V_{EE} = -15\text{V}$

Parameter	Symbol	Test Conditions	Value			Unit	Figs
			Min	Typ	Max		
Supply Current	I_{CC}/I_{EE}			4.0	6.0	mA	4.5
Input Offset Current	I_{IO}			5	200	nA	4.2
Input Bias Current	I_{IB}			60	500	nA	4.2
Input Common-mode Voltage	V_{IC}		± 12	± 14		V	4.3
Max. Output Voltage	V_{OM}	$R_L \geq 10\text{k}\Omega$	± 12	± 14		V	4.4
		$R_L \geq 2\text{k}\Omega$	± 10	± 13		V	4.4
Output Shot Current	I_{OS}			40		mA	4.4
Output Sink Current	I_{OSink}			40		mA	4.4
Open Loop Voltage Gain	A_{VO}	$V_O = \pm 10\text{V}$ $R_L \geq 2\text{k}\Omega$	86	100		dB	4.7
Common-mode Rejection Ratio	CMRR	$R_S \leq 10\text{k}\Omega$	70	90		dB	4.3
Supply Voltage Rejection Ratio	K_{SVR}	$R_S \leq 10\text{k}\Omega$		30	150	$\mu\text{V/V}$	4.1
Input Offset Voltage	V_{IO}	$R_S \leq 10\text{k}\Omega$		0.5	6	mV	4.1
Slew Rate	S_R	$A_V = 1$ $R_L \geq 2\text{k}\Omega$		1.0		V/ μs	4.6
Bandwidth	BW			3.0		MHz	4.7
Equivalent Input Noise Voltage	V_{NI}	$R_S = 1\text{k}\Omega$ $f = 30\text{Hz} \sim 30\text{kHz}$		2.5		μV	

4. Test Circuit

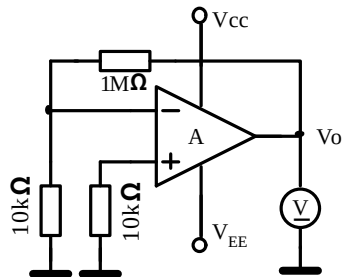


Fig 4.1

V_{IO} :

$$V_{IO} = V_O / 100 \quad (\text{V})$$

K_{SVR} :

$$K_{SVR} = (V_{IO1} - V_{IO2}) / 5 \quad (\mu\text{V/V})$$

V_{IO1} : $V_{CC} = 17.5\text{V}$, $V_{EE} = -17.5\text{V}$

V_{IO2} : $V_{CC} = 12.5\text{V}$, $V_{EE} = -12.5\text{V}$

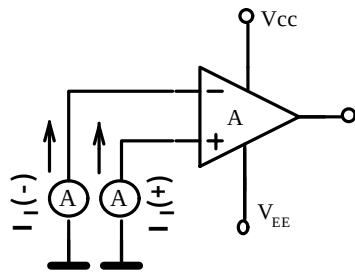


Fig 4.2

$$I_{IO} = |I_I(+)-I_I(-)|$$

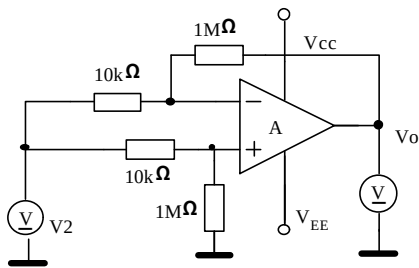


Fig 4.3

$$V_{IC}: \\ V_2 \text{ is adjustable voltage, } V_O = 1V$$

$$K_{CMR}: \\ \text{Differential Voltage Gain to Common-mode} \\ \text{Voltage Gain Ratio}$$

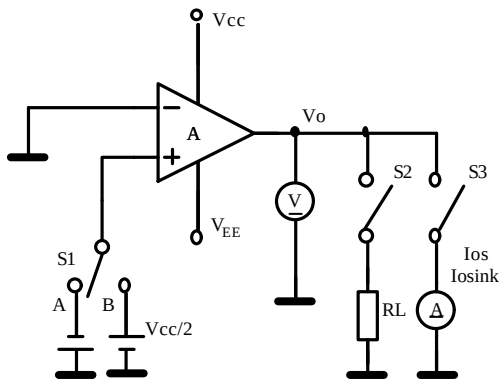


Fig 4.4

$$V_{OM\ 1+}: \\ S1=B, \ S2\ OFF, \ S3\ OFF \\ V_{OM\ 1-}: \\ S1=A, \ S2\ OFF, \ S3\ OFF \\ V_{OM\ 2+}: \\ S1=B, \ S2\ ON, \ S3\ OFF \\ V_{OM\ 2-}: \\ S1=A, \ S2\ OFF, \ S3\ ON \\ I_{osink}: \\ S1=A, \ S2\ OFF, \ S3\ ON \\ I_{os}: \\ S1=B, \ S2\ OFF, \ S3\ ON$$

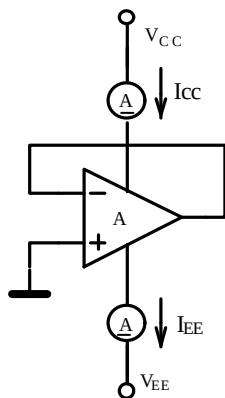


Fig 4.5

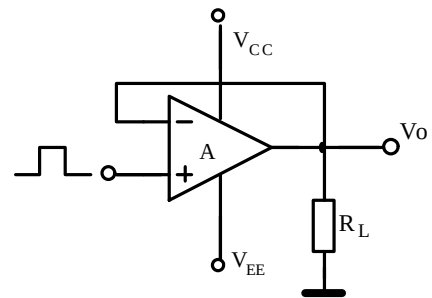


Fig 4.6

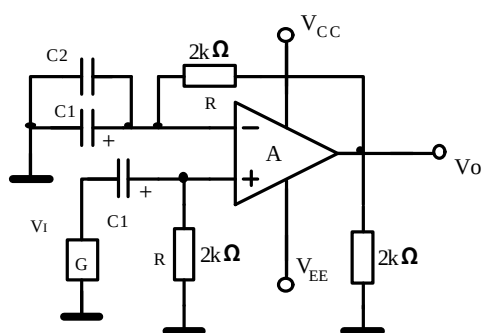
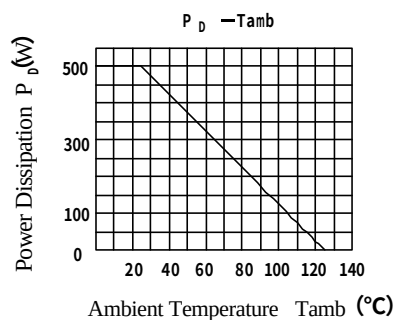
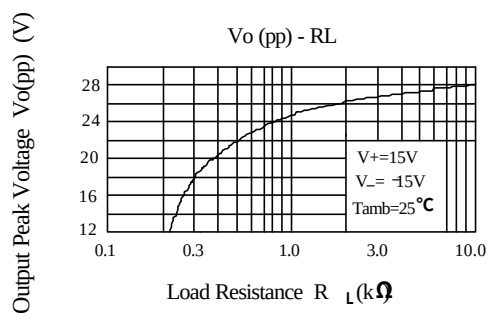
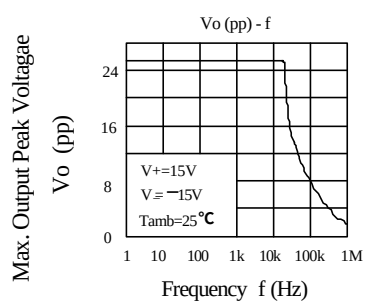
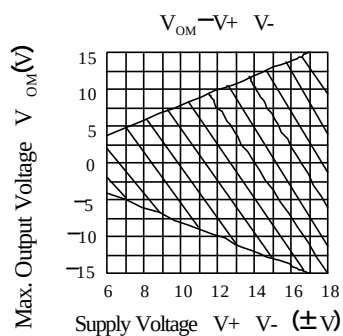
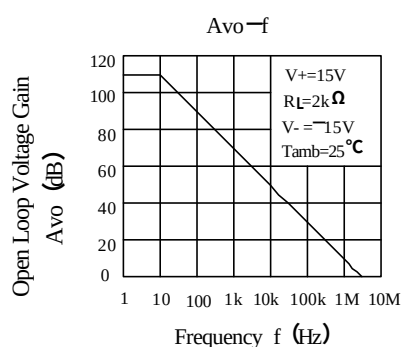
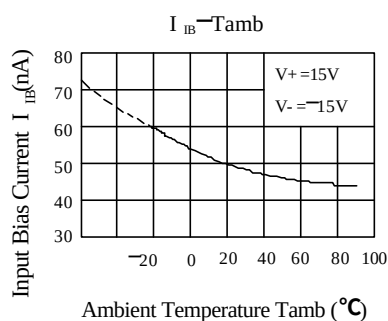


Fig 4.7

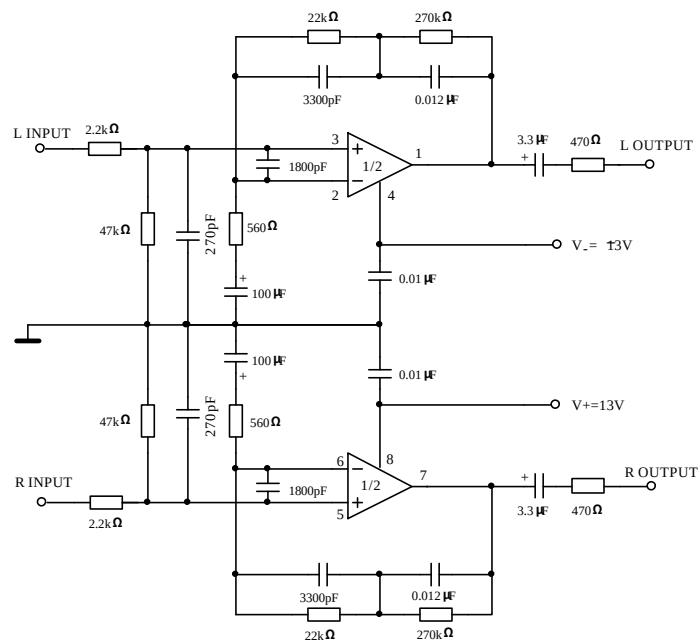
$$A_{VD} = 20 \log(V_O/V_I)$$

BW is the frequency of V_I when $V_O = V_I$

5. Characteristics Curve



6. Application Circuit



Package

Technical drawing of a 16-pin DIP package showing top, side, and end views with dimensions in inches and millimeters.

Top View Dimensions:

- Pin 1 to Pin 8 distance: 6.00 ± 0.30 in, 0.236 ± 0.012 mm
- Pin 4 to Pin 5 distance: 3.95 ± 0.20 in, 0.156 ± 0.008 mm
- Pin 1 to Pin 4 distance: 2.00 ± 0.004 in, 0.15 ± 0.10 mm
- Pin 8 to Pin 5 distance: 0.50 ± 0.20 in, 0.020 ± 0.008 mm

Side View Dimensions:

- Package height: 1.55 ± 0.20 in, 0.061 ± 0.008 mm
- Pin height: 5.13 MAX in, 0.202 MAX mm
- Pin pitch: 4.92 ± 0.20 in, 0.194 ± 0.008 mm
- Pin width: 0.56 in, (0.022) mm
- Pin spacing: 1.27 in, 0.050 mm
- Pin diameter: 0.41 ± 0.10 in, 0.016 ± 0.004 mm

End View Dimensions:

- Package width: 0.15 ± 0.004 in, 0.004 ± 0.001 mm
- Pin width: 0.180 MAX in, 0.071 MAX mm
- Pin diameter: 0.180 MAX in, 0.071 MAX mm
- Pin spacing: 0.180 MAX in, 0.071 MAX mm
- Pin diameter: 0.180 MAX in, 0.071 MAX mm

Other Dimensions:

- Package width: 0.15 ± 0.004 in, 0.004 ± 0.001 mm
- Pin width: 0.180 MAX in, 0.071 MAX mm
- Pin diameter: 0.180 MAX in, 0.071 MAX mm
- Pin spacing: 0.180 MAX in, 0.071 MAX mm
- Pin diameter: 0.180 MAX in, 0.071 MAX mm