iSCSI Controller

1-Gbps iSCSI to
133-MHz PCI-X Controller

ISP4010

Features

- Highly integrated, low power design (1.2 watts)
- 66/133-MHz, 64-bit, true multifunction PCI-X host bus interface
- Backward compatible to 33/66-MHz, 32-bit PCI
- 3.3-V and 5-V tolerant PCI interface
- 1-Gbps switched full-duplex Ethernet topologies
- Full hardware-based TCP/IP offload including fragmentation, reassembly, and out-of-order processing
- SCSI, TCP, IP, and Ethernet interfaces
- Two embedded 32-bit RISC processors
- Full iSCSI offload with header and data digests in hardware
- Overlapping data path protection through byte parity and/or ECC
- PCI dual-address cycle and cache commands
- SCSI initiator, target, and initiator/target modes
- Multi-ID aliasing in target mode
- JTAG boundary scan, full scan, and memory built-in self-test (BIST)

VERSITLE, HIGH PERFORMANCE DESIGN. The ISP4010 is a highly integrated bus master, single chip, iSCSI controller and TCP offload engine (TOE) for storage and networking applications. The ISP4010 is an optimal mix of hardware state machines for performance and embedded processors for flexibility. The bulk data movement functions of TCP/IP are executed in hardware, and embedded processors are used for iSCSI, TCP connection establishment/teardown, and other functions. By supporting SCSI, TCP, IP, and Ethernet interfaces, the ISP4010 can support a wide variety of storage area network (SAN) and local area network (LAN) applications. The ISP4010 can be used in both target and initiator systems.

The ISP4010 minimizes host CPU loads by handling complete I/O transactions without host intervention. Embedded processors control the chip interfaces; execute simultaneous, multiple I/O control blocks (IOCBs); and maintain the required thread information for each transfer.

PCI-X INTERFACE. The PCI/PCI-X interface operates as a 32/64-bit DMA bus master. The PCI bus interface unit (PBIU) contains a DMA controller that generates and samples PCI control signals, generates host memory addresses, and facilitates data transfers between host memory and the on-board frame buffer. The PBIU also facilitates access to the ISP4010 internal registers and communicates with the embedded RISC processors.

The DMA controller has 11 independent channels that initiate transactions on PCI and transfer data between host memory and various chip functions. The PBIU arbitrates among the DMA channels, servicing them alternately.

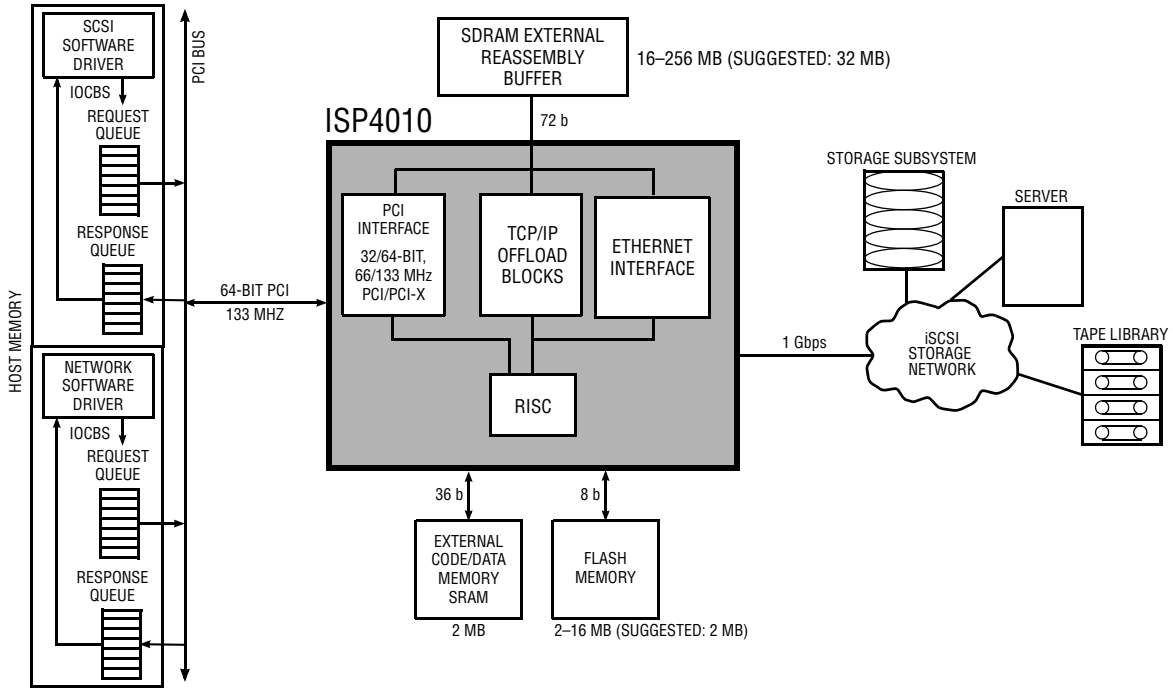
MEDIA FLEXIBILITY. The ISP4010 provides a 10-bit interface for an external copper phy, or an external SERDES for fiber optic implementations.

HARDWARE TOE FOR LOW POWER AND HIGH PERFORMANCE. The TOE has six hardware modules for transmit and receive functions for TCP, IP, and Ethernet MAC layers. Each layer is accessible to the host or embedded processors. The TOE is self-contained and implements all TCP/IP exceptions in hardware for optimal performance.

SUBSYSTEM ORGANIZATION. The ISP4010 incorporates two high-speed embedded 32-bit RISC processors; inbound and outbound hardware-based TOEs; a 1-Gbps Ethernet MAC; an external reassembly buffer interface; a PCI/PCI-X bus; and an 11-channel, bus master, DMA controller.

Each layer of the protocol stack and the RISC processors run independently; they also pipeline data to maximize traffic flow through the chip. The following illustration shows the ISP4010, with commonly used memories, connected to servers and storage in a SAN.

powered by qlogic



Host Bus Interface Specifications	
Speed	64-bit, 133-MHz PCI-X, backward compatible to 32-bit, 32/64-bit PCI
Voltage	3.3 V (5.0 V tolerant)
Compliance	Conforms to *PCI Local Bus Specification* rev. 2.2, *PCI-X Specification* rev. 1.0a, *PCI Bus Power Management Interface Specification* rev. 1.1 (PC99)
DMA channels	11-channel DMA controller
Other features	64-bit host memory addressing, 32-bit PCI target, pipelined DMA registers for efficient scatter/gather operations, 32-bit DMA transfer counter for large I/O transfer lengths
iSCSI/TOE Specifications	
Architecture	Hardware state machine based
TCP functions	TCP checksums, acknowledgements, and retransmissions; segmentation and reassembly; out-of-order processing; congestion control techniques including slow start, congestion avoidance, fast retransmission, and fast recovery
UDP functions	User datagram protocol (UDP) checksum
Compliance	Internet engineering task force (IETF): *iSCSI* (see the QLogic web site for updates: www.qlogic.com/support), *iSCSI Requirements and Design Considerations*, *iSCSI Naming and Discovery*, *Internet Protocol Specification (IPv4)*, RFC793, *Transmission Control Protocol (TCP) Specification*, RFC1122, *Requirements for Internet Hosts—Communication Layers*, RFC1323, *TCP Extensions for High Performance*, RFC2581, *TCP Congestion Control* ANSI SCSI: *SCSI-3 Architecture Model* (SAM), X3T10/994D/Rev 18, *SCSI-3 Controller Command Set*, X3T10/Project 1047D/Rev 6c IEEE: 802.1Q *Virtual LAN (VLAN)*, 802.1p *Priority of Service*, 802.3*x Flow Control*
IP functions	IP fragmentation and reassembly
Physical Specifications	
Port	Single 1-Gbps Ethernet
Package	529-pin thermally enhanced plastic ball grid array (EPBGA-T), 37.50 mm (± 0.20) × 37.50 mm (± 0.20)
Environment and Equipment Specifications	
Airflow	TBD
Case temperature	80°C
Power supply	1.8 V and 3.3 V
Power dissipation	1.2 watts
Ordering Information	
ISP4010	Ships to OEMs in 21-unit trays

www.qlogic.com

QLogic Corporation • 26650 Aliso Viejo Parkway • Aliso Viejo, CA 92656 • (800) 662-4471 or (949) 389-6000