QUAD DIGITAL ISOLATOR WITH SELECTABLE FAILSAFE OUTPUT

FEATURES

- 0-Mbps (DC) to 25 Mbps Signaling Rate
  - Low Channel-to-Channel Output Skew; 2 ns Max
  - Low Pulse-Width Distortion (PWD); 2.5 ns Max
- Typical 25-Year Life at Rated Working Voltage (see application note SLLA197 and Figure 11)
- 4000-V_{peak} Isolation, 560 V_{peak} V_{IORM}
  - UL 1577 , IEC 60747-5-2 (VDE 0884, Rev 2), IEC 61010-1 and CSA Approved
- 4 kV ESD Protection
- Operates with 3.3-V or 5-V Supplies
- High Electromagnetic Immunity (see application note SLLA181)
- –40°C to 125°C Operating Range

APPLICATIONS

- Flat Plasma Display Panels
- Industrial Fieldbus
- Computer Peripheral Interface
- Servo Control Interface
- Data Acquisition

DESCRIPTION

The ISO7240CF is a quad-channel digital isolator with an input disable function and a selectable high or low failsafe-output function with the CTRL pin (pin 10). The device has logic input and output buffers separated by TI's silicon dioxide (SiO_2) isolation barrier. When used in conjunction with isolated power supplies, the device blocks high voltage, isolates grounds, and prevents noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

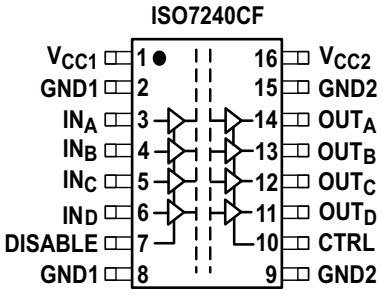
A periodic update pulse is sent across the barrier to ensure the proper dc level of the output. If this dc-refresh pulse is not received for more than 4 µs, the input is assumed to be unpowered or not being actively driven, and the failsafe circuit drives the output to the logic state selected by the user.

The failsafe-output is a logic high when a logic-high is placed on the CTRL pin or it is left unconnected. If a logic-low signal is applied to the CTRL pin, the failsafe-output becomes a logic-low output state.

The ISO7240CF also includes an input disable function that prevents data from being passed across the isolation barrier to the output. When the inputs are disabled, the outputs are set by the CTRL pin.

This device may be powered from either 3.3-V or 5-V supplies on either side in any combination. Note that the signal input pins are 5-V tolerant regardless of the voltage supply level being used.

The device is characterized for operation over the ambient temperature range of –40°C to 125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DEVICE FUNCTION TABLE(1)

V_{CC1}	V_{CC2}	DATA INPUT (IN)	DISABLE INPUT (DISABLE)	FAILSAFE CONTROL INPUT (CTRL)	DATA OUTPUT (OUT)
PU	PU	H	L or Open	X	H
PU	PU	L	L or Open	X	L
X	PU	X	H	H or Open	H
X	PU	X	H	L	L
PD	PU	X	X	H or Open	H
PD	PU	X	X	L	L

(1) PU = Powered Up; PD = Powered Down; X = Irrelevant; H = High Level; L = Low Level

ABSOLUTE MAXIMUM RATINGS(1)

					VALUE	UNIT
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}				–0.5 to 6	V
V_I	Voltage at IN, OUT, EN				–0.5 to 6	V
I_O	Output current				±15	mA
ESD	Electrostatic discharge	Human Body Model	Electrostatic discharge JEDEC Standard 22, Test Method A114-C.01	All pins	±4	kV
		Field-Induced-Charged Device Model	JEDEC Standard 22, Test Method C101		±1	
		Machine Model	ANSI/ESDS5.2-1996		±200	V
T_J	Maximum junction temperature				170	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal and are peak voltage values.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage, V_{CC1}, V_{CC2}	4.5		5.5	V
		3		3.6	
I_{OH}	High-level output current			4	mA
I_{OL}	Low-level output current	–4			mA
t_{ui}	Input pulse width	40			ns
$1/t_{ui}$	Signaling rate	0	30(1)	25	Mbps
V_{IH}	High-level input voltage (IN, DISABLE, CTRL)	2		V_{CC}	V
V_{IL}	Low-level input voltage (IN, DISABLE, CTRL)	0		0.8	V
T_J	Junction temperature			150	°C
H	External magnetic field-strength immunity per IEC 61000-4-8 and IEC 61000-4-9 certification			1000	A/m

(1) Typical signaling rate under ideal conditions at 25°C.

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} at 5-V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Supply current	Quiescent	V_I = V_{CC} or 0 V, all channels, no load		1	3	mA
		25 Mbps			7	10.5	
I_{CC2}	Supply current	Quiescent	V_I = V_{CC} or 0 V, all channels, no load		15	22	mA
		25 Mbps			17	25	
I_{OFF}	Sleep mode output current		DISABLE at V_{CC}, single channel		0		µA
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.4			V
			I_{OH} = –20 µA, See Figure 1	V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1			0.4	V
			I_{OL} = 20 µA, See Figure 1			0.1	
$V_{I(HYS)}$	Input voltage hysteresis				200		mV
I_{IH}	High-level input current		IN, DISABLE, CTRL from 0 V to V_{CC}			10	µA
I_{IL}	Low-level input current			–10			
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 4	35	50		kV/µs

SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} at 5-V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay, low-to-high-level output	See Figure 1	18		42	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)				2.5	
$t_{sk(pp)}$	Part-to-part skew (2)				8	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)			0	2	ns
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		
t_{wake}	Wake time from input disable	See Figure 2		15		µs
t_{fs}	Failsafe output delay time from input power loss	See Figure 3		12		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS

V_{CC1} at 5 V and V_{CC2} at 3.3 V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Supply current	Quiescent	V_I = V_{CC} or 0 V, all channels, no load		1	3	mA
		25 Mbps			7	10.5	
I_{CC2}	Supply current	Quiescent	V_I = V_{CC} or 0 V, all channels, no load		9.5	15	mA
		25 Mbps			10.5	17	
I_{OFF}	Sleep mode output current		DISABLE at Vcc, single channel		0		µA
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.4			V
			I_{OH} = –20 µA, See Figure 1	V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1			0.4	V
			I_{OL} = 20 µA, See Figure 1			0.1	
$V_{I(HYS)}$	Input voltage hysteresis				200		mV
I_{IH}	High-level input current		IN, DISABLE, CTRL from 0 V to V_{CC}			10	µA
I_{IL}	Low-level input current			–10			
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 4	25	50		kV/µs

SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} at 3.3-V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay, low-to-high-level output	See Figure 1	20		46	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)				3	
$t_{sk(pp)}$	Part-to-part skew (2)				10	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)			0	2.5	ns
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		
t_{wake}	Wake time from input disable	See Figure 2		15		µs
t_{fs}	Failsafe output delay time from input power loss	See Figure 3		18		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS

V_{CC1} at 3.3-V, V_{CC2} at 5-V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Supply current	Quiescent	V_I = V_{CC} or 0 V, all channels, no load		0.5	1	mA
		25 Mbps			3	5	
I_{CC2}	Supply current	Quiescent	V_I = V_{CC} or 0 V, all channels, no load		15	22	mA
		25 Mbps			17	25	
I_{OFF}	Sleep mode output current		DISABLE at V_{CC}, single channel		0		µA
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.4			V
			I_{OH} = –20 µA, See Figure 1	V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1			0.4	V
			I_{OL} = 20 µA, See Figure 1		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis				200		mV
I_{IH}	High-level input current		IN, DISABLE, CTRL from 0 V to V_{CC}			10	µA
I_{IL}	Low-level input current			–10			
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 4	25	50		kV/µs

SWITCHING CHARACTERISTICS

V_{CC1} at 3.3-V and V_{CC2} at 5-V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay, low-to-high-level output	See Figure 1	22		51	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)				3	
$t_{sk(pp)}$	Part-to-part skew (2)				10	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)			0	2.5	ns
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		
t_{wake}	Wake time from input disable	See Figure 2		15		µs
t_{fs}	Failsafe output delay time from input power loss	See Figure 3		12		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} at 3.3-V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Supply current	Quiescent	V_I = V_{CC} or 0 V, all channels, no load		0.5	1	mA
		25 Mbps			3	5	
I_{CC2}	Supply current	Quiescent	V_I = V_{CC} or 0 V, all channels, no load		9.5	15	mA
		25 Mbps			10.5	17	
I_{OFF}	Sleep mode output current		DISABLE at V_{CC}, single channel		0		µA
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.4			V
			I_{OH} = –20 µA, See Figure 1	V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1			0.4	V
			I_{OL} = 20 µA, See Figure 1			0.1	
$V_{I(HYS)}$	Input voltage hysteresis				200		mV
I_{IH}	High-level input current		IN, DISABLE, CTRL from 0 V to V_{CC}			10	µA
I_{IL}	Low-level input current			–10			
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 4	25	50		kV/µs

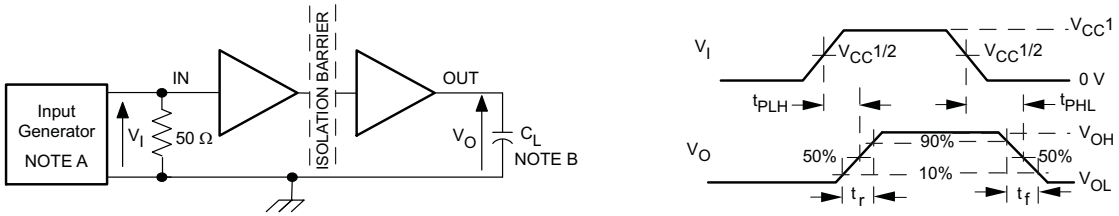
SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} at 3.3-V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay, low-to-high-level output	See Figure 1	25		56	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)				4	
$t_{sk(pp)}$	Part-to-part skew (2)				10	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)			0	3	ns
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		
t_{wake}	Wake time from input disable	See Figure 2		15		µs
t_{fs}	Failsafe output delay time from input power loss	See Figure 3		18		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

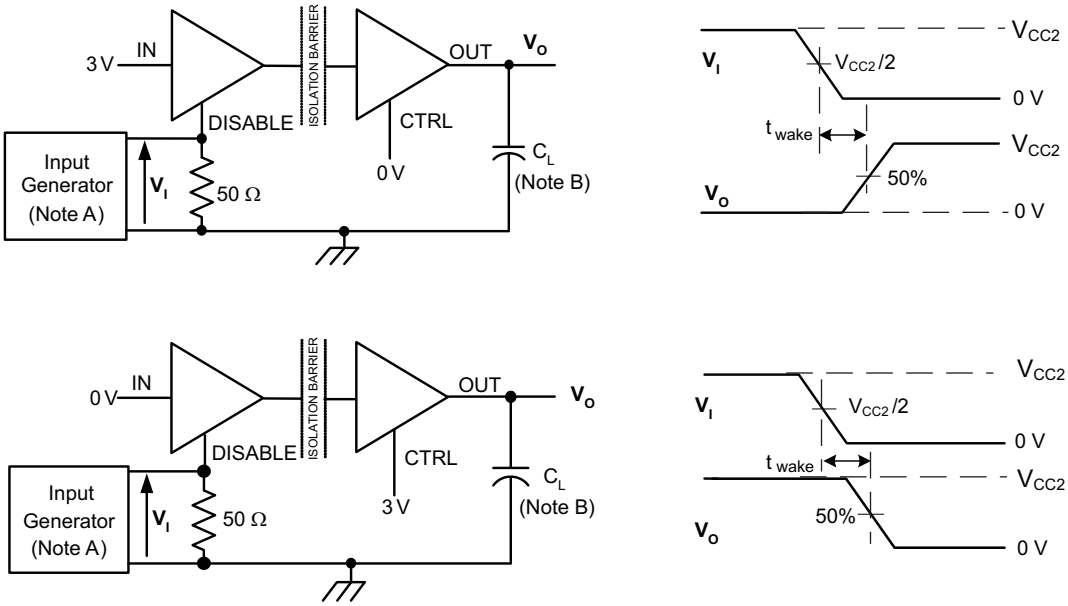
PARAMETER MEASUREMENT INFORMATION



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms

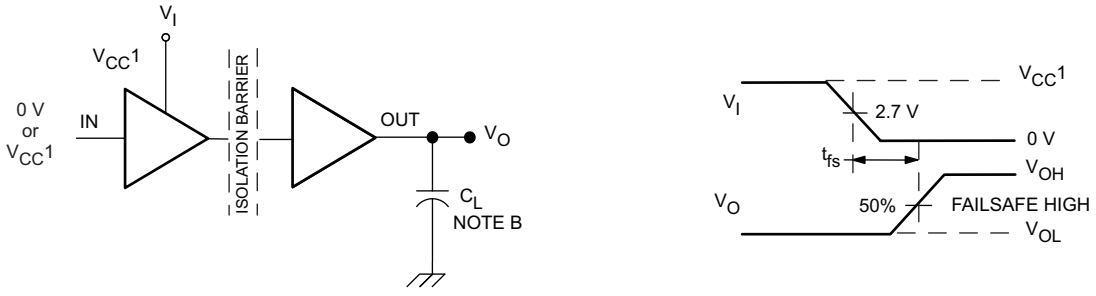


NOTE: Which ever test yields the longest time is used in this data sheet.

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 2. Wake Time From Input Disable

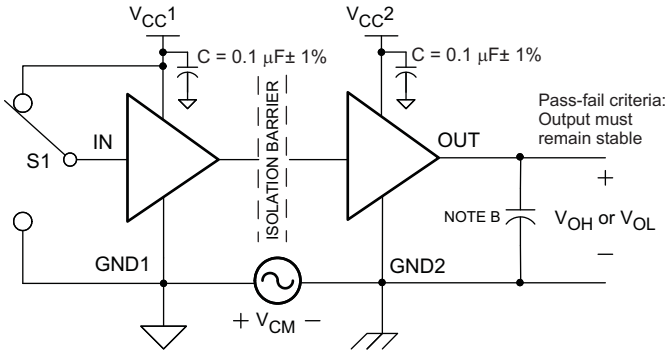


A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 3. Failsafe Delay Time Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

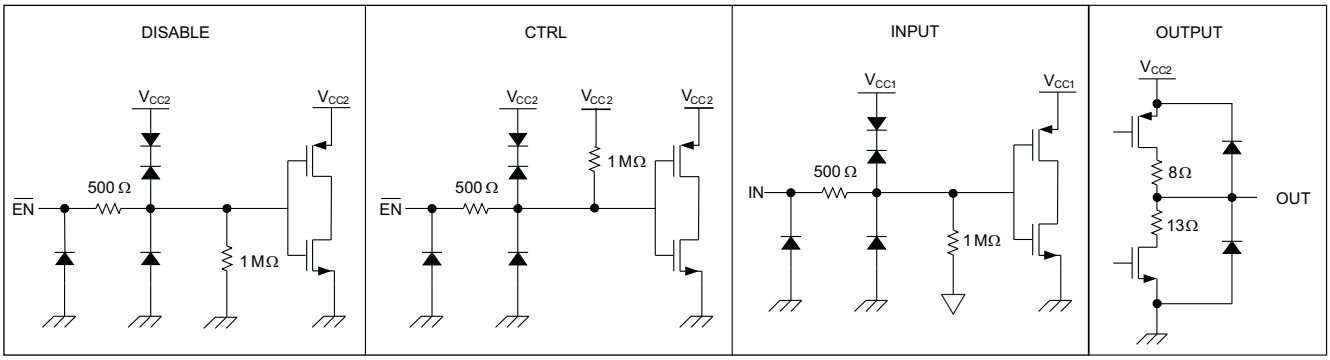
Figure 4. Common-Mode Transient Immunity Test Circuit

DEVICE INFORMATION

PACKAGE CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal-to-terminal distance through air	7.7			mm
L(I02)	Minimum external tracking (Creepage)	Shortest terminal-to-terminal distance across the package surface	8.1			mm
	Minimum Internal Gap (Internal Clearance)	Distance through the insulation	0.008			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together creating a two-terminal device, T_A < 100°C		>10^{12}		Ω
		Input to output, V_{IO} = 500 V, 100°C ≤ T_A ≤ T_A max		>10^{11}		Ω
C_{IO}	Barrier capacitance Input to output	V_I = 0.4 sin (4E6πt)		1		pF
C_I	Input capacitance to ground	V_I = 0.4 sin (4E6πt)		1		pF

DEVICE I/O SCHEMATICS



THERMAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-air	Low-K Thermal Resistance(1)		168		°C/W
		High-K Thermal Resistance		96.1		
θ_{JB}	Junction-to-Board Thermal Resistance			61		°C/W
θ_{JC}	Junction-to-Case Thermal Resistance			48		°C/W
P_D	Device Power Dissipation	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 12.5 MHz 50% duty cycle square wave			220	mW

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

REGULATORY INFORMATION

UL
Recognized under 1577 Component Recognition Program(1)
File Number: E181974

(1) Production tested ≥ 3000 VRMS for 1 second in accordance with UL 1577.

TYPICAL CHARACTERISTIC CURVES

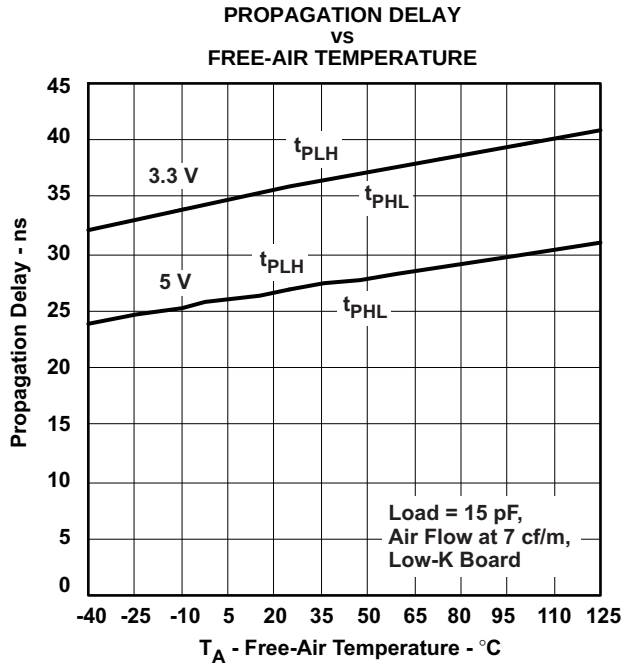


Figure 5.

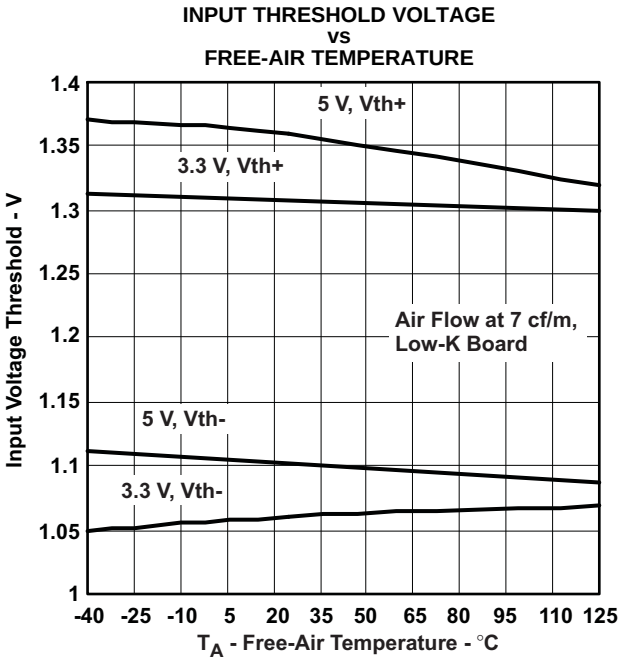


Figure 6.

TYPICAL CHARACTERISTIC CURVES (continued)

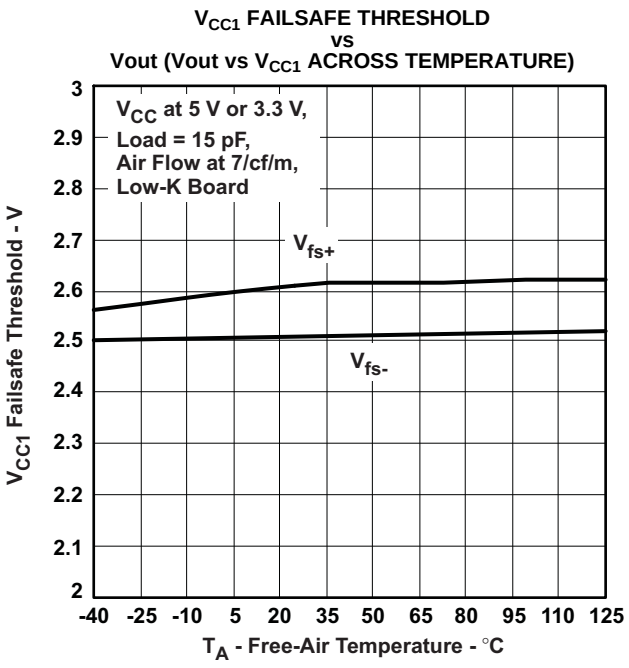


Figure 7.

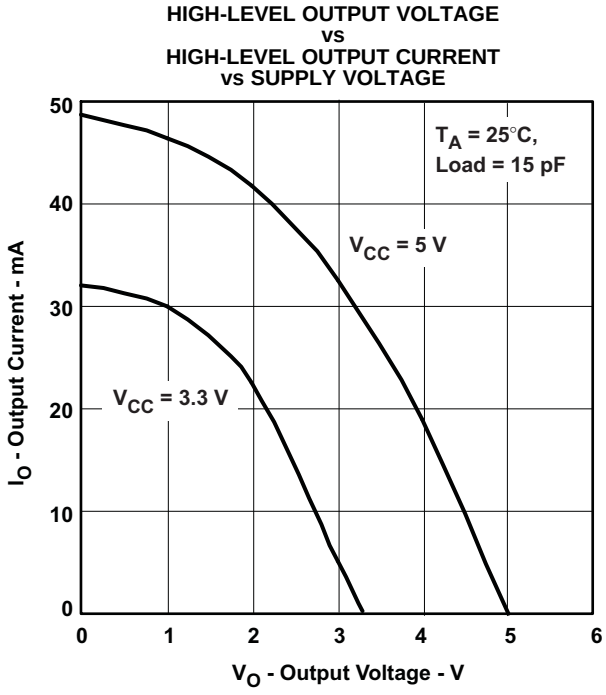


Figure 8.

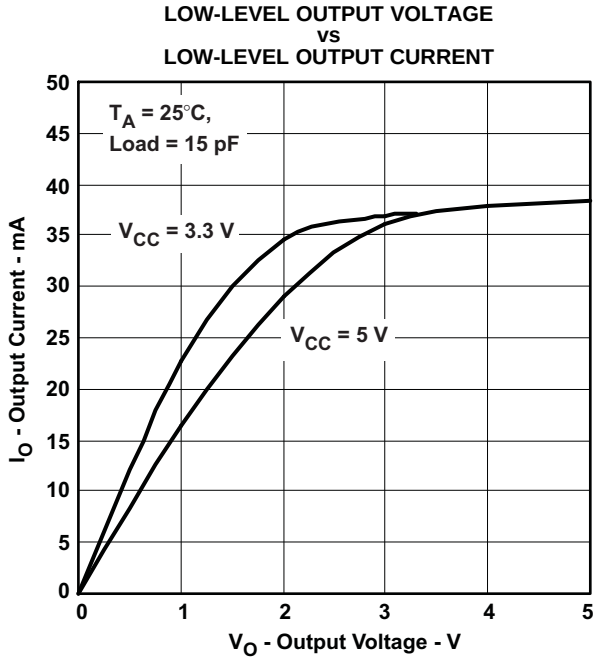
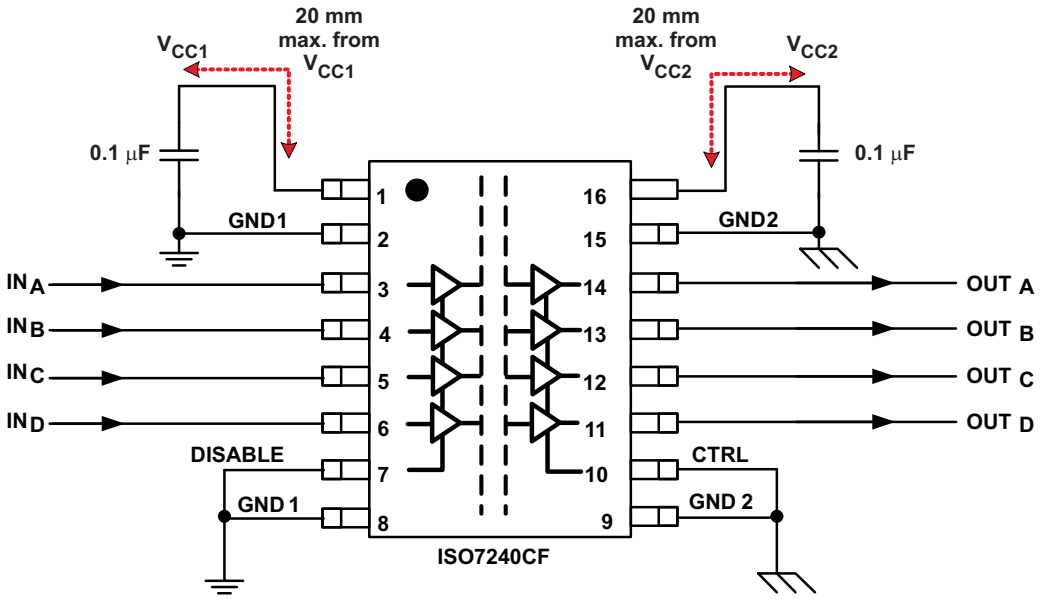


Figure 9.

APPLICATION INFORMATION



NOTE: It is recommended that the DISABLE pin not be left floating if unused in an application.

Figure 10. Typical ISO7240CF Failsafe-Low Application Circuit

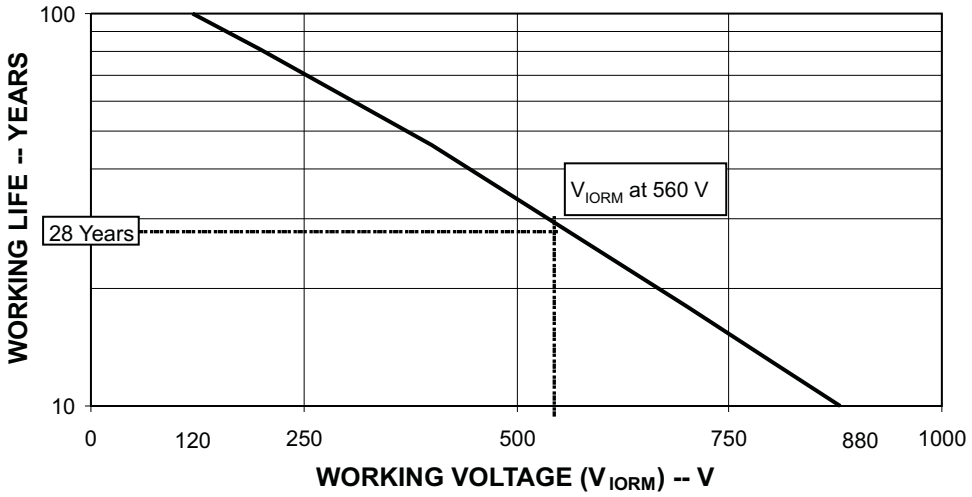


Figure 11. Time Dependent Dielectric Breakdown Test Results

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ISO7240CFDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7240CFDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7240CFDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7240CFDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

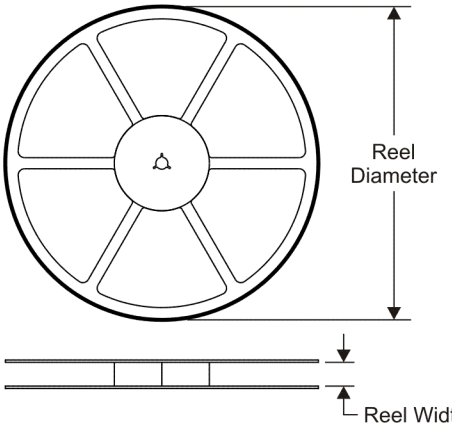
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

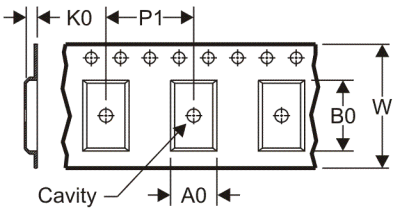
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

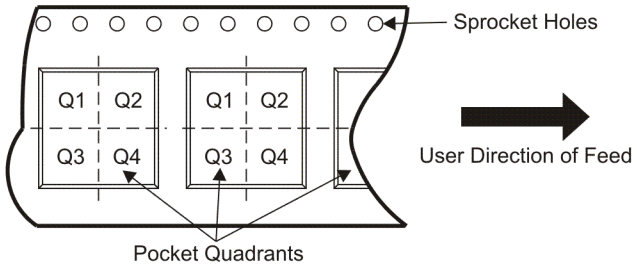


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

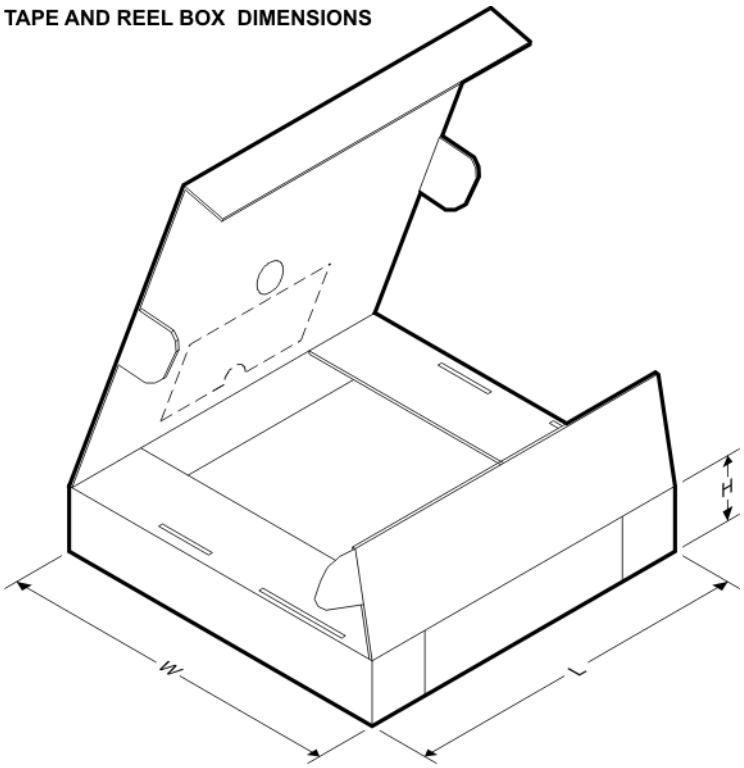
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7240CFDWR	SOIC	DW	16	2000	330.0	16.4	10.9	10.78	3.0	12.0	16.0	Q1

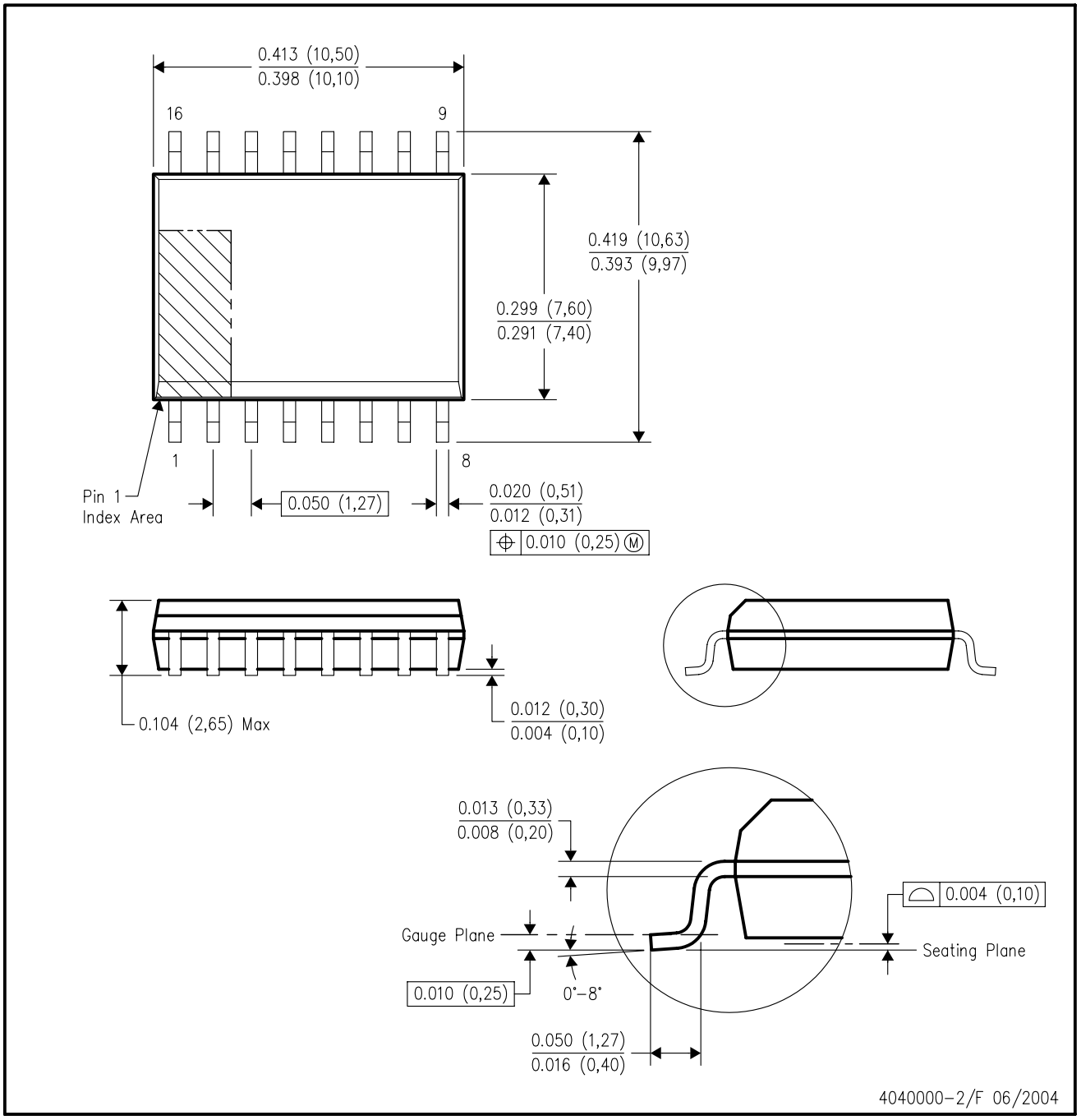
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7240CFDWR	SOIC	DW	16	2000	406.0	348.0	63.0

DW (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

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