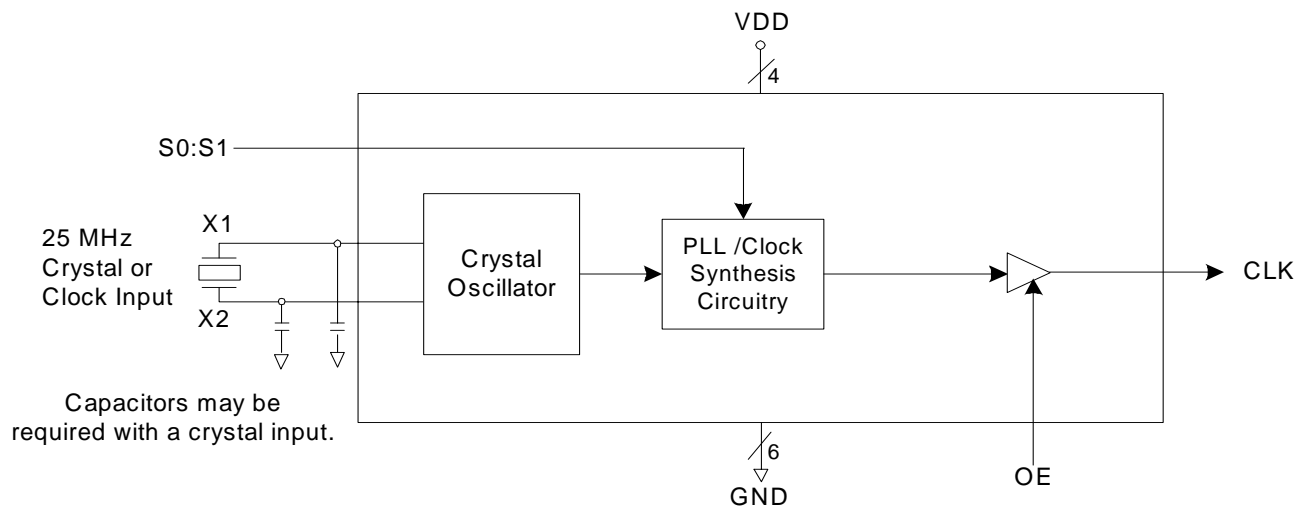## Description

The ICS426 was developed for serial ATA (SATA) and fiber channel. It generates a high quality, high frequency clock output from a low cost frequency crystal or clock input.

Using Phase-Locked-Loop (PLL) techniques, the device runs from a standard fundamental mode, inexpensive crystal or clock input.
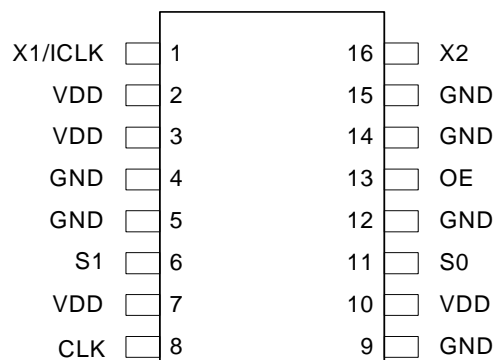
Features

- Packaged in 16 pin TSSOP
- Input crystal or clock frequency of 25 MHz (typical)
- Supports serial ATA Generation 1
- Supports Fiber Channel
- Duty cycle of 45/55
- Operating voltage of 3.3V
- Advanced, low power, CMOS process

Block Diagram

Pin Assignment

```
X1/ICLK  ⌷ 1        16 ⌷  X2
   VDD   ⌷ 2        15 ⌷  GND
   VDD   ⌷ 3        14 ⌷  GND
   GND   ⌷ 4        13 ⌷  OE
   GND   ⌷ 5        12 ⌷  GND
    S1   ⌷ 6        11 ⌷  S0
   VDD   ⌷ 7        10 ⌷  VDD
   CLK   ⌷ 8         9 ⌷  GND
```

16 pin 173 mil (0.65 mm) TSSOP

Clock Output Select Table (MHz)

S1	S0	Input	CLK Output
0	0	25	75
0	1	25	150
1	0	25	106.25
1	1	25	156.25

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1/ICLK	XI	Crystal connection. Connect to a 25 MHz fundamental mode crystal or clock input.
2	VDD	Power	Connect to +3.3 V.
3	VDD	Power	Connect to +3.3 V.
4	GND	Power	Connect to ground.
5	GND	Power	Connect to ground.
6	S1	Input	Select pin 1 determines CLK output based on table above. Internal pull-up.
7	VDD	Power	Connect to +3.3 V.
8	CLK	Output	Clock output. Tri-state output when OE is low.
9	GND	Power	Connect to ground.
10	VDD	Power	Connect to +3.3V.
11	S0	Input	Select pin 0 determines CLK output based on table above. Internal pull-up.
12	GND	Power	Connect to ground.
13	OE	Input	Output Enable. All outputs are tri-stated when low. Internal pull-up.
14	GND	Power	Connect to ground.
15	GND	Power	Connect to ground.
16	X2	XO	Crystal connection. Connect to a 25 MHz fundamental mode crystal or float for clock input.

External Components

Decoupling Capacitor

As with any high performance mixed-signal IC, the ICS426 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01µF must be connected between each VDD and the PCB ground plane.

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω.

Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors, if needed, must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal $(C_L -18pF)*2$. In this equation, C_L = crystal load capacitance in pF. Example: For a crystal with a 20 pF load capacitance, each crystal capacitor would be 4 pF $[(20-18) \times 2] = 20$.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitors should be mounted on the component side of the board as close to the VDD pins as possible. No vias should be used between the decoupling capacitors and VDD pins. The PCB trace to VDD pins should be kept as short as possible, as should the PCB trace to the ground via.

2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) To minimize EMI the 33Ω series termination resistor, if needed, should be placed close to the clock output.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the ICS426. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Phase Noise Graph

25 MHz crystal input, 106.25 MHz CLK output.

Phase Noise 106.25 MHz
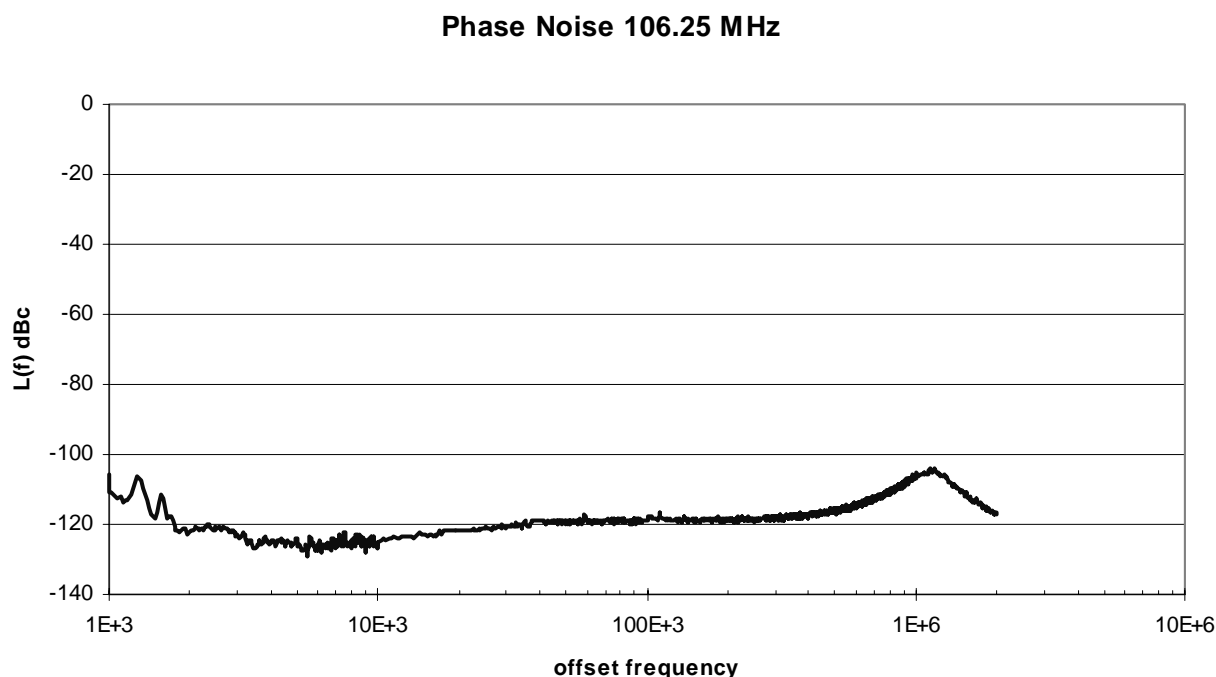
Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS426. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7V
All Inputs and Outputs	-0.5V to VDD+0.5V
Ambient Operating Temperature	0 to +70°C
Storage Temperature	-65 to +150°C
Junction Temperature	175°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.13	+3.3	+3.46	V

DC Electrical Characteristics

Unless stated otherwise, VDD = 3.3V ±5%, Ambient Temperature 0 to +70°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.13	3.3	3.47	V
Supply Current	IDD	No load		22		mA
Input High Voltage	V_{IH}	OE, S0, S1	2			V
Input Low Voltage	V_{IL}	OE, S0, S1			0.8	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12mA			0.4	V
Short Circuit Current	I_{OS}	CLK output		±50		mA
On Chip Pull-up Resistor	R_{PU}	OE, S0, S1		150		kΩ
Input Capacitance	C_{IN}	OE, S0, S1		5		pF

AC Electrical Characteristics

Unless stated otherwise, VDD = 3.3V ±5%, Ambient Temperature 0 to +70° C

| Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	F_{IN}	Crystal or clock input		25		MHz
Output Clock Duty Cycle		Measured at VDD/2, Note 1	45	50	55	%
Output Rise Time	t_{OR}	0.8 to 2.0V, Note 1		1		ns
Output Fall Time	t_{OF}	2.0 to 0.8V, Note 1		1		ns
Short Term Jitter		peak to peak, Note 1		±70		ps
Long Term Jitter		Measured over 1000 cycles; peak to peak, Note 1		170		ps
Phase Noise		106.25M CLK, relative to carrier, 100 Hz offset		-90		dBc/Hz
		106.25M CLK, relative to carrier, 1kHz offset		-115		dBc/Hz
		106.25M CLK, relative to carrier, 10 kHz offset		-121		dBc/Hz
		106.25M CLK, relative to carrier, 100 kHz offset		-116		dBc/Hz

Note 1: Measured with 15 pF load.

Package Outline and Package Dimensions (16 pin TSSOP, 173 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95
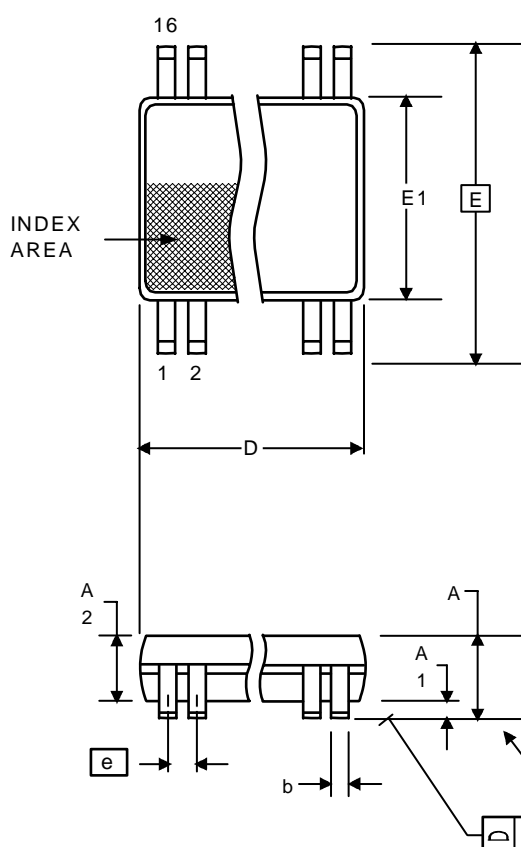
	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.1	0.193	0.201
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004
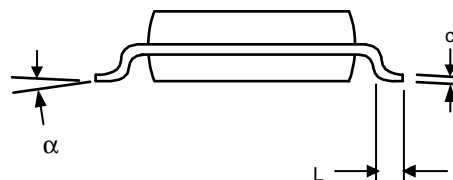
Ordering Information

Part / Order Number	Marking (both)	Shipping packaging	Package	Temperature
ICS426G	ICS426G	Tubes	16 pin TSSOP	0 to +70° C
ICS426GT	ICS426G	Tape and Reel	16 pin TSSOP	0 to +70° C