

32Meg x 16 512-MBIT DDR SDRAM

MARCH 2006

FEATURES

- Clock Frequency: 166 MHz
- Power supply (V_{DD} and V_{DDQ})
DDR 333: 2.5V $\pm$ 0.2V
- SSTL 2 interface
- Four internal banks to hide row Pre-charge and Active operations
- Commands and addresses register on positive clock edges (CK)
- Bi-directional Data Strobe signal for data capture
- Differential clock inputs (CK and $\overline{\text{CK}}$) for two data accesses per clock cycle
- Data Mask feature for Writes supported
- DLL aligns data I/O and Data Strobe transitions with clock inputs
- Programmable burst length for Read and Write operations
- Programmable CAS Latency (2 or 2.5 clocks)
- Programmable burst sequence: sequential or interleaved
- Burst concatenation and truncation supported for maximum data throughput
- Auto Pre-charge option for each Read or Write burst
- 8192 refresh cycles every 64ms
- Auto Refresh and Self Refresh Modes
- Pre-charge Power Down and Active Power Down Modes
- Lead-free package

DEVICE OVERVIEW

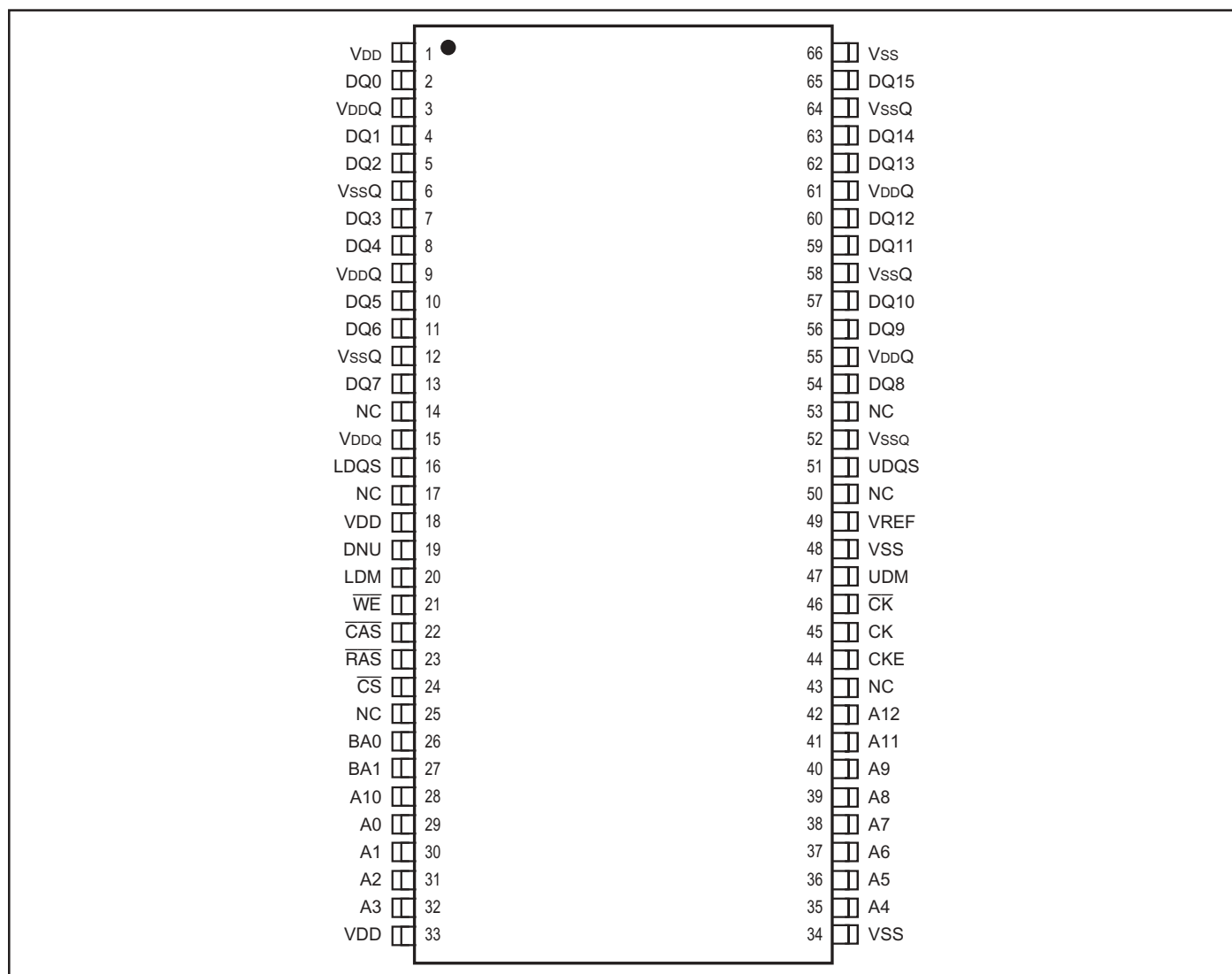
ISSI's 512-Mbit DDR SDRAM achieves high-speed data transfer using pipeline architecture and two data word accesses per clock cycle. The 536,870,912-bit memory array is internally organized as four banks of 128M-bit to allow concurrent operations. The pipeline allows Read and Write burst accesses to be virtually continuous, with the option to concatenate or truncate the bursts. The programmable features of burst length, burst sequence and CAS latency enable further advantages. The device is available in 16-bit data word size. Input data is registered on the I/O pins on both edges of Data Strobe signal(s), while output data is referenced to both edges of Data Strobe and both edges of CK. Commands are registered on the positive edges of CK. Auto Refresh, Active Power Down, and Pre-charge Power Down modes are enabled by using clock enable (CKE) and other inputs in an industry-standard sequence. All input and output voltage levels are compatible with SSTL 2.

KEY TIMING PARAMETERS

Parameter	-6	Unit
DDR333		
Clock Cycle Time		
$\overline{\text{CAS}}$ Latency = 3	—	ns
$\overline{\text{CAS}}$ Latency = 2.5	6	ns
$\overline{\text{CAS}}$ Latency = 2	7.5	ns
Clock Frequency		
$\overline{\text{CAS}}$ Latency = 3	—	MHz
$\overline{\text{CAS}}$ Latency = 2.5	166	MHz
$\overline{\text{CAS}}$ Latency = 2	133	MHz

PIN CONFIGURATIONS

66 pin TSOP - Type II for x16

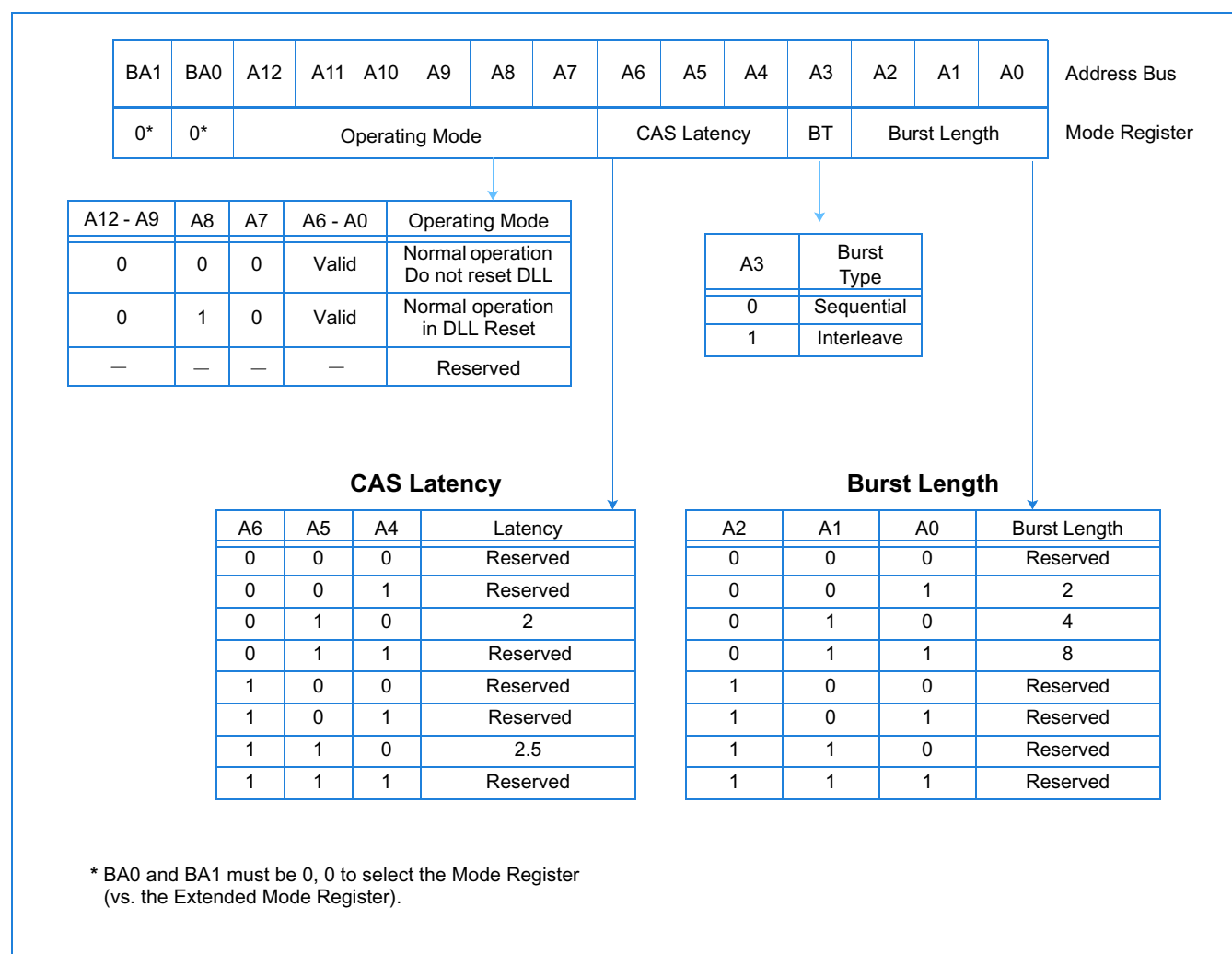


PIN DESCRIPTIONS

A0-A12	Row Address Input
A0-A9	Column Address Input
BA0, BA1	Bank Select Address
DQ0 to DQ15	Data I/O
CK, $\overline{CK}$	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe Command
$\overline{CAS}$	Column Address Strobe Command

$\overline{WE}$	Write Enable
LDM, UDM	x16 Input Mask
LDQS, UDQS	Data Strobe
VDD	Power
Vss	Ground
VDDQ	Power Supply for I/O Pin
VssQ	Ground for I/O Pin
VREF	Input Reference Voltage
DNU	Do Not Use
NC	No Connection

Mode Register Operation



Burst Definition

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
	A2	A1	A0	Type = Sequential	Type = Interleaved
2			0	0-1	0-1
			1	1-0	1-0
4		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

Notes:

1. For a burst length of two, A1-A i selects the two-data-element block; A0 selects the first access within the block.
2. For a burst length of four, A2-A i selects the four-data-element block; A0-A1 selects the first access within the block.
3. For a burst length of eight, A3-A i selects the eight-data- element block; A0-A2 selects the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3. The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in *Burst Definition*.

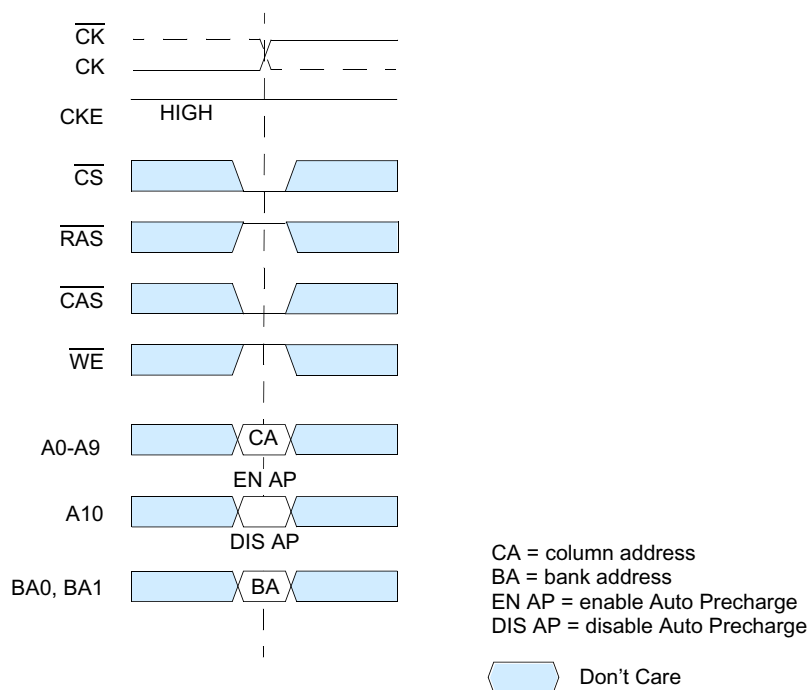
Read Latency

The Read latency, or CAS latency, is the delay, in clock cycles, between the registration of a Read command and the availability of the first burst of output data. The latency can be programmed 2 or 2.5 clocks for DDR333.

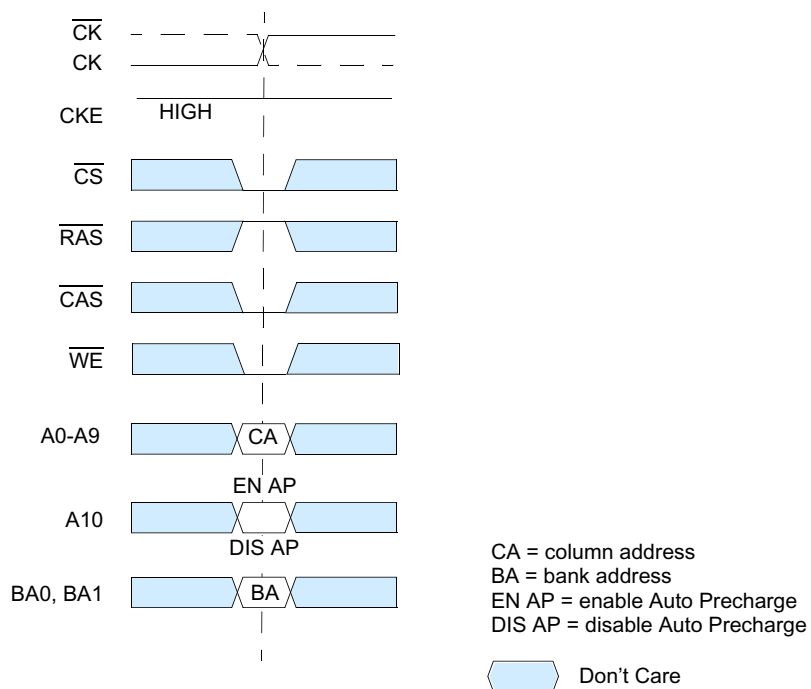
If a Read command is registered at clock edge n , and the latency is m clocks, the data is available nominally coincident with clock edge $n + m$.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Read Command



Write Command



Capacitance

Parameter	Symbol	Min.	Max.	Units	Notes
Input Capacitance: CK, $\overline{\text{CK}}$	Cl_1	2.0	3.0	pF	1
Delta Input Capacitance: CK, $\overline{\text{CK}}$	delta Cl_1		0.25	pF	1
Input Capacitance: All other input-only pins (except DM)	Cl_2	2.0	3.0	pF	1
Delta Input Capacitance: All other input-only pins (except DM)	delta Cl_2		0.5	pF	1
Input/Output Capacitance: DQ, DQS, DM	C_{IO}	4.0	5.0	pF	1, 2
Delta Input/Output Capacitance: DQ, DQS, DM	delta C_{IO}		0.5	pF	1

1. $V_{\text{DDQ}} = V_{\text{DD}} = 2.5\text{V} \pm 0.2\text{V}$ (minimum range to maximum range), $f = 100\text{MHz}$, $T_{\text{A}} = 25^\circ\text{C}$, $V_{\text{O}_{\text{DC}}} = V_{\text{DDQ}/2}$, $V_{\text{O}_{\text{Peak}} - \text{Peak}} = 0.2\text{V}$.
 2. Although DM is an input-only pin, the input capacitance of this pin must model the input capacitance of the DQ and DQS pins. This is required to match input propagation times of DQ, DQS and DM in the system.

DC Electrical Characteristics and Operating Conditions

($0^\circ\text{C} \leq T_{\text{A}} \leq 70^\circ\text{C}$; $V_{\text{DDQ}} = V_{\text{DD}} = \pm 2.5\text{V} \pm 0.2\text{V}$ (DDR333); see AC Characteristics)

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	Supply Voltage DDR333	2.3	2.7	V	1
V_{DDQ}	I/O Supply Voltage DDR333	2.3	2.7	V	1
$V_{\text{SS}}, V_{\text{SSQ}}$	Supply Voltage I/O Supply Voltage	0	0	V	
V_{REF}	I/O Reference Voltage	$0.49 \times V_{\text{DDQ}}$	$0.51 \times V_{\text{DDQ}}$	V	1, 2
V_{TT}	I/O Termination Voltage (System)	$V_{\text{REF}} - 0.04$	$V_{\text{REF}} + 0.04$	V	1, 3
$V_{\text{IH(DC)}}$	Input High (Logic1) Voltage	$V_{\text{REF}} + 0.15$	$V_{\text{DDQ}} + 0.3$	V	1
$V_{\text{IL(DC)}}$	Input Low (Logic0) Voltage	-0.3	$V_{\text{REF}} - 0.15$	V	1
$V_{\text{IN(DC)}}$	Input Voltage Level, CK and $\overline{\text{CK}}$ Inputs	-0.3	$V_{\text{DDQ}} + 0.3$	V	1
$V_{\text{ID(DC)}}$	Input Differential Voltage, CK and $\overline{\text{CK}}$ Inputs	0.30	$V_{\text{DDQ}} + 0.6$	V	1, 4
$V_{\text{IX(DC)}}$	Input Crossing Point Voltage, CK and $\overline{\text{CK}}$ Inputs	0.30	$V_{\text{DDQ}} + 0.6$	V	1, 4
$V_{\text{I Ratio}}$	V-I Matching Pullup Current to Pulldown Current Ratio	0.71	1.4		5
I_{I}	Input Leakage Current Any input $0\text{V} \leq V_{\text{IN}} \leq V_{\text{DD}}$; (All other pins not under test = 0V)	-2	2	μA	1
I_{OZ}	Output Leakage Current (DQs are disabled; $0\text{V} \leq V_{\text{out}} \leq V_{\text{DDQ}}$)	-5	5	μA	1

1. Inputs are not recognized as valid until V_{REF} stabilizes.
 2. V_{REF} is expected to be equal to $0.5 V_{\text{DDQ}}$ of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed $\pm 2\%$ of the DC value.
 3. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} , and must track variations in the DC level of V_{REF} .
 4. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{\text{CK}}$.
 5. The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages for 0.25 volts to 1.0 volts. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.

DC Electrical Characteristics and Operating Conditions

(0°C ≤ T_A ≤ 70°C; V_{DDQ} = V_{DD} = ± 2.5V ± 0.2V (DDR333); see AC Characteristics)

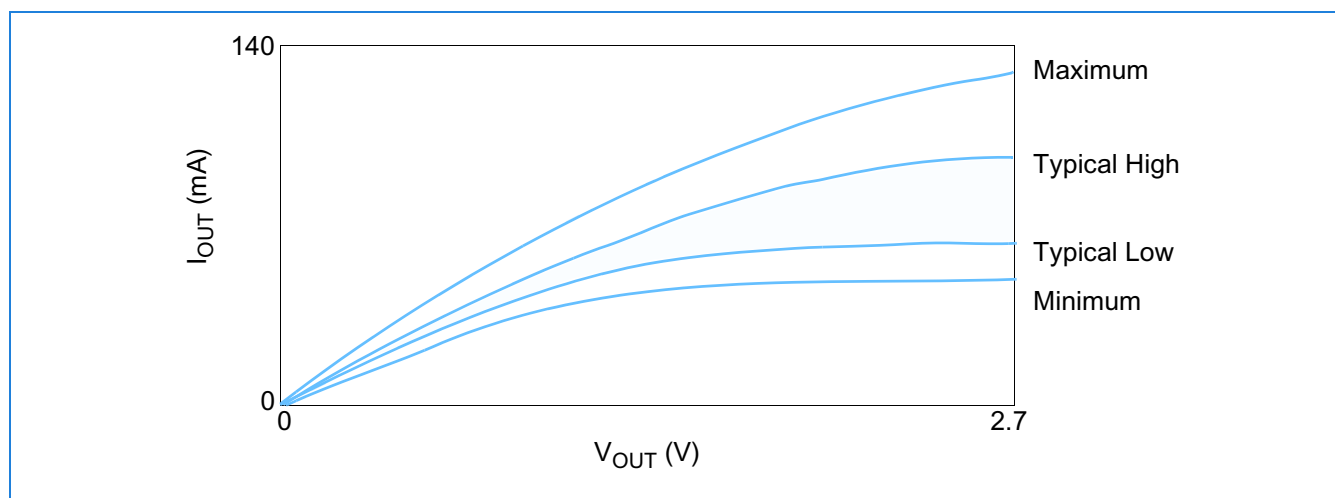
Symbol	Parameter	Min	Max	Units	Notes
I _{OH}	Output Current: Nominal Strength Driver High current (V _{OUT} = V _{DDQ} - 0.373V, min V _{REF} , min V _{TT})	- 16.8		mA	1
I _{OL}	Low current (V _{OUT} = 0.373V, max V _{REF} , max V _{TT})	16.8			
I _{OHW}	Output Current: Half- Strength Driver High current (V _{OUT} = V _{DDQ} - 0.763V, min V _{REF} , min V _{TT})	- 9.0		mA	1
I _{OLW}	Low current (V _{OUT} = 0.763V, max V _{REF} , max V _{TT})	9.0			

- Inputs are not recognized as valid until V_{REF} stabilizes.
- V_{REF} is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed ± 2% of the DC value.
- V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
- V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{\text{CK}}$.
- The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages for 0.25 volts to 1.0 volts. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.

Normal Strength Driver Pulldown and Pullup Characteristics

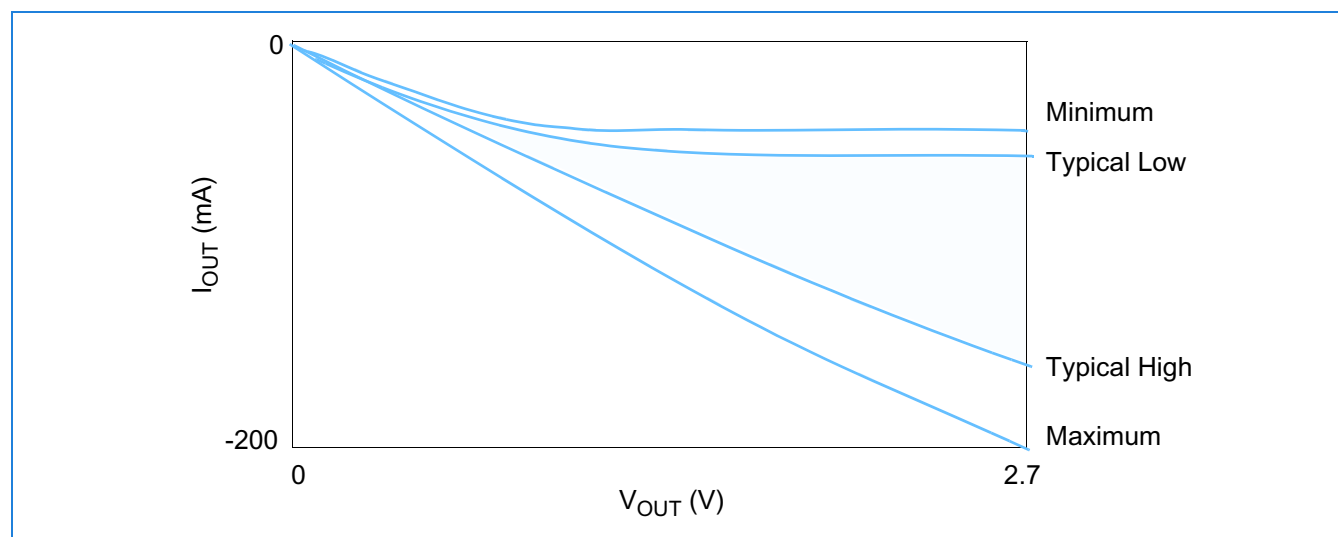
- The full variation in driver pulldown current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve.
- It is recommended that the “typical” IBIS pulldown V-I curve lie within the shaded region of the V-I curve.

Normal Strength Driver Pulldown Characteristics



- The full variation in driver pullup current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve.
- It is recommended that the “typical” IBIS pullup V-I curve lie within the shaded region of the V-I curve.

Normal Strength Driver Pullup Characteristics



5. The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1.7, for device drain to source voltages from 0.1 to 1.0.
6. The full variation in the ratio of the "typical" IBIS pullup to "typical" IBIS pulldown current should be unity $\pm$ 10%, for device drain to source voltages from 0.1 to 1.0. This specification is a design objective only. It is not guaranteed.
7. These characteristics are intended to obey the SSTL_2 class II standard.
8. This specification is intended for DDR SDRAM only.

Normal Strength Driver Pulldown and Pullup Currents

Voltage (V)	Pulldown Current (mA)				Pullup Current (mA)			
	Typical Low	Typical High	Min	Max	Typical Low	Typical High	Min	Max
0.1	6.0	6.8	4.6	9.6	-6.1	-7.6	-4.6	-10.0
0.2	12.2	13.5	9.2	18.2	-12.2	-14.5	-9.2	-20.0
0.3	18.1	20.1	13.8	26.0	-18.1	-21.2	-13.8	-29.8
0.4	24.1	26.6	18.4	33.9	-24.0	-27.7	-18.4	-38.8
0.5	29.8	33.0	23.0	41.8	-29.8	-34.1	-23.0	-46.8
0.6	34.6	39.1	27.7	49.4	-34.3	-40.5	-27.7	-54.4
0.7	39.4	44.2	32.2	56.8	-38.1	-46.9	-32.2	-61.8
0.8	43.7	49.8	36.8	63.2	-41.1	-53.1	-36.0	-69.5
0.9	47.5	55.2	39.6	69.9	-43.8	-59.4	-38.2	-77.3
1.0	51.3	60.3	42.6	76.3	-46.0	-65.5	-38.7	-85.2
1.1	54.1	65.2	44.8	82.5	-47.8	-71.6	-39.0	-93.0
1.2	56.2	69.9	46.2	88.3	-49.2	-77.6	-39.2	-100.6
1.3	57.9	74.2	47.1	93.8	-50.0	-83.6	-39.4	-108.1
1.4	59.3	78.4	47.4	99.1	-50.5	-89.7	-39.6	-115.5
1.5	60.1	82.3	47.7	103.8	-50.7	-95.5	-39.9	-123.0
1.6	60.5	85.9	48.0	108.4	-51.0	-101.3	-40.1	-130.4
1.7	61.0	89.1	48.4	112.1	-51.1	-107.1	-40.2	-136.7
1.8	61.5	92.2	48.9	115.9	-51.3	-112.4	-40.3	-144.2
1.9	62.0	95.3	49.1	119.6	-51.5	-118.7	-40.4	-150.5
2.0	62.5	97.2	49.4	123.3	-51.6	-124.0	-40.5	-156.9
2.1	62.9	99.1	49.6	126.5	-51.8	-129.3	-40.6	-163.2
2.2	63.3	100.9	49.8	129.5	-52.0	-134.6	-40.7	-169.6
2.3	63.8	101.9	49.9	132.4	-52.2	-139.9	-40.8	-176.0
2.4	64.1	102.8	50.0	135.0	-52.3	-145.2	-40.9	-181.3
2.5	64.6	103.8	50.2	137.3	-52.5	-150.5	-41.0	-187.6
2.6	64.8	104.6	50.4	139.2	-52.7	-155.3	-41.1	-192.9
2.7	65.0	105.4	50.5	140.8	-52.8	-160.1	-41.2	-198.2

Normal Strength Driver Evaluation Conditions

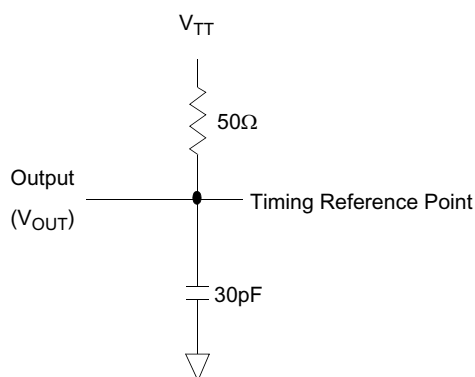
	Typical	Minimum	Maximum
Temperature (T_{ambient})	25 °C	70 °C	0 °C
V_{DDQ}	2.5V	2.3V	2.7V
Process conditions	typical process	slow-slow process	fast-fast process

AC Characteristics

(Notes 1-5 apply to the following Tables; Electrical Characteristics and DC Operating Conditions, AC Operating Conditions, I_{DD} Specifications and Conditions, and Electrical Characteristics and AC Timing.)

1. All voltages referenced to V_{SS} .
2. Tests for AC timing, I_{DD} , and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load. Refer to the AC Output Load Circuit below.
4. AC timing and I_{DD} tests may use a V_{IL} to V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK , $\overline{CK}$), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1V/ns in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver effectively switches as a result of the signal crossing the AC input level, and remains in that state as long as the signal does not ring back above (below) the DC input low (high) level.

AC Output Load Circuit Diagrams



AC Input Operating Conditions(0 °C ≤ T_A ≤ 70°C V_{DD} = V_{DDQ} = 2.5V ± 0.2V (DDR333); See AC Characteristics)

Symbol	Parameter/Condition	Min	Max	Unit	Notes
V _{IH(AC)}	Input High (Logic 1) Voltage, DQ, DQS, and DM Signals	V _{REF} + 0.31		V	1, 2
V _{IL(AC)}	Input Low (Logic 0) Voltage, DQ, DQS, and DM Signals		V _{REF} - 0.31	V	1, 2
V _{ID(AC)}	Input Differential Voltage, CK and $\overline{\text{CK}}$ Inputs	0.62	V _{DDQ} + 0.6	V	1, 2, 3
V _{IX(AC)}	Input Crossing Point Voltage, CK and $\overline{\text{CK}}$ Inputs	0.5*V _{DDQ} - 0.2	0.5*V _{DDQ} + 0.2	V	1, 2, 4

1. Input slew rate = 1V/ns
2. Inputs are not recognized as valid until V_{REF} stabilizes.
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{\text{CK}}$.
4. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

I_{DD} Specifications and Conditions(0 °C ≤ T_A ≤ 70°C V_{DD} = V_{DDQ} = 2.5V ± 0.2V (DDR333); See AC Characteristics)

Symbol	Parameter/Condition	DDR333 (6K) t _{CK} =6ns	Unit	Notes
I _{DD0}	Operating Current: one bank; active / precharge; t _{RC} = t _{RC} (min); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	96	mA	1
I _{DD1}	Operating Current: one bank; active / read / precharge; Burst = 2; t _{RC} = t _{RC} (min); CL = 2.5; I _{OUT} = 0mA; address and control inputs changing once per clock cycle	99	mA	1
I _{DD2P}	Precharge Power Down Standby Current: all banks idle; Power Down mode; CKE ≤ V _{IL} (max)	5	mA	1
I _{DD2N}	Idle Standby Current: $\overline{\text{CS}} \geq V_{IH}$ (min); all banks idle; CKE ≥ V _{IH} (min); address and control inputs changing once per clock cycle	25	mA	1
I _{DD3P}	Active Power Down Standby Current: one bank active; Power Down mode; CKE ≤ V _{IL} (max)	11	mA	1
I _{DD3N}	Active Standby Current: one bank; active / precharge; $\overline{\text{CS}} \geq V_{IH}$ (min); CKE ≥ V _{IH} (min); t _{RC} = t _{RAS} (max); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	45	mA	1
I _{DD4R}	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; I _{OUT} = 0mA	104	mA	1
I _{DD4W}	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL = 2.5	117	mA	1
I _{DD5}	Auto-Refresh Current: t _{RC} = t _{RFC} (min)	193	mA	1
I _{DD6}	Self-Refresh Current: CKE ≤ 0.2V	5	mA	1, 2
I _{DD7}	Operating current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; t _{RC} = t _{RC} (min); I _{OUT} = 0mA.	307	mA	1

1. I_{DD} specifications are tested after the device is properly initialized.
2. Enables on-chip refresh and address counters.
Values are averaged from high and low temp values using x16 devices.

Electrical Characteristics & AC Timing - Absolute Specifications

(0 °C ≤ T_A ≤ 70 °C V_{DD} = V_{DDQ} = 2.5V ± 0.2V (DDR333); See AC Characteristics)

Symbol	Parameter		DDR333 (6K)		Unit	Notes
			Min	Max		
t _{AC}	DQ output access time from CK/ $\overline{\text{CK}}$		-0.7	+0.7	ns	1-4
t _{DQSCK}	DQS output access time from CK/ $\overline{\text{CK}}$		-0.6	+0.6	ns	1-4
t _{CH}	CK high-level width		0.45	0.55	t _{CK}	1-4
t _{CL}	CK low-level width		0.45	0.55	t _{CK}	1-4
t _{CK}	Clock cycle time	CL = 3.0			ns	1-4
		CL = 2.5	6	12	ns	1-4
		CL = 2.0	7.5	12	ns	1-4
t _{DH}	DQ and DM input hold time		0.45		ns	1-4, 15, 16
t _{DS}	DQ and DM input setup time		0.45		ns	1-4, 15, 16
t _{IPW}	Input pulse width		2.2		ns	2-4, 12
t _{DIPW}	DQ and DM input pulse width (each input)		1.75		ns	1-4
t _{HZ}	Data-out high-impedance time from CK/ $\overline{\text{CK}}$		-0.7	+0.7	ns	1-4, 5
t _{LZ}	Data-out low-impedance time from CK/ $\overline{\text{CK}}$		-0.7	+0.7	ns	1-4, 5
t _{DQSQ}	DQS-DQ skew (DQS & associated DQ signals)	TSOP Package		+0.45	ns	1-4
		BGA Package		+0.4	ns	1-4
t _{HP}	Minimum half clk period for any given cycle; defined by clk high (t _{CH}) or clk low (t _{CL}) time		min (t _{CL} , t _{CH})		t _{CK}	1-4
t _{QH}	Data output hold time from DQS		t _{HP} - t _{QHS}		t _{CK}	1-4
t _{QHS}	Data hold Skew Factor	TSOP Package		0.55	t _{CK}	1-4
		BGA Package		0.5	t _{CK}	1-4
t _{DQSS}	Write command to 1st DQS latching transition		0.75	1.25	t _{CK}	1-4
t _{DQSH}	DQS input high pulse width (write cycle)		0.35		t _{CK}	1-4
t _{DQSL}	DQS input low pulse width (write cycle)		0.35		t _{CK}	1-4
t _{DSS}	DQS falling edge to CK setup time (write cycle)		0.2		t _{CK}	1-4
t _{DSH}	DQS falling edge hold time from CK (write cycle)		0.2		t _{CK}	1-4
t _{MRD}	Mode register set command cycle time		2		t _{CK}	1-4
t _{WPRES}	Write preamble setup time		0		ns	1-4, 7
t _{WPST}	Write postamble		0.40	0.60	t _{CK}	1-4, 6
t _{WPRES}	Write preamble		0.25		t _{CK}	1-4
t _{IH}	Address and control input hold time (fast slew rate)		0.75		ns	2-4, 9, 11, 12
t _{IS}	Address and control input setup time (fast slew rate)		0.75		ns	2-4, 9, 11, 12
t _{IH}	Address and control input hold time (slow slew rate)		0.8		ns	2-4, 10-12, 14
t _{IS}	Address and control input setup time (slow slew rate)		0.8		ns	2-4, 10, 11, 12, 14
t _{RPRES}	Read preamble		0.9	1.1	t _{CK}	1-4
t _{RPST}	Read postamble		0.40	0.60	t _{CK}	1-4

Electrical Characteristics & AC Timing - Absolute Specifications(0 °C ≤ T_A ≤ 70 °C V_{DD} = V_{DDQ} = 2.5V ± 0.2V (DDR333); See AC Characteristics)

Symbol	Parameter	DDR333 (6K)		Unit	Notes
		Min	Max		
t _{RAS}	Active to Precharge command	42	120,000	ns	1-4
t _{RC}	Active to Active/Auto-refresh command period	60		ns	1-4
t _{RFC}	Auto-refresh to Active/Auto-refresh command period	72		ns	1-4
t _{RCD}	Active to Read or Write delay	18		ns	1-4
t _{RAP}	Active to Read Command with Autoprecharge	min (t _{RCD} , t _{RAS})		ns	1-4
t _{RP}	Precharge command period	18		ns	1-4
t _{RRD}	Active bank A to Active bank B command	12		ns	1-4
t _{WR}	Write recovery time	15		ns	1-4
t _{DAL}	Auto precharge write recovery + precharge time	(t _{WR} /t _{CK}) + (t _{RP} /t _{CK})		t _{CK}	1-4, 13
t _{WTR}	Internal write to read command delay	1		t _{CK}	1-4
t _{PDEX}	Power down exit time	6		ns	1-4
t _{XSNR}	Exit self-refresh to non-read command	75		ns	1-4
t _{XSRD}	Exit self-refresh to read command	200		t _{CK}	1-4
t _{REFI}	Average Periodic Refresh Interval		7.8	us	1-4, 8

Electrical Characteristics & AC Timing - Absolute Specifications Notes

1. Input slew rate = 1V/ns.
2. The CK/ $\overline{\text{CK}}$ input reference level (for timing reference to CK/ $\overline{\text{CK}}$) is the point at which CK and $\overline{\text{CK}}$ cross; the input reference level for signals other than CK/ $\overline{\text{CK}}$ is V_{REF} .
3. Inputs are not recognized as valid until V_{REF} stabilizes.
4. The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (Note 3) is V_{TT} .
5. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
6. The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
7. The specific requirement is that DQS be valid (high, low, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from high to low at this time, depending on t_{DQSS} .
8. A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.
9. For command/address input slew rate $\geq 1.0\text{V/ns}$. Slew rate is measured between V_{OH} (AC) and V_{OL} (AC).
10. For command/address input slew rate $\geq 0.5\text{V/ns}$ and $< 1.0\text{V/ns}$. Slew rate is measured between V_{OH} (AC) and V_{OL} (AC).
11. CK/ $\overline{\text{CK}}$ slew rates are $\geq 1.0\text{V/ns}$.
12. These parameters guarantee device timing, but they are not necessarily tested on each device, and they may be guaranteed by design or tester characterization.
13. For each of the terms in parentheses, if not already an integer, round to the next highest integer. t_{CK} is equal to the actual system clock cycle time. For example, for DDR333 at CL = 2.5, $t_{\text{DAL}} = (15\text{ns}/6\text{ns}) + (18\text{ns}/6\text{ns}) = 3 + 3 = 6$.

14. An input setup and hold time derating table is used to increase t_{IS} and t_{IH} in the case where the input slew rate is below 0.5 V/ns.

Input Slew Rate	delta (t_{IS})	delta (t_{IH})	Unit	Notes
0.5 V/ns	0	0	ps	1,2
0.4 V/ns	+50	0	ps	1,2
0.3 V/ns	+100	0	ps	1,2

1. Input slew rate is based on the lesser of the slew rates determined by either $V_{IH}(AC)$ to $V_{IL}(AC)$ or $V_{IH}(DC)$ to $V_{IL}(DC)$, similarly for rising transitions.
2. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

15. An input setup and hold time derating table is used to increase t_{DS} and t_{DH} in the case where the I/O slew rate is below 0.5 V/ns.

Input Slew Rate	delta (t_{DS})	delta (t_{DH})	Unit	Notes
0.5 V/ns	0	0	ps	1,2
0.4 V/ns	+75	+75	ps	1,2
0.3 V/ns	+150	+150	ps	1,2

1. I/O slew rate is based on the lesser of the slew rates determined by either $V_{IH}(AC)$ to $V_{IL}(AC)$ or $V_{IH}(DC)$ to $V_{IL}(DC)$, similarly for rising transitions.
2. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

16. An I/O Delta Rise, Fall Derating table is used to increase t_{DS} and t_{DH} in the case where DQ, DM, and DQS slew rates differ.

Input Slew Rate	delta (t_{DS})	delta (t_{DH})	Unit	Notes
0.0 V/ns	0	0	ps	1,2,3,4
0.25 V/ns	+50	+50	ps	1,2,3,4
0.5 V/ns	+100	+100	ps	1,2,3,4

1. Input slew rate is based on the lesser of the slew rates determined by either $V_{IH}(AC)$ to $V_{IL}(AC)$ or $V_{IH}(DC)$ to $V_{IL}(DC)$, similarly for rising transitions.
2. Input slew rate is based on the larger of AC to AC delta rise, fall rate and DC to DC delta rise, fall rate.
3. The delta rise, fall rate is calculated as: $[1/(\text{slew rate 1})] - [1/(\text{slew rate 2})]$
 For example: slew rate 1 = 0.5 V/ns; slew rate 2 = 0.4 V/ns
 Delta rise, fall = $(1/0.5) - (1/0.4)$ [ns/V]
 = -0.5 ns/V
 Using the table above, this would result in an increase in t_{DS} and t_{DH} of 100 ps.
4. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

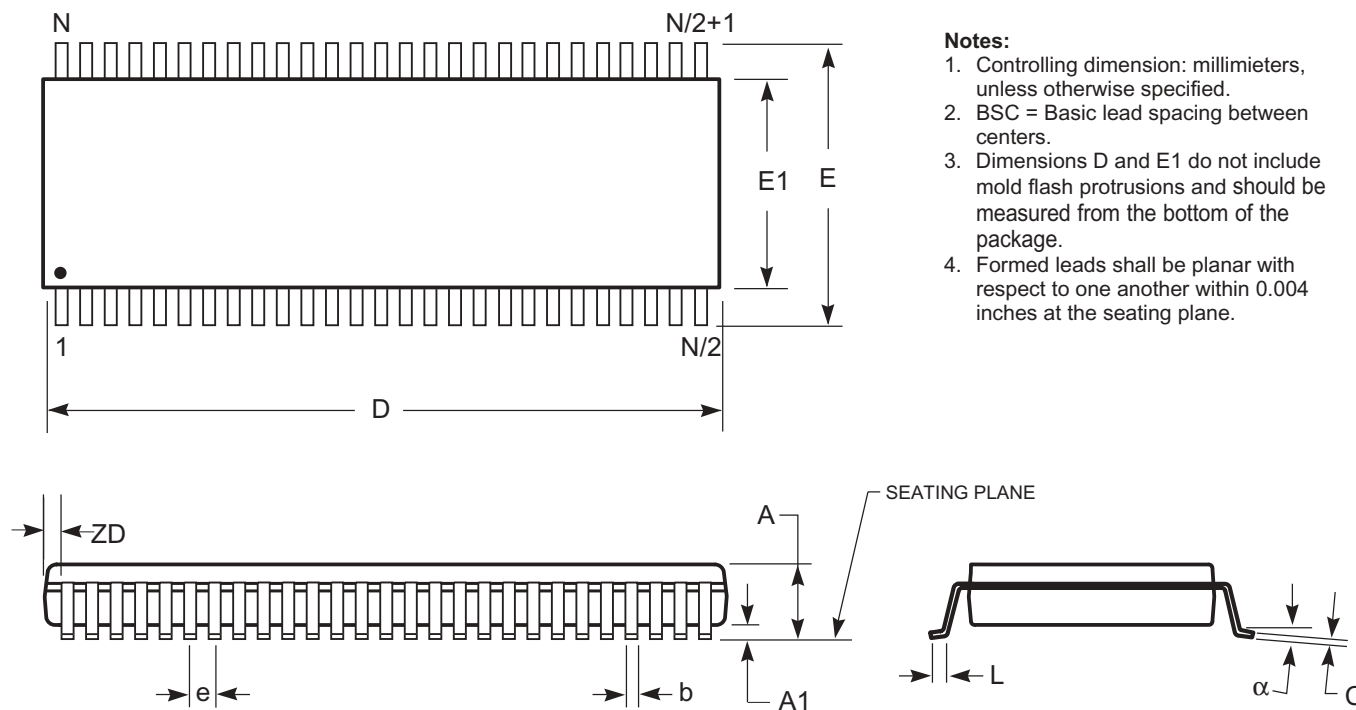
ORDERING INFORMATION**Commercial Range: 0°C to +70°C**

Frequency	Speed (ns)	Order Part No.	Package
166 MHz	6	IS43R16320A-6TL	66-pin TSOP-II, Lead-free

PACKAGING INFORMATION

Plastic TSOP 66-pin

Package Code: T (Type II)



Notes:

1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

Plastic TSOP (T - Type II)				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
Ref. Std.				
No. Leads (N)	66			
A	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006
A2	—	—	—	—
b	0.24	0.40	0.009	0.016
C	0.12	0.21	0.005	0.0083
D	22.02	22.42	0.867	0.8827
E1	10.03	10.29	0.395	0.405
E	11.56	11.96	0.455	0.471
e	0.65 BSC		0.026 BSC	
L	0.40	0.60	0.016	0.024
L1	—	—	—	—
ZD	0.71	REF	0.028	REF
α	0°	8°	0°	8°