

IRL3502PbF

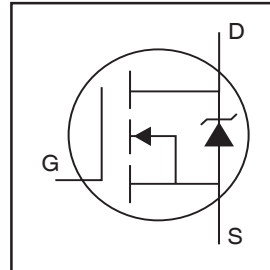
HEXFET® Power MOSFET

- Advanced Process Technology
- Optimized for 4.5V-7.0V Gate Drive
- Ideal for CPU Core DC-DC Converters
- Fast Switching
- Lead-Free

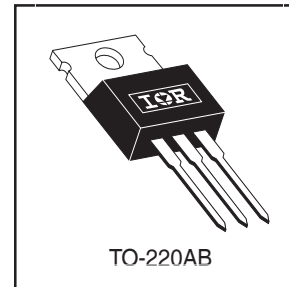
Description

These HEXFET Power MOSFETs were designed specifically to meet the demands of CPU core DC-DC converters in the PC environment. Advanced processing techniques combined with an optimized gate oxide design results in a die sized specifically to offer maximum efficiency at minimum cost.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



$V_{DS} = 20V$
$R_{DS(on)} = 0.007\Omega$
$I_D = 110A^{\textcircled{5}}$



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 5.0V$	110 ^⑤	A
$I_D @ T_C = 100^{\circ}C$	Continuous Drain Current, $V_{GS} @ 5.0V$	67	
I_{DM}	Pulsed Drain Current ①	420	
$P_D @ T_C = 25^{\circ}C$	Power Dissipation	140	W
	Linear Derating Factor	1.1	W/°C
V_{GS}	Gate-to-Source Voltage	± 10	V
V_{GSM}	Gate-to-Source Voltage (Start Up Transient, $t_p = 100\mu s$)	14	V
E_{AS}	Single Pulse Avalanche Energy ^②	390	mJ
I_{AR}	Avalanche Current ^①	64	A
E_{AR}	Repetitive Avalanche Energy ^①	14	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

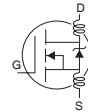
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.89	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	20	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.019	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.008	Ω	$V_{GS} = 4.5V, I_D = 64A$ ④
		—	—	0.007		$V_{GS} = 7.0V, I_D = 64A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	0.70	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	77	—	—	S	$V_{DS} = 10V, I_D = 64A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 20V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 10V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = -10V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = 10V$
Q_g	Total Gate Charge	—	—	110	nC	$I_D = 64A$
Q_{gs}	Gate-to-Source Charge	—	—	27		$V_{DS} = 16V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	39		$V_{GS} = 4.5V$, See Fig. 6 ④
$t_{d(on)}$	Turn-On Delay Time	—	10	—	ns	$V_{DD} = 10V$
t_r	Rise Time	—	140	—		$I_D = 64A$
$t_{d(off)}$	Turn-Off Delay Time	—	96	—		$R_G = 3.8\Omega, V_{GS} = 4.5V$
t_f	Fall Time	—	130	—		$R_D = 0.15\Omega$, ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	4700	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	1900	—		$V_{DS} = 15V$
C_{rss}	Reverse Transfer Capacitance	—	640	—		$f = 1.0\text{MHz}$, See Fig. 5



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	110	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	420		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 64A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	87	130	ns	$T_J = 25^\circ\text{C}, I_F = 64A$
Q_{rr}	Reverse Recovery Charge	—	200	310	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 190\mu H$
 $R_G = 25\Omega$, $I_{AS} = 64A$.
- ③ $I_{SD} \leq 64A$, $di/dt \leq 86A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ Calculated continuous current based on maximum allowable junction temperature; for recommended current-handling of the package refer to Design Tip # 93-4

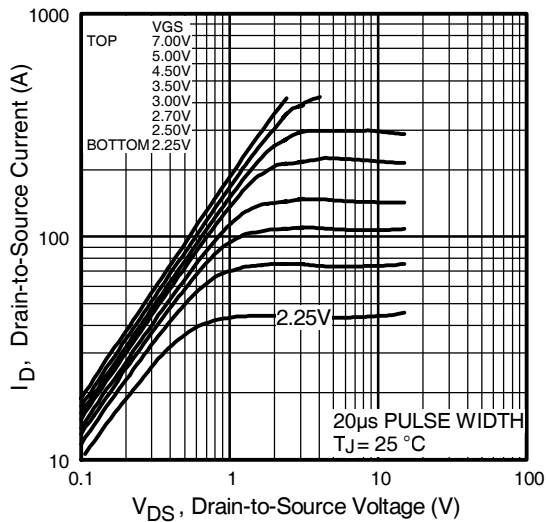


Fig 1. Typical Output Characteristics

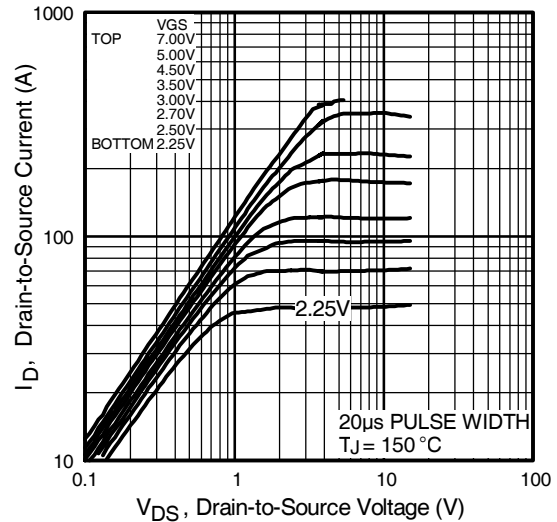


Fig 2. Typical Output Characteristics

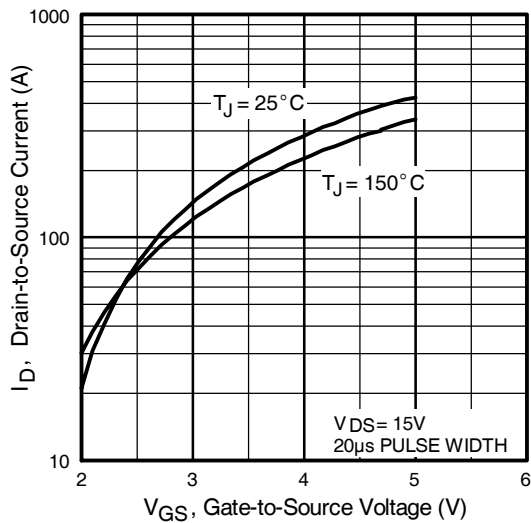


Fig 3. Typical Transfer Characteristics

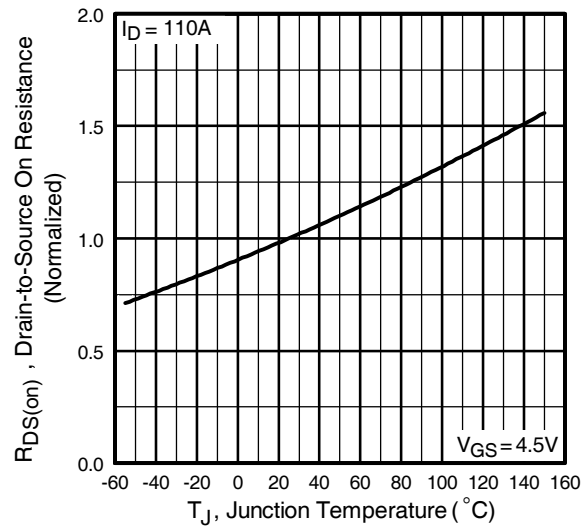


Fig 4. Normalized On-Resistance Vs. Temperature

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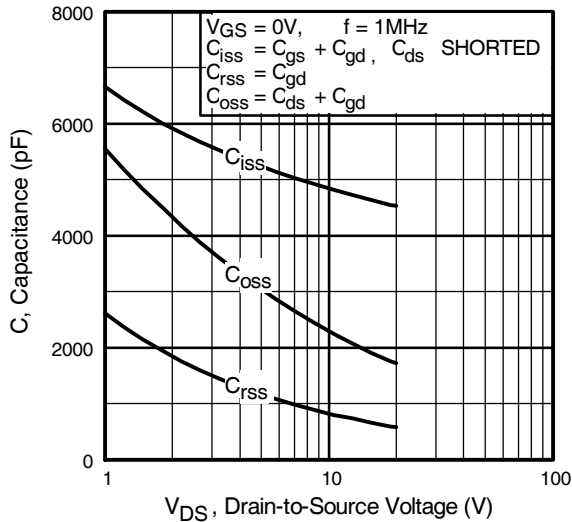


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

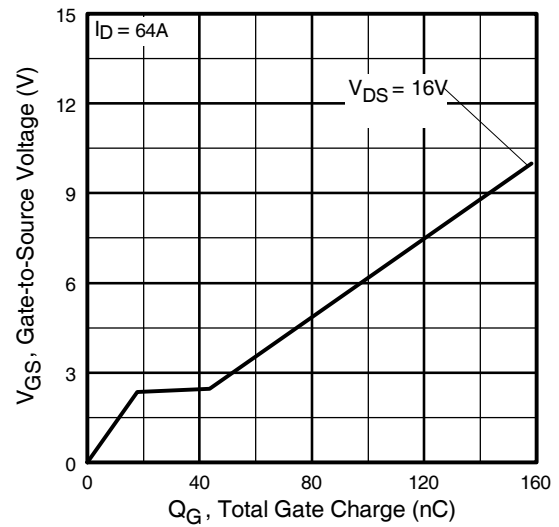


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

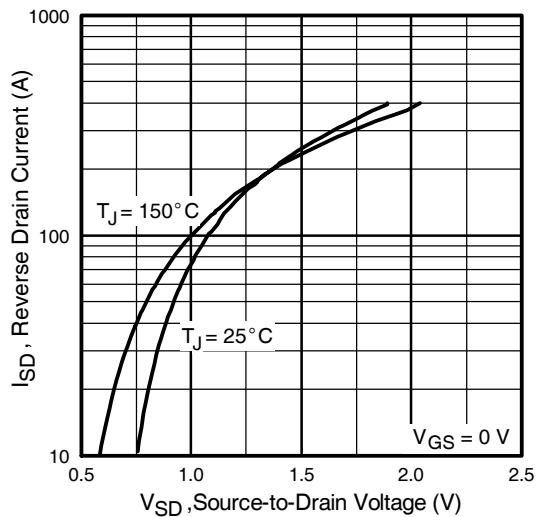


Fig 7. Typical Source-Drain Diode Forward Voltage

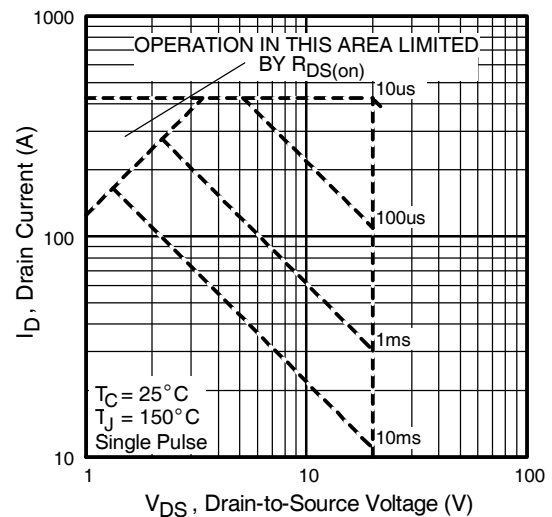


Fig 8. Maximum Safe Operating Area

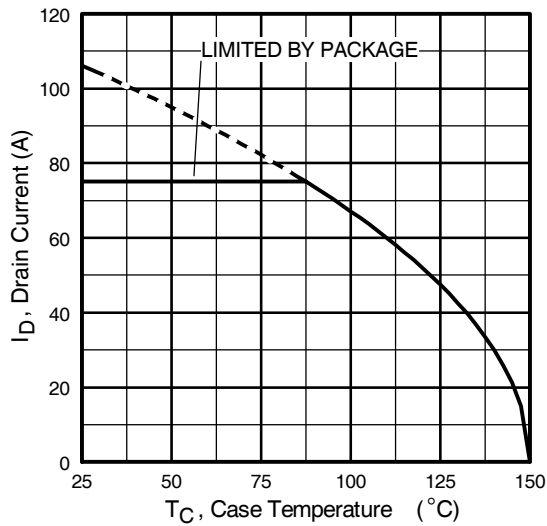


Fig 9. Maximum Drain Current Vs. Case Temperature

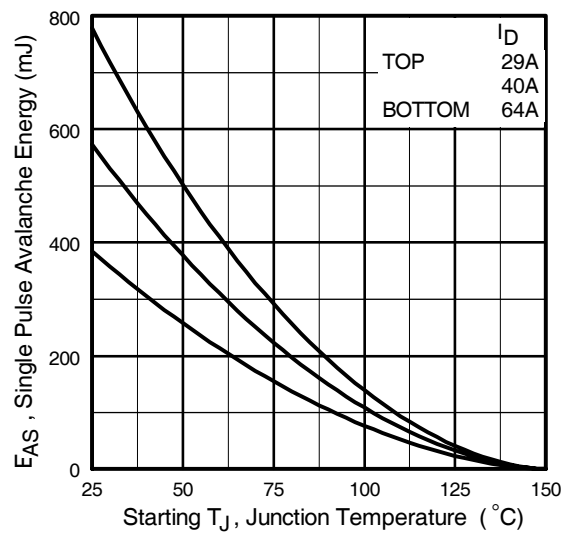


Fig 10. Maximum Avalanche Energy Vs. Drain Current

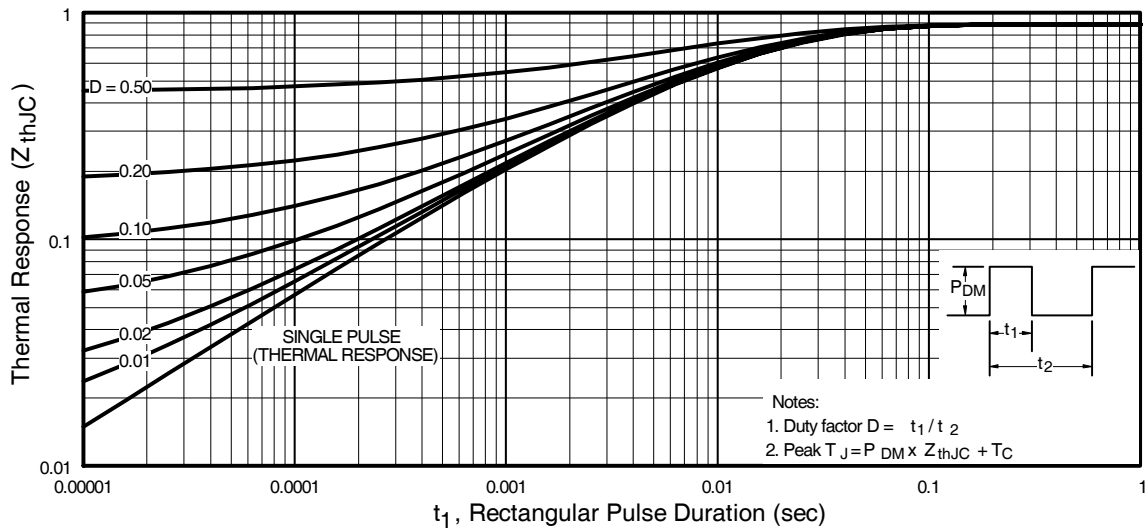


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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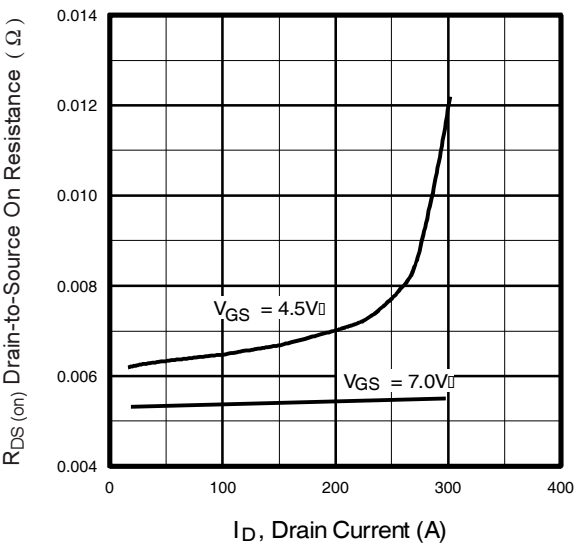


Fig 12. On-Resistance Vs. Drain Current

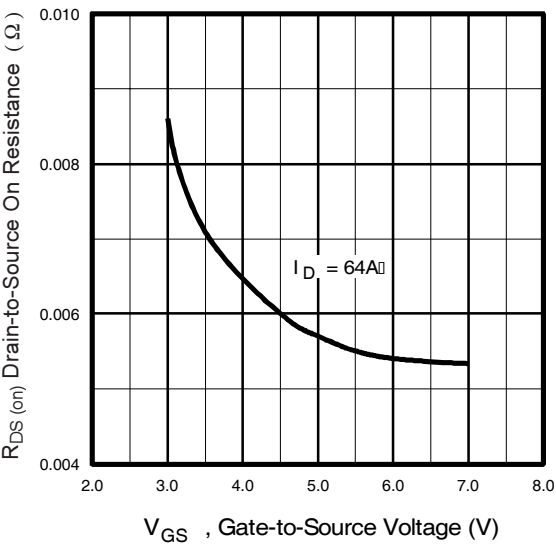
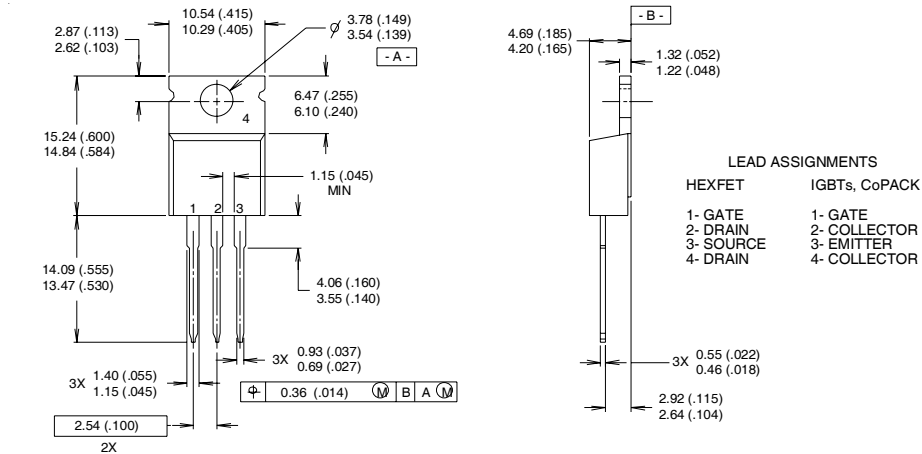


Fig 13. On-Resistance Vs. Gate Voltage

TO-220AB Package Outline

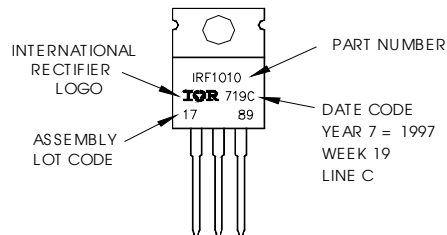
Dimensions are shown in millimeters (inches)



- NOTES:
- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
 - 2 CONTROLLING DIMENSION : INCH
 - 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
 - 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"
Note: "P" in assembly line
position indicates "Lead-Free"



Data and specifications subject to change without notice.

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