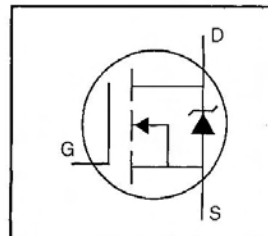


IRFR320PbF

IRFU320PbF

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Surface Mount (IRFR320)
- Straight Lead (IRFU320)
- Available in Tape & Reel
- Fast Switching
- Ease of Paralleling
- Lead-Free



$$V_{DS} = 400V$$

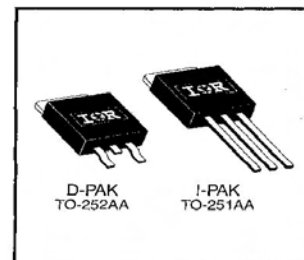
$$R_{DS(on)} = 1.8\Omega$$

$$I_D = 3.1A$$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D-Pak is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	3.1	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	2.0	
I_{DM}	Pulsed Drain Current ①	12	
$P_D @ T_C = 25^\circ C$	Power Dissipation	42	W
$P_D @ T_A = 25^\circ C$	Power Dissipation (PCB Mount)**	2.5	
	Linear Derating Factor	0.33	
	Linear Derating Factor (PCB Mount)**	0.020	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	160	mJ
I_{AR}	Avalanche Current ①	3.1	A
E_{AR}	Repetitive Avalanche Energy ①	4.2	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	260 (1.6mm from case)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	3.0	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)**	—	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	—	110	

** When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	400	—	—	V	$V_{GS}=0V$, $I_D=250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.51	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D=1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	1.8	Ω	$V_{GS}=10V$, $I_D=1.9A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
g_{fs}	Forward Transconductance	1.7	—	—	S	$V_{DS}=50V$, $I_D=1.9A$ ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS}=400V$, $V_{GS}=0V$
		—	—	250		$V_{DS}=320V$, $V_{GS}=0V$, $T_J=125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS}=20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS}=-20V$
Q_g	Total Gate Charge	—	—	20	nC	$I_D=3.3A$
Q_{gs}	Gate-to-Source Charge	—	—	3.3		$V_{DS}=320V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	11		$V_{GS}=10V$ See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	10	—	ns	$V_{DD}=200V$
t_r	Rise Time	—	14	—		$I_D=3.3A$
$t_{d(off)}$	Turn-Off Delay Time	—	30	—		$R_G=18\Omega$
t_f	Fall Time	—	13	—		$R_D=56\Omega$ See Figure 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	350	—	pF	$V_{GS}=0V$
C_{oss}	Output Capacitance	—	120	—		$V_{DS}=25V$
C_{rss}	Reverse Transfer Capacitance	—	47	—		$f=1.0\text{MHz}$ See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	3.1	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	12		
V_{SD}	Diode Forward Voltage	—	—	1.6	V	$T_J=25^\circ\text{C}$, $I_S=3.1A$, $V_{GS}=0V$ ④
t_{rr}	Reverse Recovery Time	—	270	600	ns	$T_J=25^\circ\text{C}$, $I_F=3.3A$
Q_{rr}	Reverse Recovery Charge	—	1.4	3.0	μC	$di/dt=100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② $V_{DD}=50V$, starting $T_J=25^\circ\text{C}$, $L=29\text{mH}$, $R_G=25\Omega$, $I_{AS}=3.1A$ (See Figure 12)
- ③ $I_{SD}\leq 3.1A$, $di/dt\leq 65A/\mu s$, $V_{DD}\leq V_{(BR)DSS}$, $T_J\leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

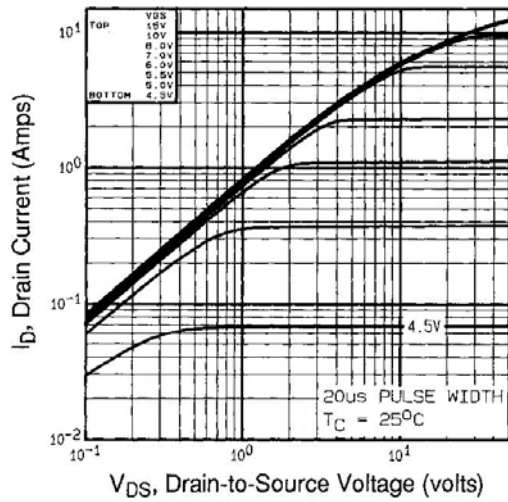


Fig 1. Typical Output Characteristics,
 $T_C=25^{\circ}\text{C}$

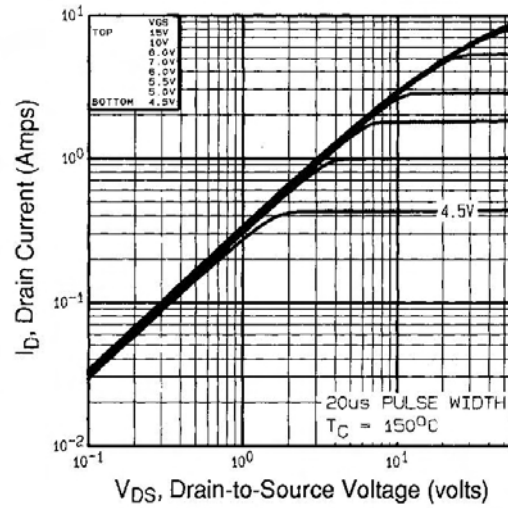


Fig 2. Typical Output Characteristics,
 $T_C=150^{\circ}\text{C}$

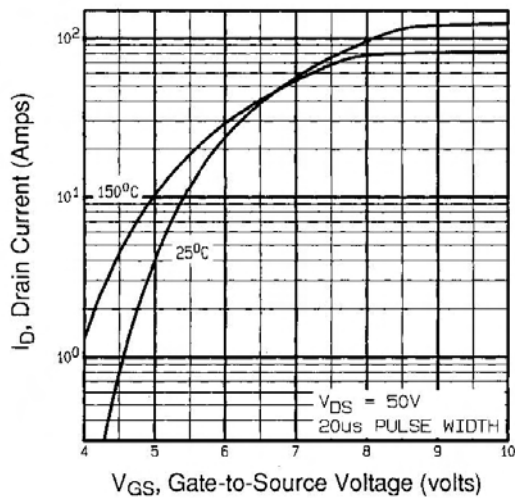


Fig 3. Typical Transfer Characteristics

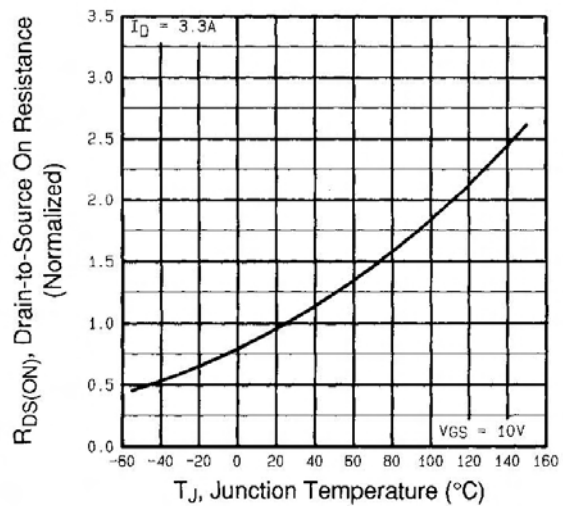


Fig 4. Normalized On-Resistance
Vs. Temperature

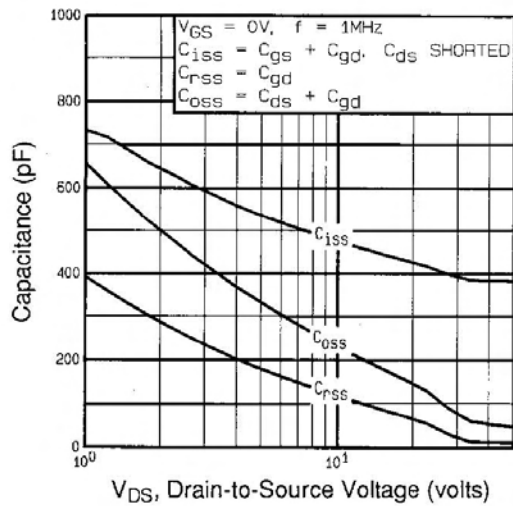


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

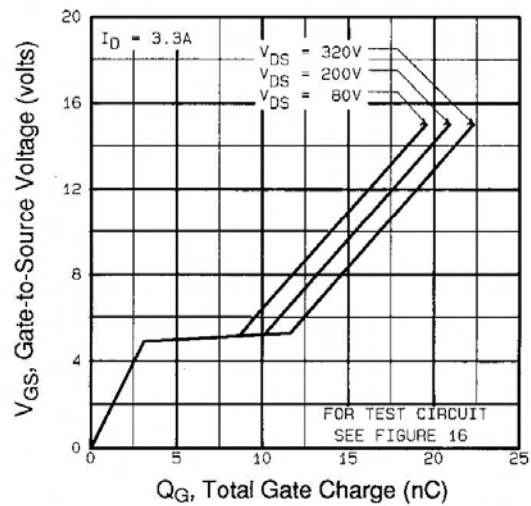


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

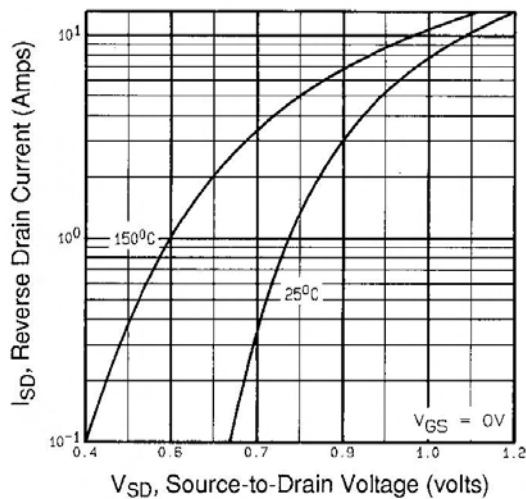


Fig 7. Typical Source-Drain Diode Forward Voltage

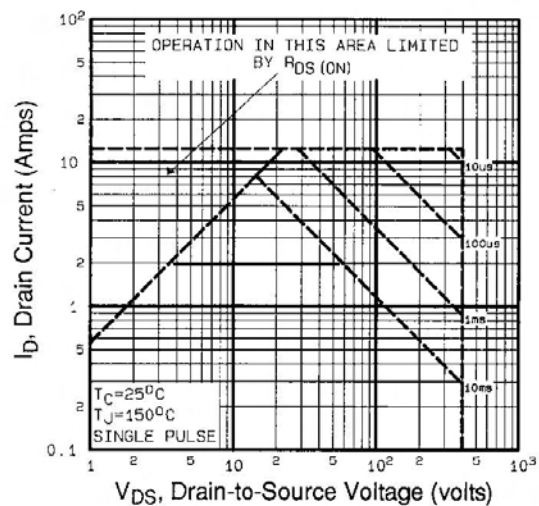


Fig 8. Maximum Safe Operating Area

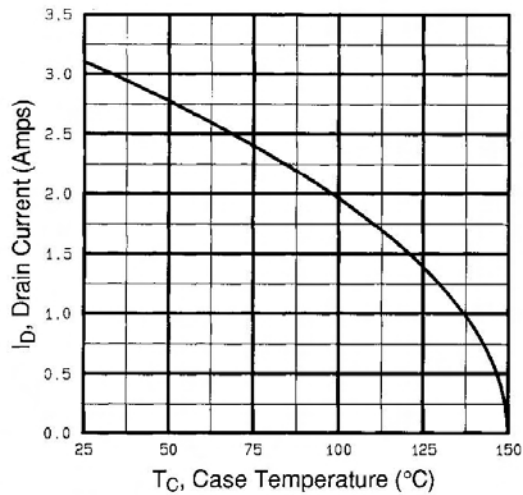


Fig 9. Maximum Drain Current Vs. Case Temperature

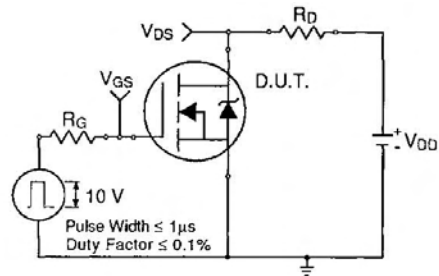


Fig 10a. Switching Time Test Circuit

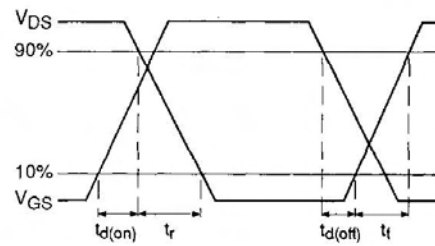


Fig 10b. Switching Time Waveforms

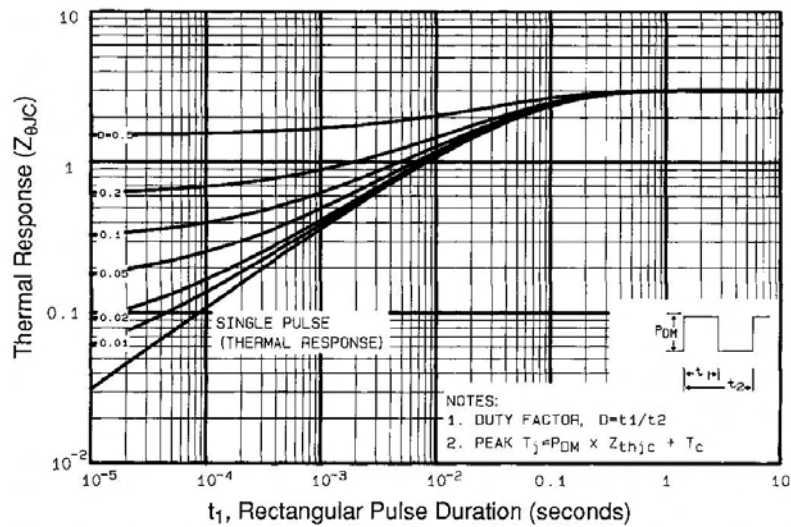


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

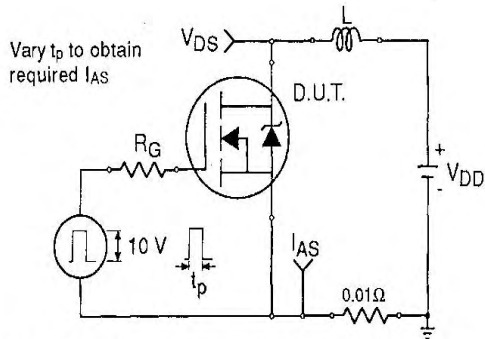


Fig 12a. Unclamped Inductive Test Circuit

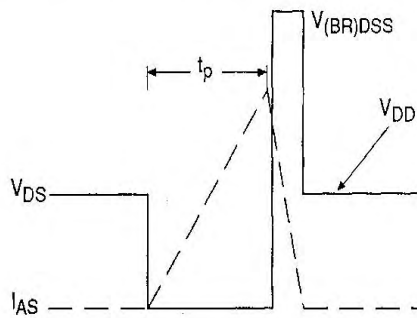


Fig 12b. Unclamped Inductive Waveforms

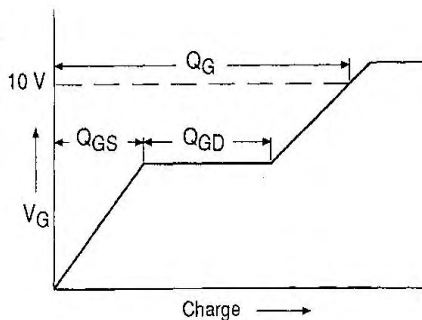


Fig 13a. Basic Gate Charge Waveform

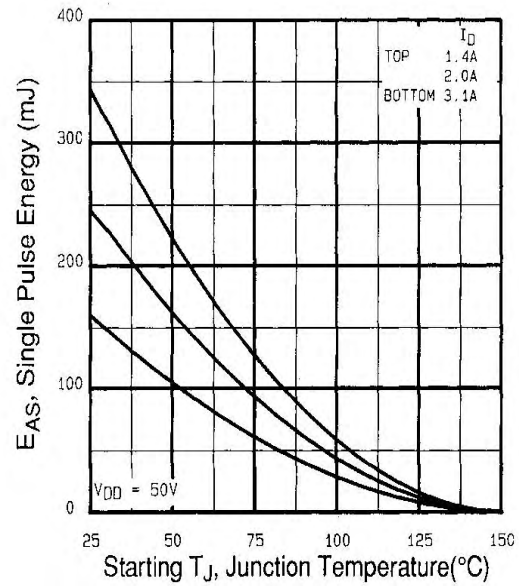


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

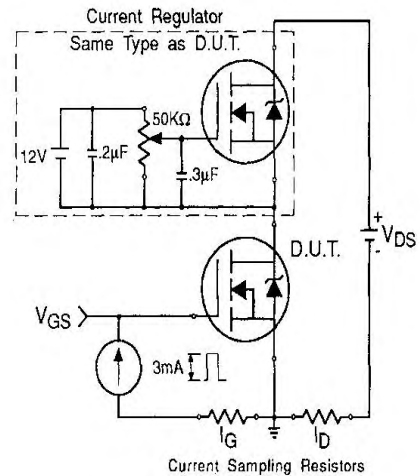
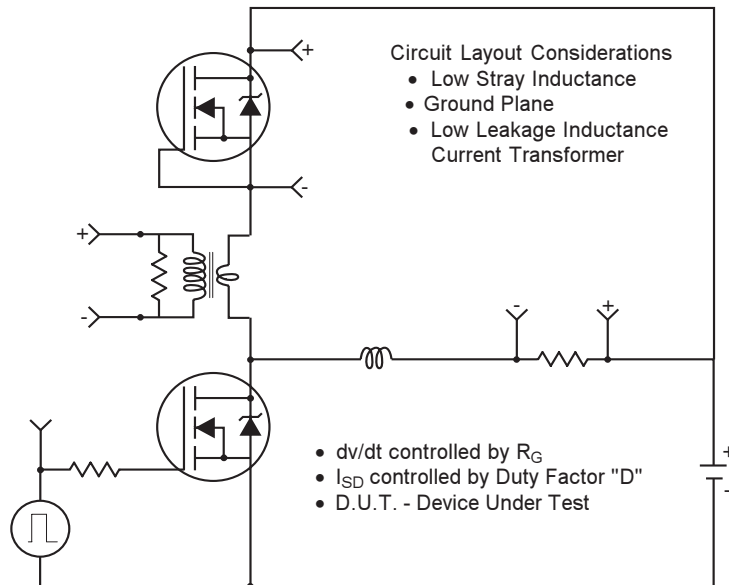


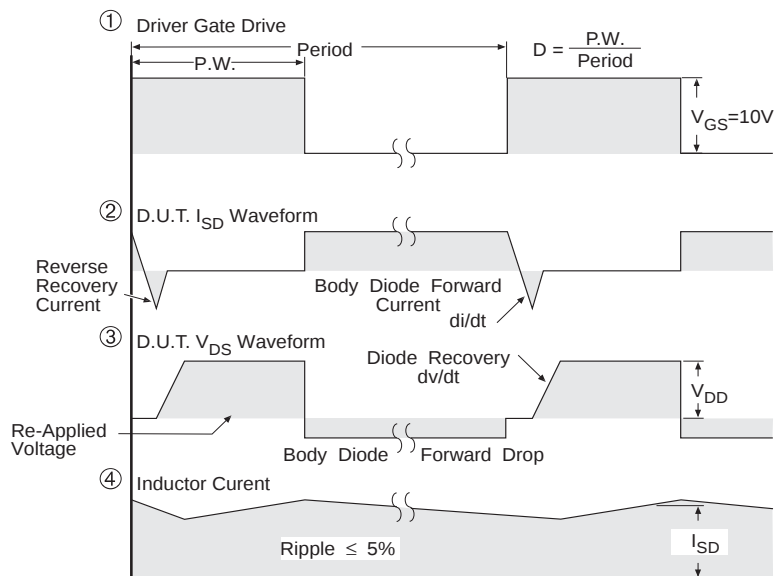
Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel

** Use P-Channel Driver for P-Channel Measurements



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

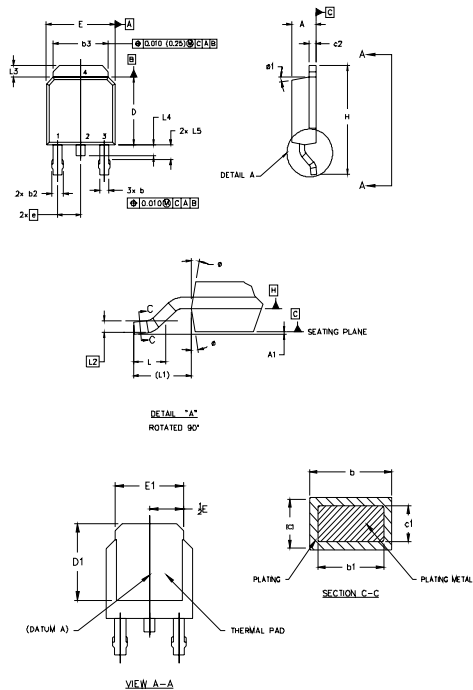
Fig 14 For N Channel HEXFETS

IRFR/U320PbF

International
IR Rectifier

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

- 1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2.0 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.0 LEAD DIMENSION UNCONTROLLED IN L5.
- 4.0 DIMENSION D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.0 SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 [0.127] AND .010 [0.254] FROM THE LEAD TIP.
- 6.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 7.0 OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1		0.13		.005	
b	0.64	0.89	.025	.035	5
b1	0.64	0.79	.025	0.031	5
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	
c	0.46	0.61	.018	.024	5
c1	0.41	0.56	.016	.022	5
c2	.046	0.89	.018	.035	5
D	5.97	6.22	.235	.245	6
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	6
E1	4.32	-	.170	-	4
e	2.29		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.76	.055	.070	
L1	2.74 REF.		.108 REF.		
L2	0.651 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	
L4		1.02		.040	
L5	1.14	1.52	.045	.060	3
ø	0"	10"	0"	10"	
ø1	0"	15"	0"	15"	

LEAD ASSIGNMENTS

HEXFEET

1.- GATE
2.- DRAIN
3.- SOURCE
4.- DRAIN

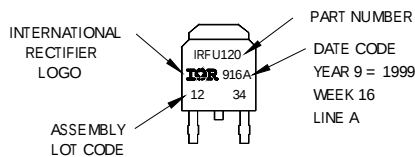
IGBTs, CoPACK

1.- GATE
2.- COLLECTOR
3.- EMITTER
4.- COLLECTOR

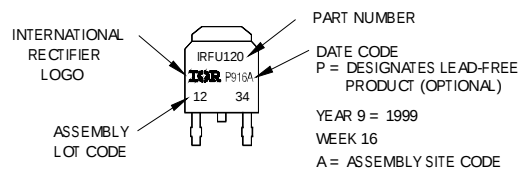
D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON VW16, 1999
IN THE ASSEMBLY LINE "A"

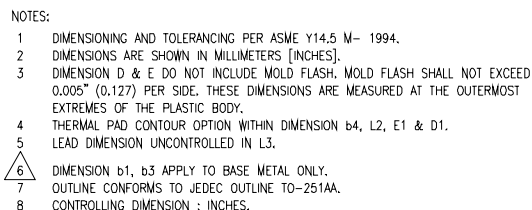
Note: "P" in assembly line position
indicates "Lead-Free"



OR



Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	.094	
A1	0.89	1.14	0.035	0.045	
b	0.64	0.89	0.025	0.035	
b1	0.64	0.79	0.025	0.031	4
b2	0.76	1.14	0.030	0.045	
b3	0.76	1.04	0.030	0.041	
b4	5.00	5.46	0.195	0.215	4
c	0.46	0.61	0.018	0.024	
c1	0.41	0.56	0.016	0.022	
c2	.046	0.86	0.018	0.035	
D	5.97	6.22	0.235	0.245	3, 4
D1	5.21	-	0.205	-	4
E	6.35	6.73	0.250	0.265	3, 4
E1	4.32	-	0.170	-	4
e	2.29		0.090 BSC		
L	8.89	9.60	0.350	0.380	
L1	1.91	2.29	0.075	0.090	
L2	0.89	1.27	0.035	0.050	4
L3	1.14	1.52	0.045	0.060	5
ø1	0"	15"	0"	15"	

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

I-Pak (TO-251AA) Part Marking Information

Note: "P" in assembly line position indicates "Lead-Free"

Diagram illustrating the identification marks on the IRFU120 MOSFET package:

- INTERNATIONAL RECTIFIER LOGO**: Located on the top left of the package.
- PART NUMBER**: IRFU120, located on the top center of the package.
- DATE CODE**: YEAR 9 = 1999, WEEK 19, LINE A, located on the top right of the package.
- ASSEMBLY LOT CODE**: 56 78, located on the bottom center of the package.

OR

Diagram illustrating the markings on the IRF1120 MOSFET package:

- INTERNATIONAL RECTIFIER LOGO**: Points to the top-left corner of the package.
- PART NUMBER**: Points to the top-right corner of the package.
- DATE CODE**: Points to the date code markings (1000, P919A) on the package.
- ASSEMBLY LOT CODE**: Points to the assembly lot code markings (56, 78) on the package.

Additional markings and codes shown:

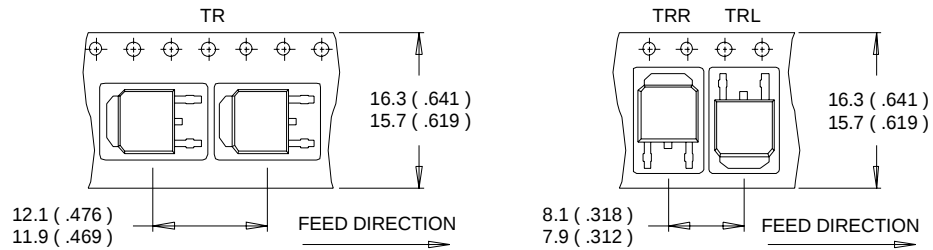
- IRF1120**: Part number printed on the package.
- 1000 P919A**: Date code markings.
- 56 78**: Assembly lot code markings.
- P = DESIGNATES LEAD-FREE PRODUCT (OPTIONAL)**: Legend for the letter P.
- YEAR 9 = 1999**: Legend for the year code.
- WEEK 19**: Legend for the week code.
- A = ASSEMBLY SITE CODE**: Legend for the assembly site code.

IRFR/U320PbF

International
IR Rectifier

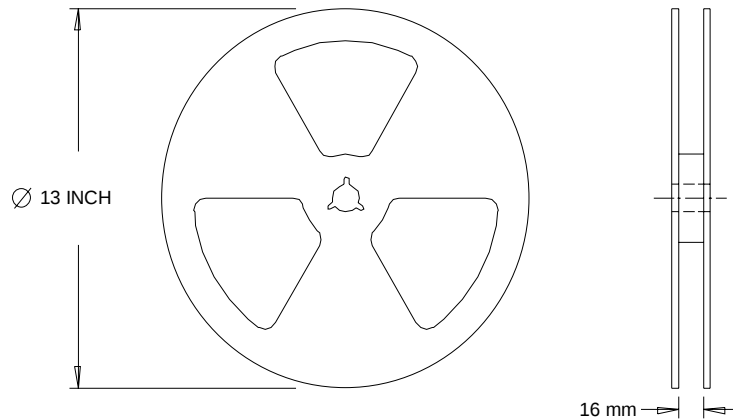
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Data and specifications subject to change without notice.

International
IR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105

TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information.12/04

www.irf.com